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The Pentek Pipeline
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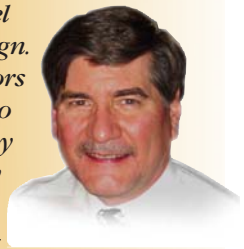
New Virtex-7 FPGAs Boost Software Radio Performance

In This Issue

- FPGAs have profoundly shaped both the application space and performance levels of software defined radios—perhaps more so than any other single technology. More in the feature article.

"FPGAs have clearly revolutionized embedded system board-level product design. FPGA vendors continue to compete by offering new features, better performance, higher density, and lower power."



Rodger Hosking, Pentek Vice President and Co-founder

- **Product Focus:** starts on page 5

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- ***2011*** edition of the *High-Speed A/Ds Handbook*

FPGAs have profoundly shaped both the application space and performance levels of software defined radios—perhaps more so than any other single technology.

Because today's crowded RF landscape imposes very expensive spectrum allocations for each type of radio, licensed carriers must squeeze as much traffic as possible into their licensed bands. The best solution to this problem is software defined radio systems that utilize digital signal processing techniques to replace traditional analog radio components. They can implement precise, complex modulation schemes to maximize the capacity of a channel while constraining the spectrum to its bandwidth limits.

The latest FPGAs from Xilinx include a host of features specifically targeting the signal processing, control, interface, and data transfer requirements of advanced communications and radar systems. These new features have also dramatically influenced architectures of virtually all new board-level products for real-time embedded systems. This article examines some significant design shifts by system engineers who are now exploiting these new FPGAs to address difficult application challenges.

Virtex-7 FPGAs

The newest generation of FPGAs from Xilinx is the Series 7. It consists of three families each targeting specific price/performance spaces. The Artix-7 family addresses low cost, low power, high volume applications. The Kintex-7 family offers a 2X boost in performance over the Virtex-6 devices. Virtex-7 offers the highest performance of the three families with twice the performance and twice the resources of the Virtex-6.

All Series-7 devices feature low-power 28 nm process technology to implement up to 3.1 Tbits/sec of I/O and over 2 million logic cells. They provide up to 6.7 TMACs of DSP resources, especially important for software radio applications. Because of new process technologies and other power management schemes, they consume half the power of Virtex-6 for a given function.

Figure 1 shows the steady improvement in the last four generations of Xilinx FPGAs ➤

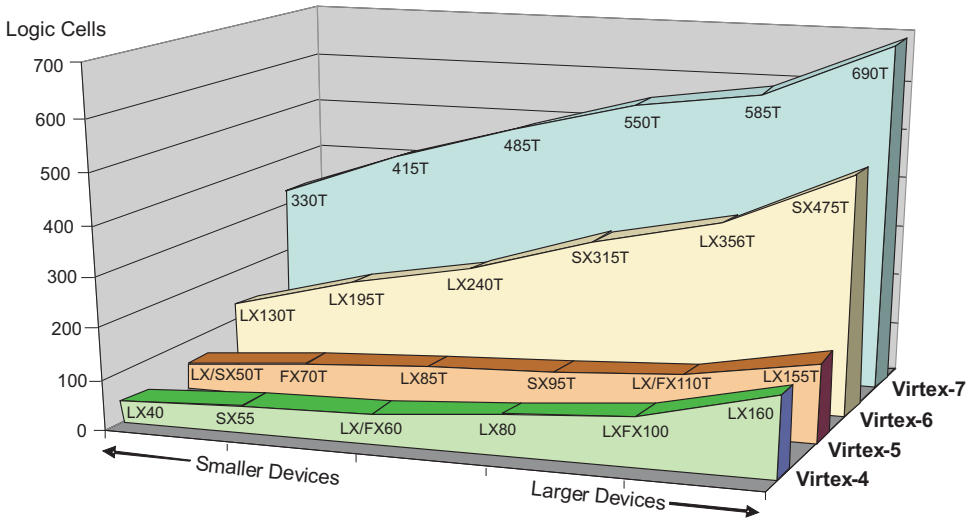

Figure 1. Logic cells in four generations of Xilinx FPGAs in 35 mm x 35 mm BGAs. Shrinking die geometries and improved power management result in significant improvements in device density.

New Virtex-7 FPGAs Boost Software Radio Performance

➤ starting with the Virtex-4 and continuing to the Virtex-7. The graph displays the number of logic cells contained in a range of different density devices offered in a 35 mm x 35 mm BGA package. This clearly shows the dramatic increase in resource density, bounded by the constraints of the size and power dissipation capacity of a given package.

This combination of lower power and higher performance for each of the key resources benefits software radio, opens up new product markets and extends the capabilities of existing applications.

Data Converter Interfaces

To feed the insatiable demand for wireless data service, many newer wideband standards like UMTS and LTE have evolved to deliver data rates up to 1 Gbit/sec. These services require channel bandwidths to 20 MHz and beyond. Other services, such as GSM, operate at more modest channel bandwidths but involve hundreds of channels. For these reasons, one major objective of software radio is to process signals as close to the antenna as possible. This supports flexible software management of the numerous frequency bands; the incorporation of security and encryption schemes; the implementation of various receive and transmit modulation schemes; and beam steering for spatial segregation of radio traffic.

The penalty for putting software radio resources closer to the antenna to handle these wider bandwidths means higher sample rates for the A/D and D/A converters. Early software radio systems operated with modest sample rates of 40 or 65 MHz, but new monolithic data converters are now available with extremely high sample rates.

For example, the National Semiconductor ADC12D1800 3.6 GHz 12-bit A/D converter can digitize signal bandwidths of 1.5 GHz. The digital interface splits the data path into four 12-bit demultiplexed outputs, each operating at 900 MHz. Of course, the problem now becomes how to connect these devices to the necessary signal processing elements. At these high-rates, interconnecting traces require controlled impedances, matched lengths, and proper terminations.

Fortunately, the latest Virtex-7 FPGAs provide a direct connection to these types of high-speed peripheral devices with I/O transfer rates reaching 1.866 GHz. To ease the onerous printed circuit board layout constraints, they include per-bit skew adjustments to help align bits in a data word. They also include digitally-controlled termination networks for tuning optimum performance while eliminating the need for external discrete resistors.

Figure 2 shows a Virtex-7 XMC software radio using the 3.6 GHz A/D converter and taking full advantage of the high-speed I/O capabilities of the FPGA.

Memory Interfaces

Synchronous DRAMs offer the densest and most economical solution for large memory arrays. Developed to support high-end PC processors, DDR3 SDRAMs deliver extremely fast read/write times to support the high-speed data converters. Data transfers to these devices occur at both edges of the clock, and the latest Virtex-7 devices can support DDR3 devices running bit transfer rates up to 1.866 Gbits/sec. Special FPGA I/O pins allow a direct, glueless connection to these memories.

At these speeds, interface timing for each memory must be carefully tuned for reliable operation. For this reason, DDR3 memory controllers must include high-resolution programmable delay elements and training algorithms, so that optimum timing parameters can be calibrated each time the system is powered up.

Xilinx provides the Memory Interface Generator tool that creates an IP core matching the characteristics of DDR3 devices connected directly to the FPGA. The core includes complete resources for initialization, training and delay leveling for reliable read and write operations. Figure 2 shows direct connections from the FPGA to four 1 GB banks of DDR3 SDRAM capable of capturing, buffering and delaying data samples from the 3.6 GHz A/D in real time with no data loss.

Data Buffering

Once high-speed peripherals have been successfully interfaced to the FPGA, the designer must deal with managing the staggering flow of data to and from other system resources. While A/D and D/A converters operate at a constant clock rate, networks and system buses transfer data in packets or blocks.

Block RAM resources of FPGAs can be used as FIFOs to provide an elastic-data buffer for some applications. In other cases, a swinging-buffer memory is more appropriate, especially for block-oriented bus interfaces. A swinging buffer, also built from FPGA internal block RAM, allows one memory bank to be filled from one resource, e.g. an A/D converter, while another bank is being emptied by another resource e.g. the PCIe interface. These schemes are ➤

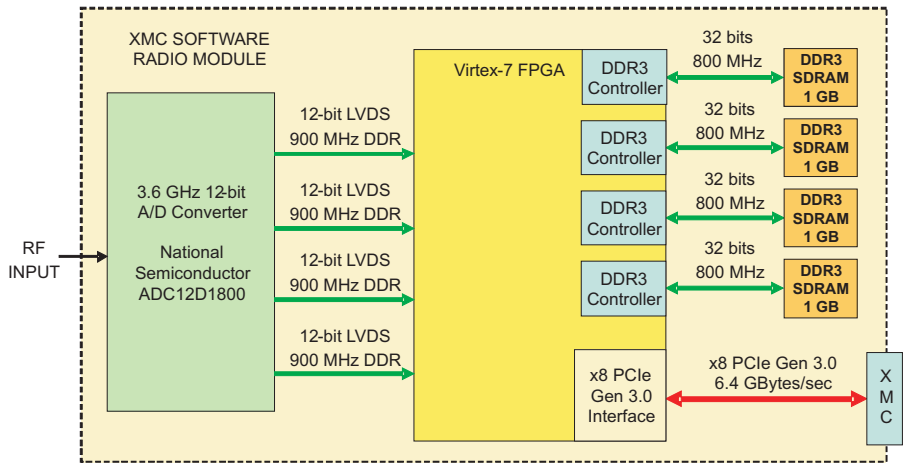

Figure 2. The Virtex-7 provides direct interfacing to a 3.6 GHz A/D converter through four demultiplexed DDR ports operating at 900 MHz each. Four gigabytes of DDR3 SDRAM can capture, buffer and delay A/D data at the full sampling rate. The Gen. 3.0 x8 PCIe interface delivers data at 6.4 GB/sec.

New Virtex-7 FPGAs Boost Software Radio Performance

➤ extremely effective when the average data rate of a peripheral is less than the average rate of the system interface.

The largest Virtex-7 devices now offer more than 10 MB of internal block RAM, more than twice as much as the previous generation.

However, transient capture applications like radar, require a large amount of data to be captured at a very high rate in real time during a range gate, even though the duty cycle of the gate is relatively low. In this case, because FPGA block RAM is too small, external memory must be used, and the specialized SDRAM interfaces discussed above come into play. In these applications, duty cycle averaging allows the system interface to operate at a much lower speed with no data loss.

For example, in a radar system, the 3.6 GHz A/D converter XMC module shown in Figure 2 generates sample data at 4.8 GBytes/sec (assuming 1.5 bytes per sample). For a range gate with 100 msec duration, the capture buffer size must be 480 MB, fitting nicely within any of the four 1 GB SDRAMs. If the duty cycle is 10%, data in the buffer must be delivered to the system interface at an average rate of only 480 MB/sec, a reasonable rate for most embedded systems.

Gigabit Serial Links

Traditional parallel buses have become serious bottlenecks because of high-speed peripherals and processors and high-density packaging. Just as desktop PCs have migrated away from PCI and PCI-X towards PCIe (PCI Express), new embedded system architectures abandon parallel backplane buses in favor of switched serial fabrics and gigabit serial links. The two main advantages are higher speed interconnects and multiple simultaneous paths between software radio system boards and components. More than any other device, FPGAs are the enabling technology for this significant transition.

They provide the low-level electrical interface, the SERDES (serializer and de-serializer), and the 8B/10B encoding engine that delivers clock and data over a single differential pair of copper lines. This interface constitutes the underlying physical and transport layers common to most of the popular gigabit serial standards, including Ethernet, Aurora, PCI Express, and Serial RapidIO.

Protocol engines for specific standards can be configured using FPGA logic so that FPGAs can adapt to different protocols as required. They interface to the SERDES and correctly process protocol-specific packets, header information, control functions, error detection and correction, and payload data format. The strategy makes FPGA-based modules truly “fabric agnostic” and allows one hardware design to be deployed in several different fabric environments.

This flexibility in using one hardware product to cover several different protocols encourages board vendors to develop FPGA-based products for the general market. It also affords system integrators the luxury of not having to commit to any particular standard when selecting boards for their systems.

In their latest Virtex-7 devices, Xilinx offers gigabit serial transceivers with four different bit rates: 6.6 GHz (GTP), 12.5 GHz (GTH), 13.1 GHz (GTX) and 28 GHz (GTZ).

PCI Express

Xilinx FPGAs advance gigabit serial technology even further by including integrated PCI interface blocks for PCI Express that incorporate key layers of the PCI Express protocol stack. This saves FPGA resources for other tasks and offers a standardized solution for sending and receiving data using one of the most popular system protocols.

Some Virtex-7 devices now support the PCI Express Base Specification 3.0 with capabilities for both endpoint and root port. Since each generation also accommodates lower generation devices, the Gen. 3 interface which operates at 8 Gbits/sec is backward compatible with Gen. 2 at 5 Gbits/sec and Gen. 1 at 2.5 Gbits/sec.

The integrated PCI interface blocks can be configured for 1, 2, 4 or 8 lanes and advanced buffering schemes raise the size to 1024 bytes for maximum sustained throughput rates.

OpenVPX

OpenVPX is a new embedded system standard well suited for high-density, high-performance applications. Instead of a parallel bus backplane, it uses direct point-to-point gigabit serial links between backplane connectors in a wide range of interconnect topologies. Each link has groups of differential pairs in both directions in 1x, 2x, 4x, 8x, 16x and 32x lane groups, each supporting any gigabit serial protocol.

The VITA 65 OpenVPX specification defines profiles for backplanes, slots, and modules to standardize on the implementation of system components from various vendors to promote interoperability.

Figure 3 on the following page shows a complete 8-channel OpenVPX beamforming system based on two 3U VPX beamformer modules installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight antenna signals feed RF tuners containing low-noise amplifiers, local oscillators and mixers. The RF tuners translate the antenna frequency signals down to an IF frequency.

The 200 MHz 16-bit A/D converters digitize the IF signals and the DSP48E1 FPGA engines in the FPGA perform further frequency downconversion to baseband. Phase and gain coefficients for each channel are applied to steer the array for directionality. The four weighted baseband signals are summed together. An Aurora engine on each module accepts a sum generated by a previous module and propagates a new sum out to the next module using two 4X gigabit links out to the backplane.

In this system the top left module sends its 4-channel sum to the bottom left module to form the final 8-channel sum. This is delivered to the CPU module in slot 3 over the x4 PCIe interface. In addition, the CPU module uses these PCIe links for initialization, status and control of the two beamformer modules.

Here the Virtex-7 FPGA provides interfaces to the A/D converters; performs the digital downconversion; implements the beamforming phase shift and gain adjustments; sums the channels together; links the summation Aurora chain across the backplane; provides a PCIe interface to the CPU; and implements all control, data flow, synchronization and timing within each module. ➤

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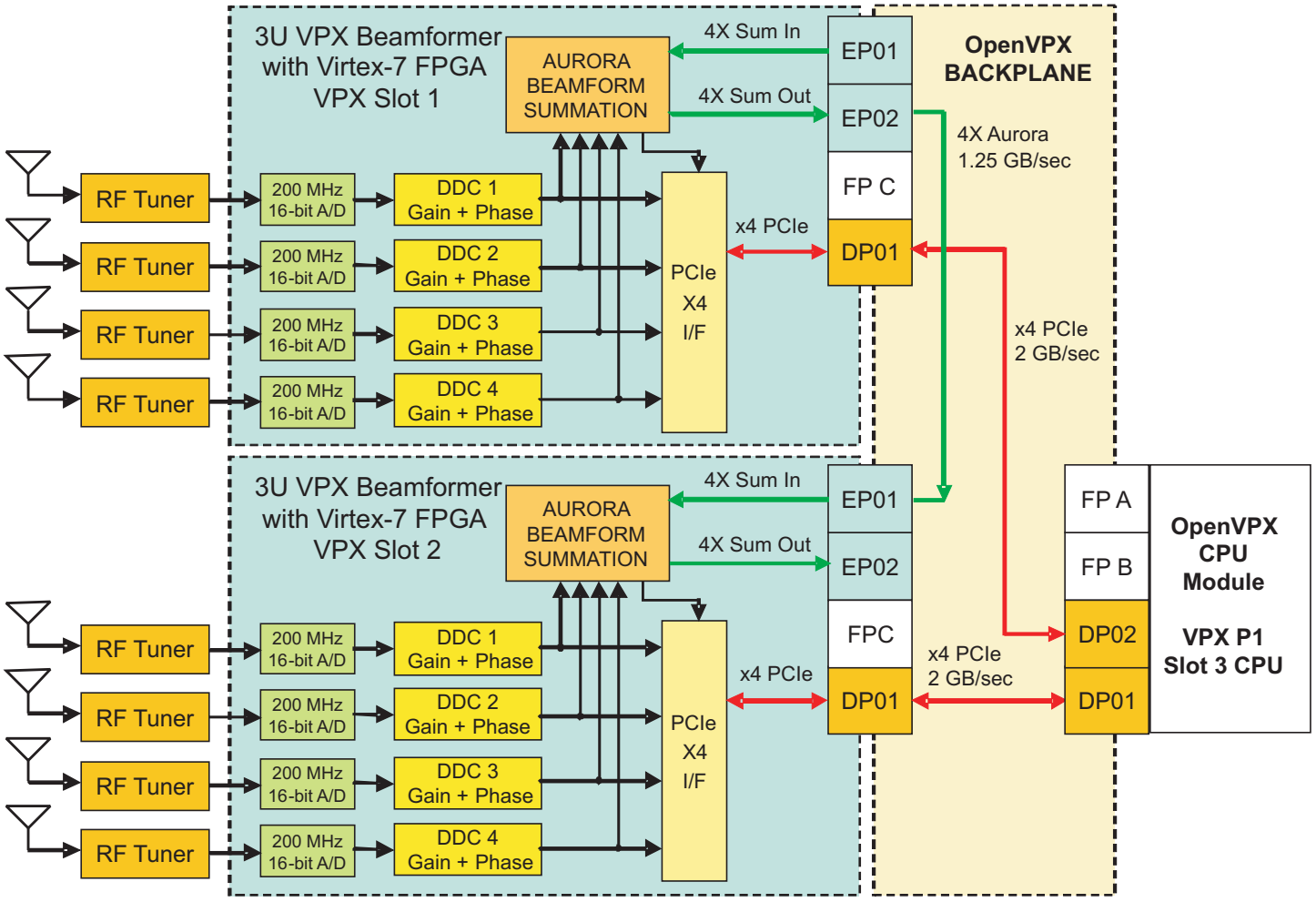

Figure 3. 8-Channel 3U OpenVPX Beamforming System. Gigabit serial links on the backplane support the 4X Aurora beamforming chain at 1.25 GB/sec between two boards as well as x4 Gen. 2 PCIe ports for control, data and status at 2 GB/sec in slot 3.

Summary

The system example above clearly shows that, except for the A/Ds, every other aspect of the module is implemented with FPGA technology. No other design approach is viable, except for a custom ASIC solution, practical only for high volume production.

When coupled with their impressive DSP capabilities, FPGAs have clearly revolutionized embedded system board-level product design. FPGA vendors continue to compete by offering new features, better performance, higher density, and lower power. To take the best advantage of these powerful components, software radio system designers must constantly keep abreast of frequent announcements. ❑

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Product Focus

Model 71662

32-Channel Digital Downconverter with four 200 MHz, 16-bit A/Ds and Virtex-6 FPGA - XMC

General Information

Model 71662 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

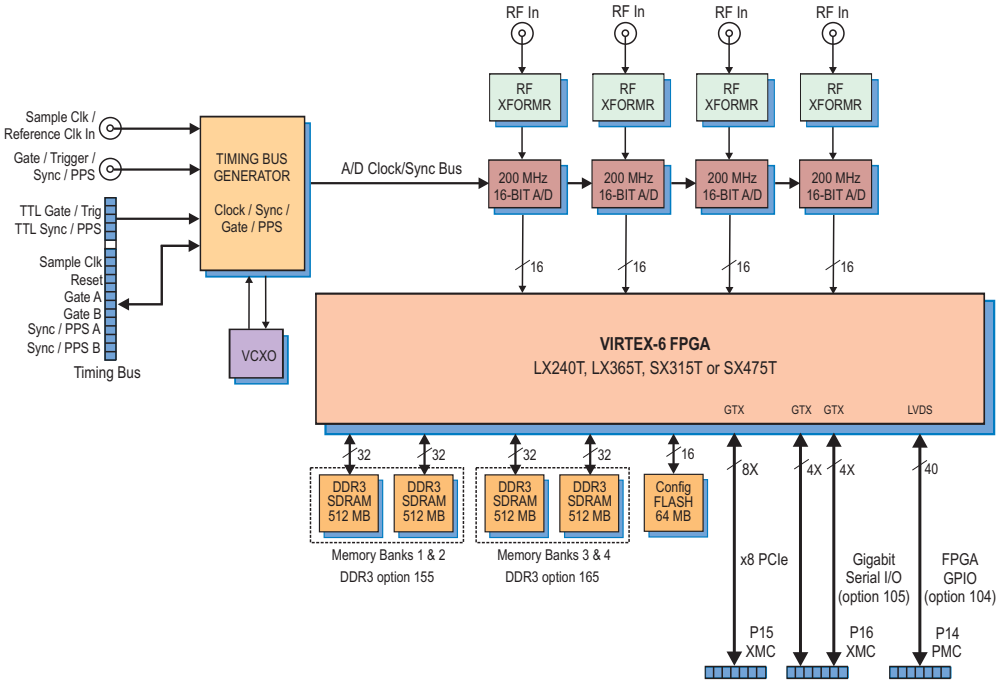
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71662 factory-installed functions include four A/D acquisition IP modules.

Model 71662 is also available in OpenVPX, PCI Express and CompactPCI formats.

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- User-configurable serial gigabit interfaces
- LVDS connections to the Virtex-6 FPGA for custom I/O

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 71662 to operate as a complete turnkey solution without the need to develop any FPGA IP.



DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For more information and a price quotation on the Model 71662, go to:

pentek.com/go/pipe71662 ❑

Product Focus
Model 78690

L-Band RF Tuner with 2-Channel 200 MHz 16-bit A/Ds and Virtex-6 FPGA - x8 PCIe

Model 78690 is also available in XMC, OpenVPX and CompactPCI formats.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8

General Information

Model 78690 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

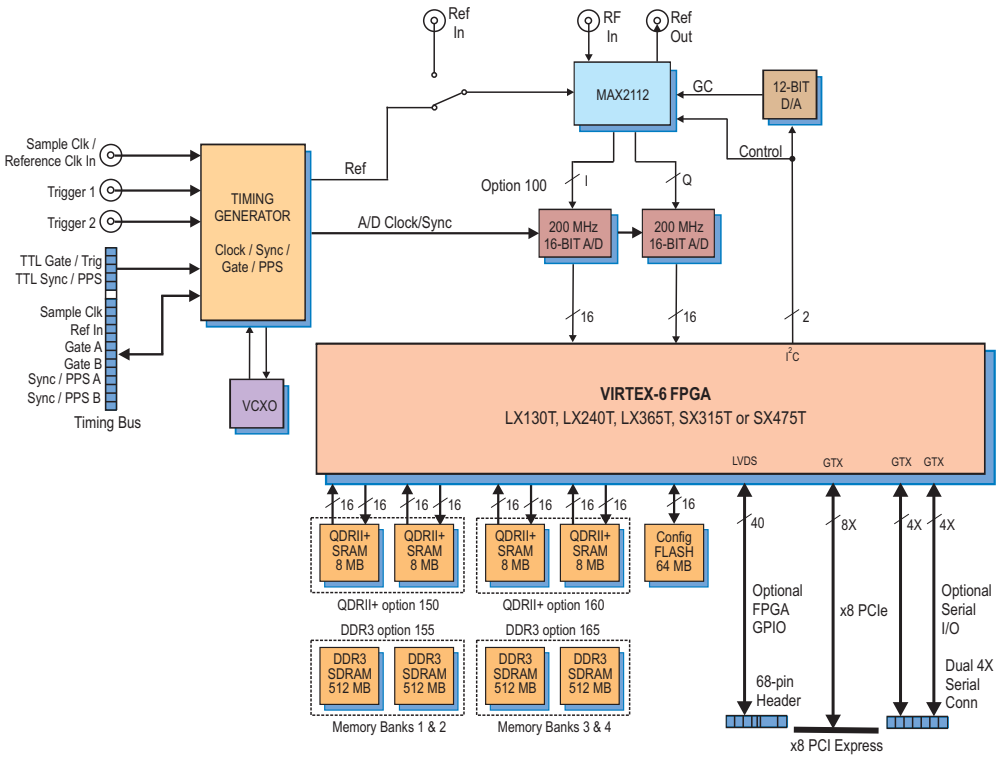
It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78690 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78690 to operate as a complete turnkey solution without the need to develop any FPGA IP.



RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

For more information and a price quotation on the Model 78690, go to:

pentek.com/go/pipe78690 ❑

Product Focus

Model 53640

1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D and Virtex-6 FPGA - 3U VPX

General Information

Model 53640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

Model 53640 COTS and rugged versions. This model is also available in XMC, PCI Express and CompactPCI formats.

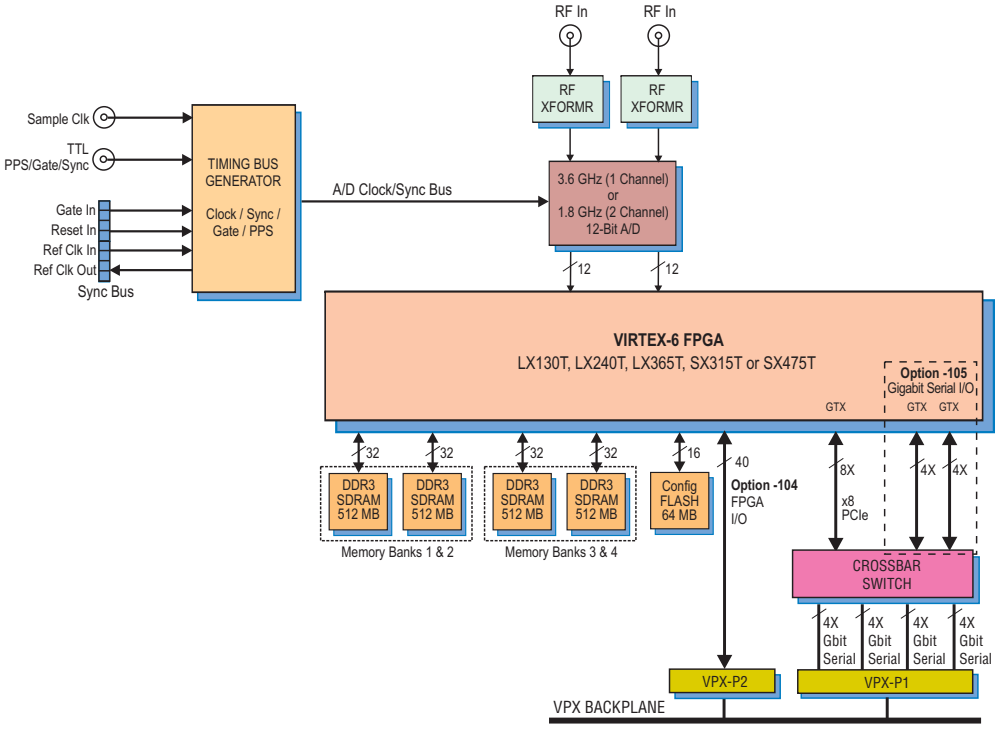
Features

- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.



A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a National Semiconductor ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, or for routing to other board resources.

PCI Express Interface

The Model 53640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

For more information and a price quotation on the Model 53640, go to:

pentek.com/go/pipe53640 ❑

Product Focus
Cobalt Boards

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Models 72620, 73620, 74620: Transceivers, with three or six 200 MHz A/Ds, DUCs and two or four 800 MHz D/As

- Product Information:
  - Model 72620 - 6U cPCI, single density
  - Model 73620 - 3U cPCI, single density
  - Model 74620 - 6U cPCI, double density

Models 72660, 73660, 74660: 4- or 8-Channel 200 MHz, 16-bit A/Ds

- Product Information:
  - Model 72660 - 6U cPCI, single density
  - Model 73660 - 3U cPCI, single density
  - Model 74660 - 6U cPCI, double density

Models 72640, 73640, 74640: 1- or 2-Ch. 3.6 GHz and 2- or 4-Ch 1.8 GHz A/Ds

- Product Information:
  - Model 72640 - 6U cPCI, single density
  - Model 73640 - 3U cPCI, single density
  - Model 74640 - 6U cPCI, double density

Models 72621, 73621, 74621: Models 72620, 73620, 74620 with wideband DDCs and Interpolation Filters

- Product Information:
  - Model 72621 - 6U cPCI, single density
  - Model 73621 - 3U cPCI, single density
  - Model 74621 - 6U cPCI, double density

Models 72661, 73661, 74661: Models 72660, 73660, 74661 with DDCs and Beamformers

- Product Information:
  - Model 72661 - 6U cPCI, single density
  - Model 73661 - 3U cPCI, single density
  - Model 74661 - 6U cPCI, double density

Models 72662, 73662, 74662: Models 72660, 73660, 74661 with 32- or 64-Channel DDC

- Product Information:
  - Model 72662 - 6U cPCI, single density
  - Model 73662 - 3U cPCI, single density
  - Model 74662 - 6U cPCI, double density

Models 72630, 73630, 74630: 1 GHz A/Ds, 1GHz D/As

- Product Information:
  - Model 72630 - 6U cPCI, single density
  - Model 73630 - 3U cPCI, single density
  - Model 74630 - 6U cPCI, double density

Models 72650, 73650, 74650: Transceivers, with two or four 500 MHz A/Ds, one or two DUCs and two or four 800 MHz D/As

- Product Information:
  - Model 72650 - 6U cPCI, single density
  - Model 73650 - 3U cPCI, single density
  - Model 74650 - 6U cPCI, double density

Models 72690, 73690, 74690: One or Two RF L-Band Tuners with Two or Four 200 MHz A/Ds

- Product Information:
  - Model 72690 - 6U cPCI, single density
  - Model 73690 - 3U cPCI, single density
  - Model 74690 - 6U cPCI, double density