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Interview: Rodger Hosking on Signal Processing

A Window on the Embedded Computing World, January 4, 2010

Rodger Hosking, Pentek Vice President and Cofounder has seen many generations of signal processing come and go. He discussed a variety of current topics of interest with *Open Architecture Review*, including the emergence of point-to-point serial links, the roles of VXS and VPX, mezzanine trends, the FPGA phenomenon and the uncertain future of general-purpose DSPs in military and government electronics.

Open Architecture Review

OAR: The system interconnect of the past was primarily the parallel bus, and now it's the point–to-point (P2P) serial link. How has this changed signal processing?

HOSKING: It has pretty much revolutionized our architectures. About three years ago, we migrated our VME designs towards VITA 41 VXS, which augments parallel VME with gigabit serial interfaces on the same board. That's very effective for solving some problems where VME used to be a bottleneck.

OAR: And VXS lets you continue to use legacy VMEbus boards, right?

HOSKING: Yes, and there are going to be an awful lot of designs going forward that will still use VME and legacy boards over the next ten to fifteen years. And when the VME backplane is not sufficient to handle the bandwidth you need, you can use VXS to give you rates that are twenty times higher than what VME can do.

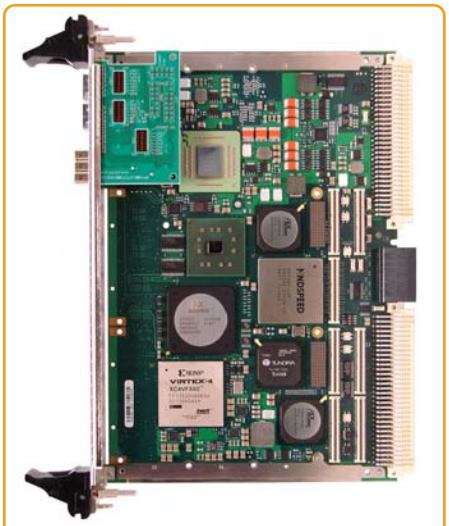
VXS

OAR: Doesn't having to handle all that traffic introduce some complications?

HOSKING: Sure. As I said, we've pretty much revolutionized our architectures because of it. We've moved from communicating over a shared resource, a bus, to communicating via direct pathways with no contention. The architectures are fundamentally different.

OAR: Can you point to one relevant difference in board architecture?

HOSKING: To support the change for one particular processor board, we incorporated a gigabit serial crossbar switch to serve as the traffic cop for on-board resources, connecting a PowerPC processor, XMC mezzanines, FPGA resources and backplane. That's a major change for us.



Pentek VXS PowerPC Processor Board

OAR: How is the market trending in mezzanine boards? Where is there movement to XMC and serial P2P links? Where are people staying with PMC and its legacy parallel PCI bus?

HOSKING: PMCs are being replaced by XMCs to add the gigabit serial links. We originally made PMC modules, then shifted to hybrid XMC modules with both PMC and XMC connectors on them, and our latest introduction has XMC connectors only. You can see the progression from parallel, to parallel plus serial, to straight serial.

OAR: Pentek chose PCI Express as its P2P link. Why PCI Express? ➤

Interview: Rodger Hosking on Signal Processing

HOSKING: PCI Express is really nice because you can reuse a lot of the software you've previously developed for PCI and PCI-X under Windows or Linux and not have to do very much to it to support the shift from parallel buses to serial P2P links. A lot of the software remains the same.

OAR: Do you support PCI Express exclusively?

HOSKING: At this point we're promoting PCI Express as the standard control and data plane fabric, but we're also supporting and delivering the Xilinx Aurora protocol. We just announced a family of beamforming products for software radio, communications and radar. They use PCI Express for controlling and loading data on and off the modules, but they also use the Aurora protocol as a high-speed interconnect between boards in the form of a daisy chain.

OAR: Doesn't PCI Express provide that capability?

HOSKING: Aurora is a very low-level, lightweight protocol with very low overhead, whereas PCI Express has many layers of protocols and conventions you have to follow in order to be a true PCI Express entity. Something like Aurora is the best way to handle the high-speed summation across multiple channels, which is the critical operation in beamforming.

OAR: Do you run Aurora over the VXS backplane?

HOSKING: No, over cables, like people always did (and some people continue to do) with the old FPDP (Front Panel Data Port). We can daisy chain boards down a card cage as many slots as required, pretty much without limit, by simply attaching cables for the gigabit serial connection. At the end, you pull out the final sum and send it out across the PCI Express interface; but from the beginning to the end of the daisy chain, you don't have to rely on the motherboard or carrier at all. It really simplifies a lot of the beamforming operations people need to do.

Pentek PCI Express SDR Board

OAR: You're supporting Aurora on a PCI Express board. If you did the same on a VXS or VPX board, would you continue to use cable for the traffic?

HOSKING: That depends on what it's attached to. The cables that we provide for the PC environment are definitely not what people are looking for in a military VPX chassis. There, Aurora links would probably be done through backplane connectors, and the boards could either be joined by a switch board or by a custom backplane that's hardwired between slots to provide the daisy chaining capability.

OAR: Regarding VXS, I see very little activity in support of it these days, and most VXS suppliers seem to be plunging into VPX as rapidly as possible. Is there a shift going on here? Was VXS just a short-term, transitional standard?

HOSKING: VXS was definitely a transitional move. It represents a shift from parallel only to parallel plus serial. The next shift is to serial only: that is, to VPX. The same shift is going on in mezzanines: first from PMCs to XMCs with both PMC and XMC connectors, and then to XMC-only boards.

OAR: So what are your VPX intentions?

HOSKING: We will be announcing a VPX product line in Q1 2010, primarily for 3U and eventually for 6U VPX.

OAR: Pentek didn't have a small form-factor 3U line for VXS?

HOSKING: There's no room for a P0-type connector on a 3U board. But VPX made provisions ahead of time for both 3U and 6U, and things are extremely well laid out and defined. The 3U VPX specification is more mature and more uniform across suppliers than 6U.

OAR: Has the stampede to VPX we've been seeing been influenced by the OpenVPX collaboration?

HOSKING: Very much so. The OpenVPX initiative, the migration to VITA 65 in October, 2009, and its eventual adoption by ANSI will do a lot towards unifying the market.

OAR: When do you expect ANSI adoption?

HOSKING: The first quarter of 2010 or so.

OAR: What motivated OpenVPX was the real-world interchangeability difficulties users have been having with VPX boards. Does the new specification solve the problem?

HOSKING: There are still quite a few government agencies and organizations that are concerned that VPX is not yet stable enough. They want to know that the VPX system they buy today will accept future boards from different vendors, and that everything will work together. I expect their fears will fade over the next year or so.

OAR: What has been causing the incompatibilities?

HOSKING: It's just based on the individual choices that designers made when they put together the first VPX boards and systems.

OpenVPX™

OAR: Examples?

HOSKING: Clock distribution and management, chassis configuration and control, naming the various Gbit lane bonding conventions, and defining slot profiles for different types of VPX cards. Many of these issues were addressed in the OpenVPX effort.

OAR: Did the same type of problem arise with VXS?

HOSKING: Because VXS is simpler with only two 4X VXS ports on any card, there were fewer design choices. Even so, there are several flavors of both switched and switchless VXS backplanes. With VPX, though, each card can have 20 or more different ports ranging from 1X to 16X, all needing to go to specific destinations. VPX has the capability for doing a lot of very, very high-performance embedded computing, but that freedom comes with a penalty in how all those interconnects are actually implemented.

OAR: So what does the near term look like for VPX?

HOSKING: We see a lot of vendors lining up with available products. ➤

Interview: Rodger Hosking on Signal Processing

One complication is that VPX will require a diverse range of backplanes, which is quite different from VME. There will probably be four or five popular backplane configurations, but major programs will probably require custom backplanes with specific interconnections. That wasn't the case with VME.

OAR: Will VXS just wither away and eventually die?

HOSKING: Someday, but VME will definitely help prolong VXS. For us, VXS was a very positive thing and an important stepping stone. It really helped enormously to get VPX started because it got us building hardware and software to support interboard gigabit serial links. Once we developed software for VXS boards, we were immediately able to take advantage of the interfaces and drivers for VPX as well.

OAR: Have the P2P serial links in any sense been a leveler in terms of performance differences between motherboards and backplanes?

HOSKING: You can do a tremendous amount of processing and achieve a very high interconnect bandwidth in the lower cost motherboard environment, but bandwidth isn't everything. The trouble is that PCs are not very good in unfriendly environments. Also, as you get into higher density products, thermal management and adequate air flow become a problem because the PC is not a very good environment for cooling. VME or VPX or CompactPCI are much better at handling the heat than a PC.

OAR: Any other caveats?

HOSKING: Yes. The PCI Express slot connectors that are found on motherboards often don't have enough amperage on the pins to power up the devices that are being plugged into them. So, for the PMC carriers we've done for PCI Express, we've had to implement separate power connectors that go directly to the power supply.

OAR: In the past, I've seen FPGAs here and there on various board-level products, but these days they're being widely used, especially in DSP environments. Why and why now?

HOSKING: FPGAs have a traditional role of providing multiple hardware engines that perform a lot of DSP operations in parallel. What has happened more recently is that Xilinx and Altera incorporated gigabit serial engines as dedicated blocks right inside their FPGAs, making it easy for people to incorporate those serial interfaces.

Also, the high-speed devices we are typically involved with — high-speed A/Ds, D/As, network interfaces, serial FPDP, etc. — are all supported beautifully with the configurable I/O that FPGAs provide. So, you can comply with a lot of different logic levels and signaling rates up in the hundreds of MHz, and tune the I/O to match the characteristics of the peripherals you're trying to connect to.

OAR: That's a pretty powerful story.

HOSKING: It gets better. You can now also get memory controllers, either from the FPGA vendors themselves or third parties that install inside the FPGA to allow you to interface to virtually any kind of external memory available. And the icing on the cake is that the devices have become faster and denser with each new generation. The latest version of Virtex-6 from Xilinx has over 2000 DSP engines on board, each capable of performing multiply/accumulate/add operations in parallel — that's tough competition for a general-purpose DSP!

OAR: So will general-purpose DSPs wither away and die?

HOSKING: They've definitely waned in popularity in our markets. That's because over the past ten years, the leader, Texas Instruments, has focused on the telecom market. As a result, the DSP chips are mostly fixed-point devices and they tend to have dedicated telecom peripheral interfaces on board. Our markets in military/government electronics like to use floating point because it's easier to have an algorithm work properly without having to worry about scaling and dynamic range.

OAR: So Pentek doesn't see any general-purpose DSPs in its future?

HOSKING: That depends. If, for example, the telecom market appears to be getting saturated and TI gets competition for its DSPs from overseas knockoffs, they might start seeing our embedded markets as an opportunity and perhaps extend their offerings. We'd look closely at anything they might do in getting back to floating-point DSPs. We'd definitely not just give up FPGAs because they do so many different things, but we'd look at a good credible, competitive DSP.

OAR: Competitive in what sense?

HOSKING: There are two things a DSP could compete on: power consumption and cost. FPGAs are expensive and they draw a lot of power. If TI could come in and handle the algorithm number crunching we're using FPGAs for, but at a lower cost and lower power, that might be interesting.

OAR: Do you see any other trends in signal processing?

HOSKING: We definitely see more and more people using Windows and Linux, as opposed to the more traditional real-time embedded operating systems like VxWorks. Customers don't like the run-time licensing and the development tool costs. VxWorks is an excellent product, but we're seeing that when people can get away from it, they often do. ❑

Pentek XMC Software Radio Board with Virtex-6 FPGA

Follow VPX updates at:
pentek.com/go/vpxcentral

We thank OAR for allowing us to publish this interview in The Pentek Pipeline.

Product Focus

Model 71620

Software Radio XMC with Virtex-6 FPGA is the First Member of the Pentek Cobalt™ Family

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz, 16-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Clock Synthesizer with independent A/D and D/A rates
- LVPECL clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71620 is the first member of the Cobalt™ family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications and radar system. It includes three A/Ds, one upconverter, two D/As, and four banks of memory. The Model 71620 is compatible with the VITA 42.0 XMC format and supports PCI Express Gen. 2 as a native interface.

A/D Converter

The front end accepts three full scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/Ds.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A

A TI DAC5688 DUC (digital upconverter) with two D/As accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

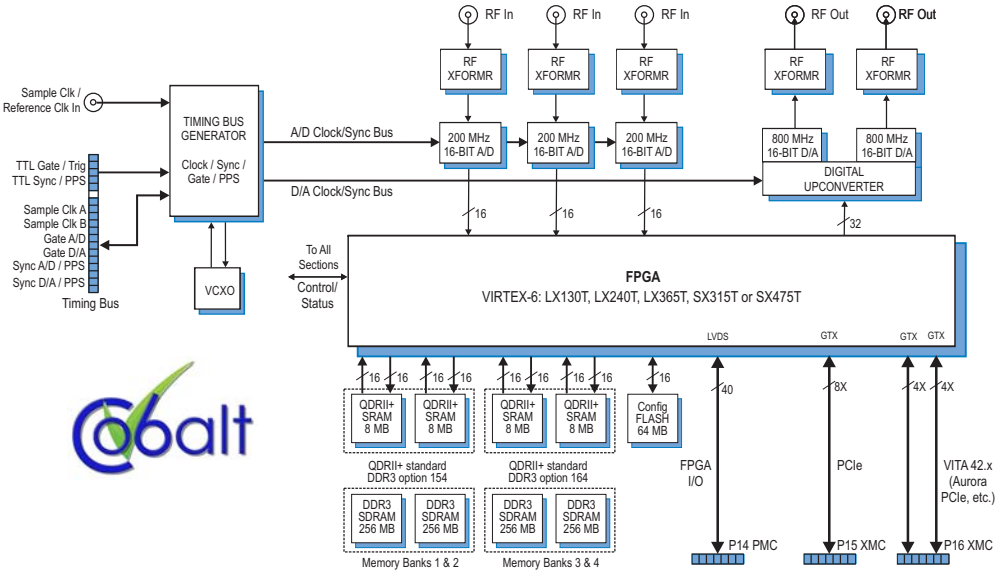
If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of x2, x4 and x8.

Xilinx Virtex-6 FPGA

The Model 71620 Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and memory control. In addition to the built-in functions, users can install their own custom IP for data processing with the Pentek GateFlow FPGA Design Kit.

The FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the data converters, DDR3 SDRAM or QDRII+ SRAM memory, PCIe interface, programmable LVDS I/O, and clock, gate and synchronization circuits.

The FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-6 LX130T, LX240T, LX365T, SX315T, or SX475T.



Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync, and a gate or trigger signal. An internal clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by the clock synthesizer circuit to provide different A/D and D/A clocks.

For more information please go to: pentek.com/go/pipe71620. ❑

Product Focus

Model 7158

New Software Radio PMC/XMC Captures and Processes Very Wideband Signals

Model 7158 is also available in PCI, PCIe and cPCI formats

ReadyFlow Board Support Package GateFlow

Features

- Two 500 MHz, 12-bit A/Ds
- One digital upconverter
- Two 800 MHz, 16-bit D/As
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Dual timing buses for independent A/D and D/A clock rates
- LVPECL clock/sync bus for multimodule synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O on P14

General Information

Model 7158 is a dual-channel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters, two Virtex-5 FPGAs and two banks of DDR2 SDRAM. The Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

A/D Converter

The front end accepts two full-scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into TI ADS5463 12-bit 500 MHz A/Ds. Designed with a 750 MHz input bandwidth, the A/Ds are excellent for undersampling applications.

The digital outputs are delivered to the Virtex-5 FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 300 MHz. It delivers real or quadrature (I+Q) outputs at up to 500 MHz to the 16-bit D/A converter. Analog output is through a pair of front panel SMC connectors at +4 dBm into 50 ohms. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of x2, x4, and x8.

Virtex-5 FPGAs

The Model 7158 architecture includes two Virtex-5 FPGAs. The processing FPGA serves as a control and status engine with data and programming interfaces to all of the on-board resources.

A second Virtex-5 FPGA provides the board's PCI-X interface. Implementing the interface in this second FPGA keeps the processing FPGA resources free for signal processing.

Option -104 adds the P14 PMC connector with 16 pairs of LVDS connections to each FPGA for custom I/O.

XMC Interface

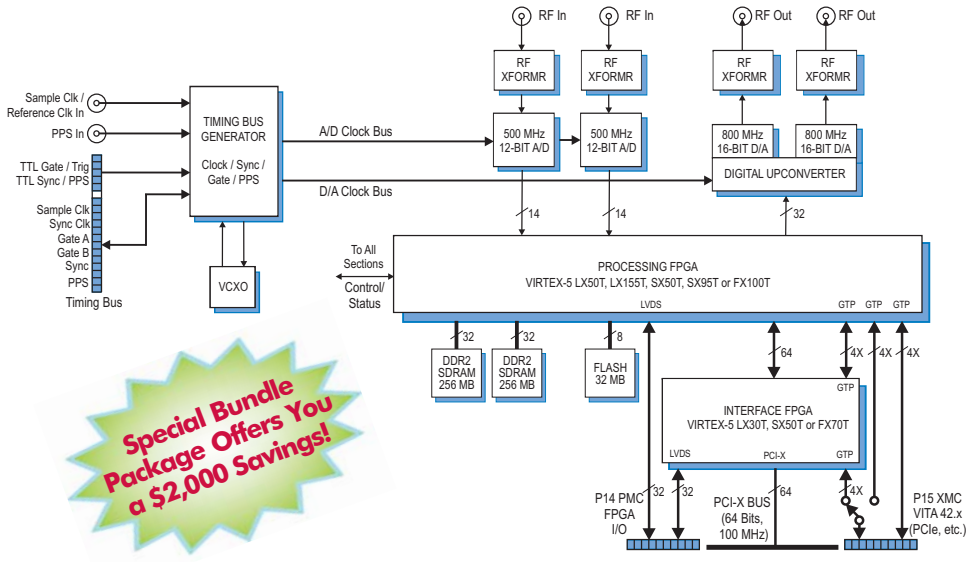
The Model 7158 complies with the VITA 42.0 XMC specification for carrier boards. This standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the 7156 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Clocking and Synchronization

Two internal timing buses can provide either a single clock or two different clock rates to the A/D and D/A signal paths.

A front panel LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

For more information on this product and the bundled discount, go to: pentek.com/go/pipe7158B. ❑



Special Bundle Package Offers You a $2,000 Savings!

Product Focus

Model 7153

4-Channel Beamformer with four 200 MHz 16-bit A/Ds

Ideal for Radar and Software Radio Applications

Model 7153 is also available in PCI, PCIe and cPCI formats

ReadyFlow Board Support Package

Features

- Built-in Beamformer supports multiboard systems
- Programmable Power Meter and Threshold Detect per channel
- Four 200 MHz, 16-bit A/Ds
- 2 or 4 Channels of DDC
- Independent DDC tuning and decimation factors for each channel
- DDC decimation range from 2 to 256 or from 2 to 65536
- Default filters offer 0.2 dB ripple and 100 dB rejection
- LVPECL clock/sync bus for multimodule synchronization

General Information

Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) and a complete set of beamforming functions. With built-in multiboard synchronization, it is ideally matched to the requirements of real-time software radio and radar systems.

A/D Converters

The front end accepts four full-scale analog RF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling to four Texas Instruments ADS5485 200 MHz, 16-bit A/Ds.

The digital outputs are delivered into a Xilinx Virtex-5 FPGA for routing, formatting and DDC signal processing operations.

DDC Input Selection and Tuning

The Model 7153 employs an advanced FPGA-based digital downconverter engine consisting of two or four DDC channels. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC channel. In this way, many different configurations can be achieved including one A/D driving all four DDC channels and each of the four A/Ds driving its own DDC bank.

Decimation and Filtering

Each of the four DDC channels can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. The DDC core can be configured in four-channel mode with each channel offering decimations between 2 and 256, or in two-channel mode with each channel having a decimation range of 2 to 65536, for applications that require a wider range of decimations.

The decimating filter for each DDC channel accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

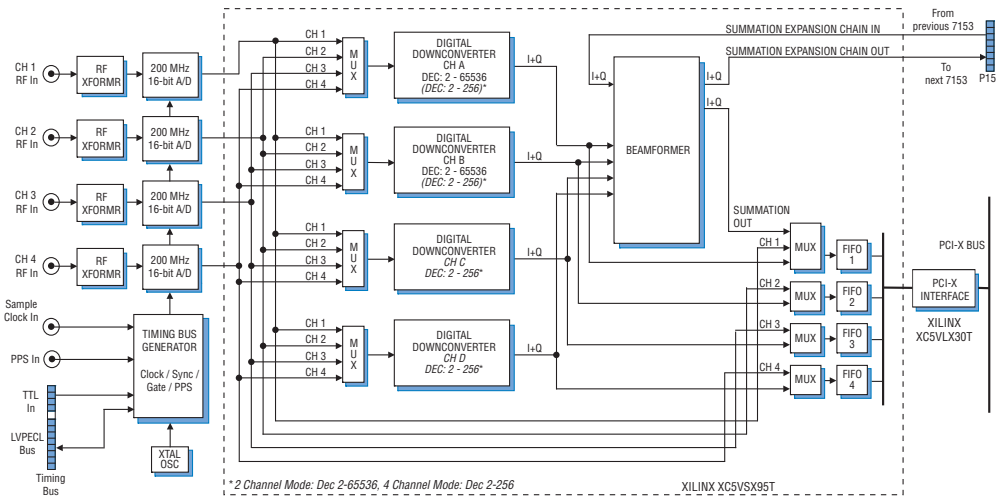
Beamformer

In addition to the DDCs, the 7153 features a complete beamforming subsystem. Each channel contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 ksamples. The power meters present average power measurements for each channel in easy-to-read registers.

In addition, each channel includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four output channels. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed to the Channel 1 FIFO for reading over PCI-X. For larger systems, multiple 7153's can be chained together via a built-in Xilinx Aurora interface through the P15 XMC connector.

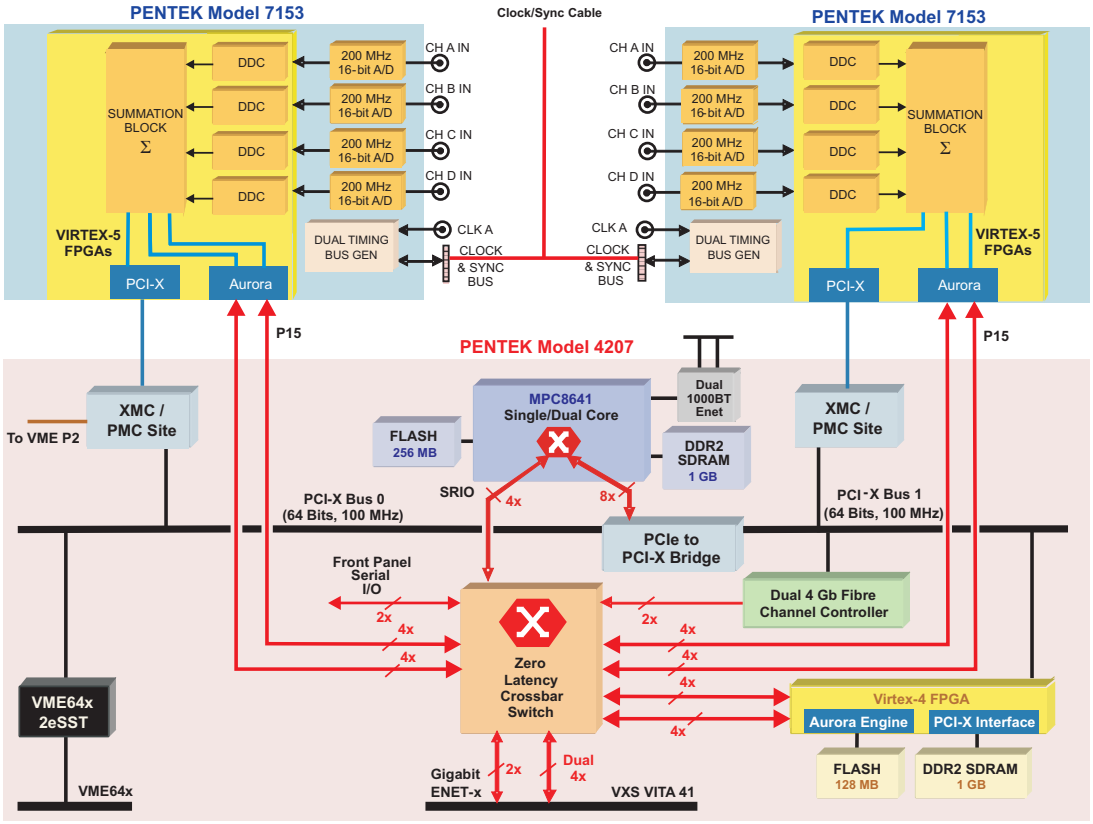
For more information please go to: pentek.com/go/pipe7153. ❑



Application: 8-Channel Aurora Beamforming System

Download a 10-minute Peoduct Techcast demonstration that describes this application in more detail.

DOWNLOAD



Two Model 7153 Beamformer PMC/XMC modules are installed on the Model 4207 I/O Processor board. The eight signals to be beamformed are connected to the eight analog inputs of these modules. Joining the two 7153 modules is a clock/sync cable that synchronizes the DDCs and guarantees synchronous sampling across all eight channels.

Signals from the first four channels of the left 7153 module are summed in the left summation block; signals from the second four channels of the right 7153 are summed in the right summation block. The summation output from the left XMC module is delivered using the Aurora 4x link into one port of the crossbar switch. Each red 4x link is capable of data rates up to 1.25 GBytes/sec. The left 4-channel sum is connected through the crossbar switch and delivered into the summation input port of the right XMC module.

The Aurora summation from the left four channels is combined with the right four channels and then delivered to the crossbar switch from the right summation output port. The eight-channel combined sum is delivered through the crossbar switch into the Aurora engine implemented in the Virtex-4 FPGA of the Model 4207 processor board.

This Aurora engine decodes the stream and delivers it to a designated block in the DDR2 memory attached to the FPGA. The PCI-X interface in this FPGA presents the SDRAM memory as a mapped resource appearing on the processor PCI-X bus 1. The Power PC reads the data from the FPGA DDR2 memory across the PCI-X bus, creates the beamformed pattern display and presents it via its front panel gigabit Ethernet port to an attached PC for display.

This concept can be expanded to create a 16-channel beamforming system by daisy-chaining a second Model 4207 with another two Model 7153 modules installed. The beamformed data from the first system is moved to the next one over the VXS backplane of the 4207's.

A 10-minute presentation with more details of this system narrated by Rodger Hosking is available on Pentek's website. You can download the 8-Channel Aurora Beamforming System demo from this link: pentek.com/go/pipebeamformer. ❑