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**Pentek, Inc.**
One Park Way, Upper Saddle River, NJ 07458
Tel: (201) 818-5900 • Fax: (201) 818-5904
email: pipeline@pentek.com
http://www.pentek.com



# XMC: A Mezzanine for all Seasons

Mezzanine cards have played an essential role in real-time embedded systems since the earliest days of single board computers and standard backplanes. They offer a wealth of specialized signal interfaces, data converters, connectors, and transceivers along with dedicated engines for protocols, networks and signal processing. Standardization of the mechanical and electrical characteristics of these mezzanine cards enables system integrators to deliver specialized, high-performance embedded applications by judiciously combining open-architecture I/O products with processor boards.

## The PMC Mezzanine

Making its debut in 1994 as IEEE standard P1386.1, the PMC (PCI mezzanine card) was successfully adopted for both commercial and government electronic systems. Based on the mechanical specifications for the P1386 CMC (common mezzanine card), it included three 64-pin connectors to support a PCI bus interconnect to the carrier board, as well as a fourth 64-pin connector for user I/O.

During the next decade, important extensions to the PMC standard included conduction-cooled versions for severe environments, pin definitions for P4 I/O, and the adoption of the Processor PMC (PrPMC) specification.

When a proposal for standardizing gigabit serial switched fabrics shook the embedded computing community in 2002 as part of the VME Renaissance, a natural extension of that technology to PMC modules was inevitable. Defined under VITA 42, the XMC specification extends the PMC card by adding new connectors to support gigabit serial interfaces plus a growing list of alternative I/O standards.

## VITA 42: The XMC Mezzanine

The hallmark of any successful standard is that it continues to evolve with technology, and none offers a better example than XMC. Figure 1 shows the current listing and status of the many standards defining XMC under VITA 42.

VITA 42.0 is the base specification that includes general information, reference and inheritance documentation, dimensional specifications, connectors, pin numbering and primary allocation of pairing and grouping of pin functions. This document is still designated as a draft document, but it was released for trial use for an 18-month period ending March 2007. Recommendations gathered during the trial will be used to produce a final released specification.

XMCs can be single- or double-wide modules that use a pin-socket connector with 114 pins arranged in a 6 x 19 array. A single width XMC can have one or two connectors with pin functions as shown in Figure 2. A double width XMC can have up to four connectors.

To support gigabit serial interfaces, notice that both P15 and P16 connectors define 10 full-duplex differential pair lines. The VITA 42.0 base specification does not dictate signal types, data rates, protocols, voltage levels or grouping for these signals. Instead, it wisely leaves that up to the several sub-specifications that follow, ➤

| VITA Doc | Description | Status |
|---|---|---|
| 42.0 | Base Specification, general info, connectors, mechanical, etc. | Draft released |
| 42.1 | Parallel RapidIO | Approved |
| 42.2 | Serial RapidIO | Approved |
| 42.3 | PCI Express | Approved |
| 42.4 | HyperTransport | Draft |
| 42.5 | Aurora | Planned |
| 42.10 | General-purpose I/O | Draft |

*Figure 1. XMC VITA 42 Standards Status*

### In This Issue



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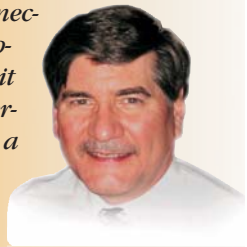

*Rodger Hosking, Pentek Vice President and Cofounder*



### Technical Resources Recently Updated!

Download the new 6th edition of the *Digital Receiver Handbook:*
pentek.com/go/pipedrhb

Download the new 3rd Edition of *FPGAs for Software Radio Handbook:*
pentek.com/go/pipefpgahb

Download the new 2nd Edition of *Critical Techniques for High-Speed A/D Converters in Real-Time Systems Handbook:*
pentek.com/go/pipehshb

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➤ allowing XMCs to evolve as new standards emerge.

In fact, contrary to the fundamental mission of supporting serial interfaces, the first sub-specification, VITA 42.1, defines these same pins for Parallel RapidIO. While VITA 42.1 is approved and fielded, few vendors have embraced this standard and have instead opted for the more popular serial protocols.

VITA 42.2, 42.3 and 42.4 define true serial switch fabric protocols for Serial RapidIO, PCI Express and Hypertransport, respectively. The first two are already approved and beginning to appear as mainstream choices for a widening range of board and silicon vendors.

In fact, two major silicon vendors have announced new processors well-suited for embedded computing applications that incorporate serial interfaces and protocol engines right on the chip. Texas Instruments offers the TMS320C6455 DSP processor with Serial RapidIO, while the Freescale MPC8641 includes both PCI Express and Serial RapidIO interfaces. These native interfaces simplify carrier board design and significantly boost peripheral I/O transfer rates by taking advantage of XMC modules.

VITA 42.5 defines the popular Xilinx Aurora protocol for use in XMC. This lightweight link layer protocol is quite attractive for XMC modules because many XMCs only need to move data from a dedicated source (like an A/D converter) to a dedicated destination (like memory on a processor board). The extra protocol layers necessary to support a full switched network and routing can significantly reduce the payload data rate and add complexity and cost at both ends of the link. This standard is still in the definition phase.

As shown in Figure 2, most of the pins on P15 are reserved for serial links, power and other functions, but P16 has a wealth of user-defined pins now being addressed by the VITA 42.10 General Purpose I/O draft specification. It offers a standardized way of implementing interfaces for popular system I/O including Ethernet, USB ports, RS-232, RS-485, Serial ATA, Fibre Channel, and SAS (Serial Attached SCSI). The clear benefit here is that by following these definitions, XMC and carrier board designers can achieve a much wider range of inter-operability, the essential goal of industry standards.

**P15 Primary XMC Connector**

- 10 differential pairs each direction
- JTAG
- System Management
- Auxiliary
- 3.3 V Power:
  - Main: 4 pins, 1 A/pin, 13.2 W
  - Auxiliary: 1 pin, for system management
- Variable Power
  - 8 pins, 1 A/pin
  - 5 V (40 W max) or 12 V (96 W max)
  - Modules must accept 5 V or 12 V
  - Carriers may provide 5 V or 12 V

**P16: Secondary XMC Connector**

- 10 more differential pairs each direction
- High-speed or single-ended user I/O
- Extensions of gigabit serial fabrics

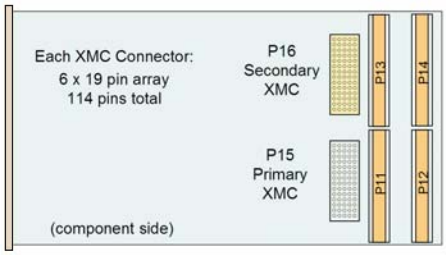


*Figure 2. VITA 42.0 Single-width PMC/XMC Connector Definition*

## FPGAs: The Vital Ingredient

In recent years, FPGAs (field programmable gate arrays) have permeated mezzanine card architectures for reasons entirely incidental to XMC, and yet today FPGAs represent the single most significant catalyst for XMC adoption.

FPGAs offer a collection of resources ideally suited for peripheral I/O functions. FPGAs may be configured to implement numerous electrical interface standards as well as a variety of protocol engines. By reconfiguring its FPGA, not only can a single I/O product replace several legacy products, it can also adapt to future standards and protocols as well. This forestalls product obsolescence, both at the board level and at the deployed system level.

Another reason FPGAs find their way onto mezzanine cards is their unmatched ability to implement real-time signal processing and high-level local control. FPGAs deal effectively with the very high front-end data rates for A/D and D/A converters, network interfaces, sensor arrays and high-speed data channels by mustering a troop of high-performance hardware resources, configured to match the specific task at hand. For more sophisticated front-end processing, most FPGAs now feature DSP engines with built-in hardware multipliers to tackle the toughest algorithms with ease. Arrays of these engines can be deployed in parallel, completely surpassing the capabilities of general-purpose programmable RISC or DSP processors that must execute serial instructions.

By performing these types of intensive protocol, formatting, decoding and DSP functions on the mezzanine, the workload for the processor on the carrier board can be significantly reduced. This may lead to fewer processors or fewer processor boards in the system, for considerable savings in system cost and size.

With integrated microcontrollers, FPGAs can now implement a complete system-on-a-chip. Executing a program coded into the FPGA or from an external FLASH, these microcontrollers can perform complex processing tasks to implement real-time control functions for adaptive processing, signal classification, target identification and object recognition. Having intimate contact with the surrounding DSP hardware, FPGA microcontrollers can modify real-time operating parameters and modes very efficiently—often well beyond the scope of larger systems with more loosely coupled elements.

With such widespread use of FPGAs on mezzanines, the emergence of built-in gigabit serial interfaces on these devices was a major windfall for XMC. During the last five years, both Xilinx and Altera have invested heavily in developing this technology, and have now produced three ➤

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➤ generations of FPGAs with gigabit serial interfaces as shown in Figure 3.

Xilinx offers their RocketIO GTP transceivers on the latest Virtex-5 LXT family devices with bit rates up to 3.125 GHz. Altera offers their Stratix-II GX multigigabit transceivers with bit rates up to 6.375 GHz. Both vendors support these physical interfaces with SERDES (serializer/deserializer) hardware engines that perform serial/parallel conversion so that data and clock are combined in the signaling on each differential pair over the external serial channel.

Protocol engines for specific standards can be configured using FPGA logic so that FPGAs can adapt to different protocols as required. They interface to the SERDES and correctly process protocol-specific packets, header information, control functions, error detection and correction, and payload data format. The strategy makes FPGA-based XMC modules truly "fabric agnostic" and allows one hardware design to be deployed in several different fabric environments.

The new Xilinx Virtex-5 LXT devices advance the technology even further by including a built-in PCI Express end point engine. This saves FPGA resources for other tasks and offers a standardized internal interface for sending and receiving data.

| | Virtex-II Pro XC2VP50 | Virtex-4 FX XC4VFX100 | Virtex-5 LXT XC5VLX220T |
|---|---|---|---|
| Logic Cells | 53,136 | 94,896 | 221,184 |
| Block RAM (bits) | 4,176k | 6,768k | 7,632 |
| Max I/O User Pins | 852 | 768 | 680 |
| Multipliers | 232 | 160 | 128 |
| 405 Power PCs | 2 | 2 | - |
| Gbit ENET Ports | - | 4 | 4 |
| Rocket I/O Serial | 16 | 20 | 16 |
| PCI Express Ports | - | - | 1 |

*Figure 3. Serial Interfaces on Three Generations of Xilinx FPGAs*

## Putting FPGAs to Work for XMC

Figure 4 shows an XMC product for software radio applications that takes maximum advantage of FPGA resources. The Xilinx Virtex-4 SX55 offers a generous 512 DSP slices, highest in the Virtex 4 family, to maximize performance of algorithms critical to software radio like digital down-conversion, analysis, energy detection, and demodulation. It also provides interfaces to the many A/D and D/A converters, timing and memory resources.

In addition, the Virtex-4 FX-100 is harnessed for its control and I/O capabilities. A nine-channel DMA controller and a complete PCI interface ensure efficient data transfers to and from the host PCI interface. The RocketIO gigabit serial interfaces are connected directly to the pins of the XMC connection, per VITA 42.0. By installing the appropriate protocol engine inside the FX100, any of the popular serial standards can be supported. Commercial intellectual property (IP) cores for both PCI Express and Serial RapidIO are now available from Xilinx, Altera, and third party sources to save development time.

Architectures like the one in Figure 4 illustrate the central role of FPGAs in PMC and XMC modules, by saving hundreds of discrete devices for improved density and function. The ability to add custom signal processing algorithms, control functions and protocol engines helps broaden the market space and extend product lifecycles. As FPGAs acquire more functions, future XMC offerings will surely benefit, ensuring them a secure and long-lasting role in high-performance embedded systems.

The claim that FPGAs have been the single most important factor in XMC adoption should now be justified. Because of FPGAs, the only incremental hardware cost to the PMC card vendor is adding copper traces from the FPGA gigabit serial interface pins to the pads of the XMC connector. The larger investments in software, drivers and FPGA development can be tuned to the market demands as appropriate. Now that XMC compliant hardware is proliferating, these investments are already being made. To view Pentek's GateFlow FPGA resources, go to:

pentek.com/go/pipegateflow ❑

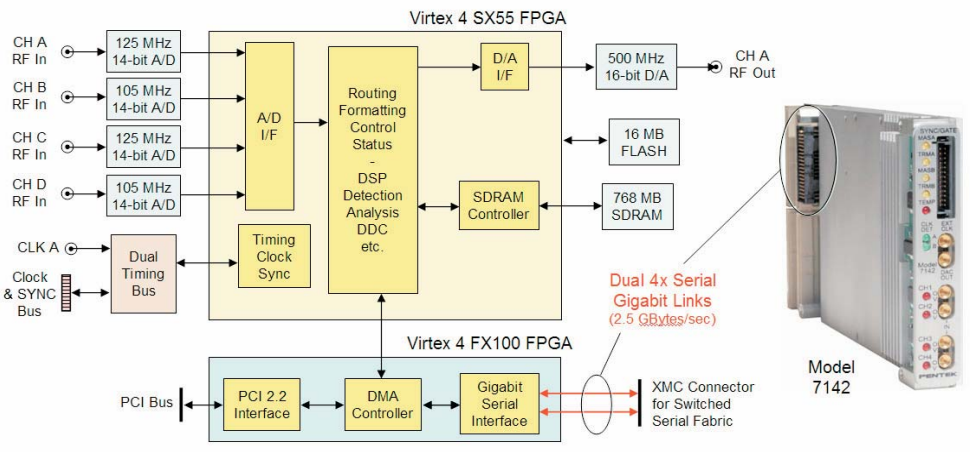



*Figure 4. Model 7142 XMC Module uses Virtex-4 FPGA for Gigabit Serial Interface*

# Pentek PMC/XMC Software Radio Transceivers

## Model 7140 Transceiver

For more information on the 7140 click here: pentek.com/go/pipe7140

### Overview

Model 7140 is a software radio transceiver suitable for connection to HF or IF ports of a communications system and capable of bandwidths to 40 MHz and above.

The front end accepts two full scale analog HF or IF inputs at +4 dBm into 50 ohms with transformer coupling into 14-bit 105 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

The 7140 includes a quad DDC and a digital upconverter with two 500 MHz D/A converters.

### Features

- Complete software radio transceiver solution
- Four digital downconverters
- Two 105 MHz 14-bit A/D converters
- Upconverter with two 500 MHz 16-bit D/As
- Xilinx Virtex-II Pro FPGA
- Optional factory-installed IP cores eliminate FPGA development tasks
- XMC I/O for high-speed data streaming
- Ruggedized and conduction-cooled versions available
- Also available: Model 7640 PCI; Models 7340 3U and Model 7240 6U cPCI boards

## Model 7142 Transceiver

For more information on the 7142 click here: pentek.com/go/pipe7142

### Overview

Model 7142 is a multichannel, high-speed data converter suitable for connection to HF or IF ports of a communications system. It includes four A/Ds and one upconverter and D/A converter capable of bandwidths to 40 MHz and above.

The front end accepts four full scale analog HF or IF inputs at +10 dBm into 50 ohms with transformer coupling into 14-bit 125 MHz A/D converters.

The digital outputs are delivered into a Virtex-4 FPGA for signal processing or for routing to other module resources.

A digital upconverter and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

### Features

- Complete software radio transceiver solution
- Four 125 MHz 14-bit A/D converters
- Upconverter with 500 MHz 16-bit D/A
- 768 MB of DDR2 SDRAM
- Two Xilinx Virtex-4 FPGAs
- Optional factory-installed IP cores eliminate FPGA development tasks
- XMC I/O for high-speed data streaming
- Ruggedized and conduction-cooled versions available
- Also available: Model 7642 PCI; Models 7342 3U and Model 7242 6U cPCI boards

## Model 7141-703 Ruggedized Transceiver

For more information on the 7141-703 click here: pentek.com/go/pipe7141-703

### Overview

Model 7141-703 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters capable of bandwidths to 40 MHz and above.

The Model 7141-703 is offered as a fully conduction-cooled/ruggedized board meeting Pentek's L3 ruggedization level (option 703).

The front end accepts two full scale analog HF or IF inputs at +10 dBm into 50 ohms with transformer coupling into 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

### Features

- Complete software radio transceiver solution
- Four digital downconverters
- Two 125 MHz 14-bit A/D converters
- Upconverter with two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- XMC I/O for high-speed data streaming
- Dual timing buses for independent input and output clock rates
- Optional factory-installed IP cores eliminate FPGA development tasks

Product Focus

SystemFlow

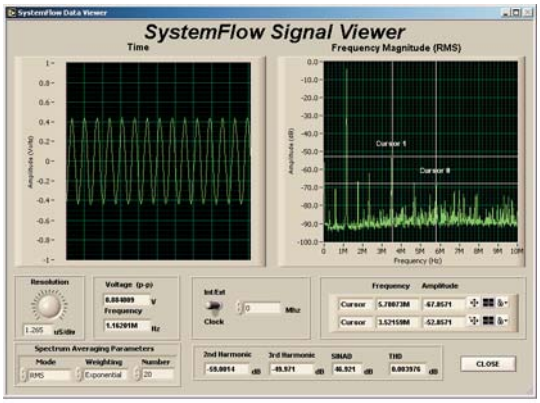
# Pentek SystemFlow Software for Real-Time Recording Systems

## Latest Release Offers Many New Features

### Features

- Ready-to-use record/playback software
- Development tool suite with APIs and source code
- New Signal Viewer offers enhanced analysis functions
- New, easy-to-use File Manager for critical data management
- RAID storage up to 6 terabytes and higher
- Now supports both Windows® and Linux® platforms


*SystemFlow File Manager*




*SystemFlow Signal Viewer*

The Model 4990 SystemFlow® provides a rich set of features for controlling the data acquisition and recording functions and ensures a consistent look and feel for developers across all Pentek RTS systems.

Pentek RTS systems are flexible and deployable real-time recording systems for acquiring, processing and analyzing signals. They are ideal for high-performance radar, wireless, military communications, SIGINT, telecom and satcom applications.

What sets the Pentek RTS recording systems apart from the rest is the well-engineered, fully-integrated SystemFlow software suite, optimized for each system. This wide range of tools, from high-level APIs to low-level source code, provides the extra flexibility engineers need to tackle even the toughest applications.

New to the SystemFlow software are a File Manager that simplifies file and data management and a Signal Viewer with enhanced display and analysis capabilities. In addition, the RTS systems now support both RAID and JBOD Fibre Channel disk arrays, thereby boosting recording capacity to 6 terabytes and higher. The new graphical user interface is written in Visual Basic for Windows PCs and Java for Linux. Complete APIs and source code, for both the host and the target, boost productivity for custom development of data acquisition, recording and display functions.

### File Manager Simplifies Data Management

The new File Manager saves each recording session as an individual file. Critical parameters including time stamping, channel identifiers, file length, data format, and user fields are automatically stored in each file header.

### Enhanced Signal Viewing, Analysis and Storage

The user interface presents a virtual instrument control panel to simplify all system operations with push button controls and hardware parameter entry windows. The enhanced Signal Viewer provides simultaneous viewing of live or recorded signals in both time and frequency domains. Also added are essential signal-analysis tools for measuring parameters such as SINAD, harmonics and THD. Spectral averaging is also available, so that the user can detect weak signals and explore points of interest.

Additional functions include channel allocation for the connected Fibre Channel RAID or JBOD disk arrays, continuous display of recording, and file transfers to the host for processing, analysis and archiving. The newly supported RAID arrays can now stream data at the same rates as JBODs, but with the additional advantages of lower cost, inherent fault tolerance, and raising storage capacities from around 0.5 to 6 terabytes or more.

### Real-Time Acquisition and Host System Development

The acquisition hardware and Fibre Channel disks are controlled by an application written in eCos, a license-free real-time operating system. This application can be easily customized to configure the RTS system interfaces and operation to fit specific applications.

### Flexible and Deployable RTS Recording Systems

Currently, three Pentek RTS systems are available: the RTS 2501 a 105 MHz Real-Time Recording System with Wideband Receiver and FPGA Processing; the RTS 2503 a 215 MHz Recording System with FPGA Processing; and the RTS 2504 105 MHz Real-Time Recording and Playback System with Multiband Transceiver and FPGA Processing. Each is housed in a portable 6U VMEbus enclosure. Future systems under development will be compatible with the SystemFlow software. ❑

For more information on SystemFlow, click here: pentek.com/go/pipe4990

For more information on RTS 2501, click here: pentek.com/go/pipe2501

For more information on RTS 2503, click here: pentek.com/go/pipe2503

For more information on RTS 2504, click here: pentek.com/go/pipe2504