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Jefferson Lab Advances the State of Science in Nuclear Physics

Jefferson Lab is a nuclear physics research facility operated for the Office of Science of the US Department of Energy by the Southeastern Universities Research Association (SURA). An international community of about 2,000 scientists conducts research to increase the understanding of the structure of matter and the forces that hold the atom's nucleus together. By smashing electrons into atoms in JLab's Continuous Electron Beam Accelerator Facility (CEBAF) the scientists have already mapped the structure of the proton to an unprecedented level.

Superconducting electron accelerating technology makes Jefferson Lab unique. The electron beam recirculates up to five times through two linear accelerators to reach energies up to 6 billion electron volts (GeV). The beam is then split for simultaneous use in three experiment rooms.

To realize new research opportunities that are beyond Jefferson Lab's present capabilities, the accelerator facility and its experimental equipment are now in the process of upgrading to new components that will double the energy of the electrons to 12 GeV. The upgrade includes adding accelerating modules, constructing a new experimental room and upgrading the present research equipment. An aerial view of this super- conducting 7/8-mile racetrack is shown in Figure 1.

Accelerator Physics

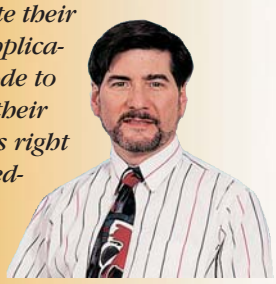
Inside the accelerator, a stream of electrons races around the racetrack. A billion times per second, magnets steer and focus the electrons into a beam the width of a human hair. The accelerator is controlled and monitored by more than one hundred computers. Together, they track, manage and respond to more than 240,000 simultaneous signals and 40,000 hardware control points. Eventually, the electron beam is funneled into three experiment halls where the high-speed particles are slammed into target materials.

Scientists from around the world use the electron beam to perform experiments which refine theories about how "quarks", the small particles that combine to form protons and neutrons, behave in the nucleus. By measuring the properties of scattered particles after the electron beam collides with a target nucleus, scientists learn how quarks and the forces that hold them together interact and form the ordinary matter in the universe. ➤

Figure 1. Aerial View of the Jefferson Lab Facility in Newport News, VA, USA (Courtesy of Jefferson Lab)

In This Issue

"Just like our other RTS systems, the RTS 2503 saves valuable development time and effort. Engineers can take the development platform and easily integrate their own application code to keep their projects right on schedule."



Rodger Hosking, Pentek Vice President and Cofounder

Technical Resources

Download the new, 5th edition of the *Digital Receiver Handbook:*
pentek.com/go/pipedrhb

Download the new *SCA Handbook:*
pentek.com/go/pipescahb

Download the *High-Speed A/D Boards and Systems Brochure:*
pentek.com/go/pipehsbro

Download the *Critical Techniques for High-Speed A/D Converters in Real-Time Systems Handbook:*
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Jefferson Lab Upgrade

Doubling the energy of Jefferson Lab's electron beam to 12 GeV will enable scientists to search systematically for glue-rich particles. In addition, the upgrade will allow in-depth study of the proton, the balance of forces within the nucleus and quark matter in the first second of the universe.

Shown in Figure 2 is a conceptual diagram of the existing recirculating linear accelerator and the planned mechanical upgrades to it. We will focus our attention on the new front-end electronic instrumentation modules that are presently under design at JLab. These modules receive and record signals from the different types of particle detectors planned for this upgrade. A cutaway view of a particle detector is shown in Figure 3.

The new experimental hall includes approximately 18,000 Flash* A/D Converter channels (ADC) and 4,300 Time-to-Digital Converter channels (TDC). These ADC and TDC channels are connected to the readout electronic modules that reside in a standard VME card enclosure. The card enclosures are known as "crates" and the new detectors proposed for the experimental hall will need approximately 70 to 80 crates. The crates provide power to the individual modules and establish a high-speed data acquisition path using defined standards for data bus protocol.

Data acquisition electronics for nuclear physics applications have taken advantage of a number of standards that define the mechanical and electrical specifications for instrumentation modules and powered card enclosures. Some of these standards date back to the late 1970's and are, for all practical purposes, obsolete. New instrumentation modules have been designed by Jefferson Lab and the industry to take advantage of higher performance standards such as VME, VME64x and VXS which are all standards created and supported by VITA, the VME International Trade Association. The new instrumentation modules will replace the aging and obsolete modules that use the older data bus standards.

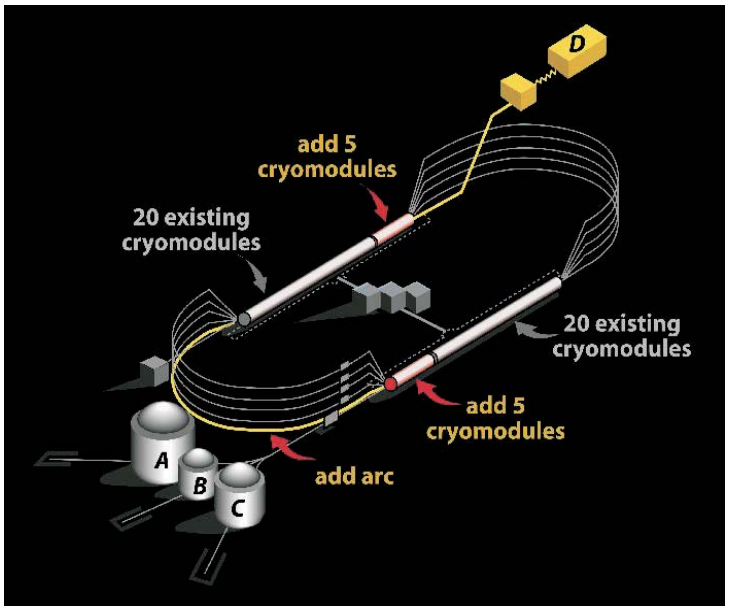


Figure 2. The Jefferson Lab Recirculating Linear Accelerator with the Planned Upgrades (Courtesy of Jefferson Lab)

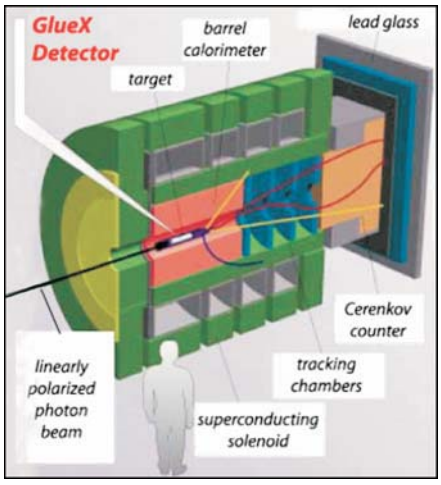


Figure 3. Cutaway View of a Particle Detector (Courtesy of Jefferson Lab)

Pipelined Data Acquisition

The new experimental apparatus, constructed with various particle detectors, requires that the front-end electronic modules support a high trigger rate. Digitization of the input signals for analog pulse information and timing must be buffered for several microseconds, while the overall trigger is formed from all the detector sections.

Since multiple signals could not be digitized and stored in the front end modules, the older instrumentation standards did not allow for pipelined data acquisition techniques. The overall data acquisition trigger rate was limited by these non-pipelined modules and remained well below 3 kHz.

With pipeline design techniques and improvements in FPGAs, the digitization process can be increased at the front end and the information can be stored until the trigger processing is completed. The design goals for the new experiment are a 200 kHz trigger rate with approximately 5 kbytes of event data. This corresponds to an overall data acquisition rate of 1 Gigabyte per second.

Creating the Trigger

The instrumentation modules connected to the detector sections that form the trigger, must transfer information from each module in the crate to a central collection module. Each module produces a digital sum of the signals that are present on each input channel. The sum signal from each module is collected and added to the other modules in the crate. The crate sum is the first level of trigger processing for the overall experiment trigger. All the crates that collect signals from detector sections responsible for the trigger are ultimately summed again to create the "Physics Event" trigger signal. This final trigger signal is distributed to all the front-end instrumentation modules and initiates the readout of stored data in the modules. ➤

* Flash ADC: Also called the *parallel* A/D converter, this circuit is the simplest of ADCs. It consists of a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.

Jefferson Lab Advances the State of Science in Nuclear Physics

Designing with VXS

The VITA 41 VXS specification provides the capability for connecting each module in a data acquisition crate with a central collection module. The VXS standard defines high speed, multigigabit serial connections from each VME64x module slots to a central collection module. The Electronics and Data Acquisition groups at Jefferson Lab have embarked on a design that takes advantage of the high speed backplane designs that the VXS standard has created. This standard allows JLab to use legacy VME/VME64x modules in a VXS crate, to develop modules that will be used in the final design of the data acquisition system for the detector systems constructed for the 12 GeV upgrade.

Commercial crate and backplane designs to support the VXS specification have been researched at JLab. To support the plans for designing front end electronic modules and testing vendor backplanes, JLab purchased the Pentek Model 6822 Dual Channel 215 MHz, 12-bit ADC VXS board.

As shown in Figure 4, it provides the hardware to drive the VITA 41 backplane. The Pentek Model 6822 is unique in that it also allows the user to develop algorithms that can be loaded to the on-board FPGA for signal processing. The preprocessed data is then transferred through the VXS backplane to the central collection module. The 6822 will be used to test data processing routines, and to verify the central collection module development and design effort.

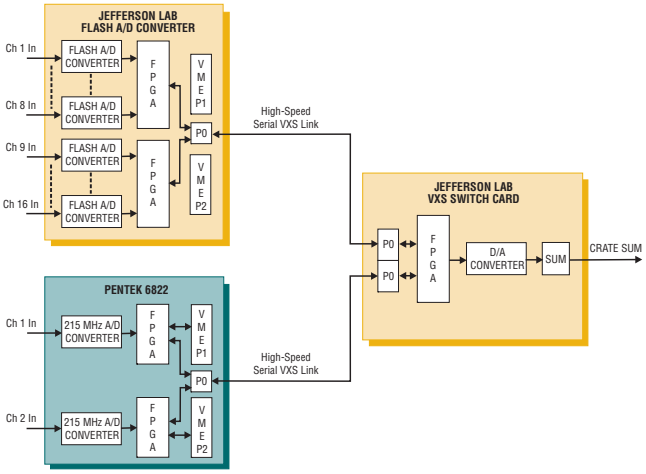


Figure 4. The Pentek Model 6822 as Used in the JLab Upgrade Tests

Commercialization

Through its technology commercialization programs, SURA is collaborating with other national labs, universities and the private sector to find practical applications for these technologies. Exciting examples include medical imaging for early detection of cancer and security scanning devices.

Through the active pursuit of applying research to meet the needs of the commercial marketplace, SURA's technology transfer program seeks to positively impact the economy and improve people's lives in ways that have never been considered before.

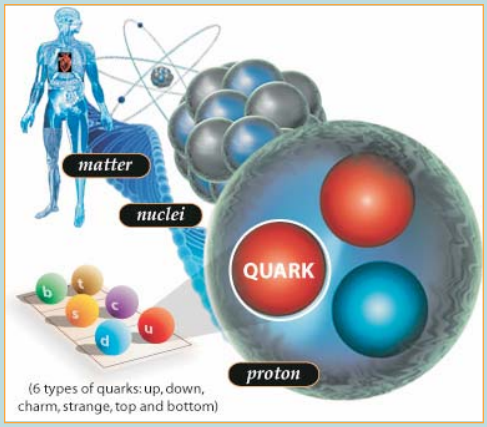
Also See:

- *Pentek DSPs Keep the ELETTRA Beam Stable and Bright,* The Pentek Pipeline Vol. 10, No. 3, Fall 2001.
- *VXS: Switched Serial Gigabit Fabric,* The Pentek Pipeline Vol. 12 No. 2, Summer 2003.
- *High-Speed A/Ds for Wideband Signal Processing Applications Reach 2 GHz*, The Pentek Pipeline, Vol. 14 No. 2, Summer 2005. ❑

Quarks and the Strong Force

From the stars overhead to the atoms in our own DNA, all matter is composed of fundamental particles — particles that cannot be divided into smaller parts. Quarks are among the few fundamental particles in the universe. There are six types of quarks: up, down, charm, strange, top, and bottom. The lightest quarks, called up and down, are the most common.

Quarks are bound to each other by the strongest force in the universe. Called simply the "strong force", this enormous force binds them so tightly that one quark cannot exist by itself. Glued by the strong force, quarks are the building blocks of matter as we know it. Understanding quarks and the strong force is fundamental to the universe, our world, and us.



Quarks and Gluons

Quarks stick together and won't come apart. When pried even one proton's width apart, quarks experience ten tons of force pulling them together. Quarks are so small that we have not been able to measure their size; they take up less than one billionth of the space inside the proton, and make up only a few percent of its mass.

So, what takes up the rest of the space and gives protons the rest of their mass? The strong force itself, via carrier particles called "gluons". This binding glue surrounds and connects the quarks and generates 98% of the universe's visible mass. Scientists have discovered that nature builds particles in hundreds of ways from these tiny quarks and forceful gluons.

Product Focus

Model 6826

Blazingly Fast Data-Capture and Processing Board with 2 GHz Sampling Rate

The Model 6826 6U VME/VXS board features single- or dual-channel data acquisition at two gigasamples per second with 10-bit resolution using the new Atmel AT84AS008 A/Ds. It includes a high-performance Virtex II-Pro FPGA for signal processing and delivers digital output samples over FPDP connectors utilizing FPDP or FPDP II standards. The 6826 digitizes signal bandwidths to nearly 900 MHz for applications such as wideband radar and communication signals.

Features

- Dual Atmel AT84AS008 10-bit A/Ds
- User-configurable Xilinx Virtex-II Pro FPGA with 11 million gates includes two PowerPC cores to create complete application engines
- Pentek GateFlow® FPGA Resources: FPGA Design Kit, IP cores and preinstalled cores
- Pentek ReadyFlow® Board Support Libraries for quick board startup and operation
- Multiple high-speed FPDP and VXS I/O
- Multiboard synchronization
- Ruggedized and conduction-cooled versions

The Model 6826 is shown here equipped with option -224, two additional FPDP ports available on a second slot front panel.

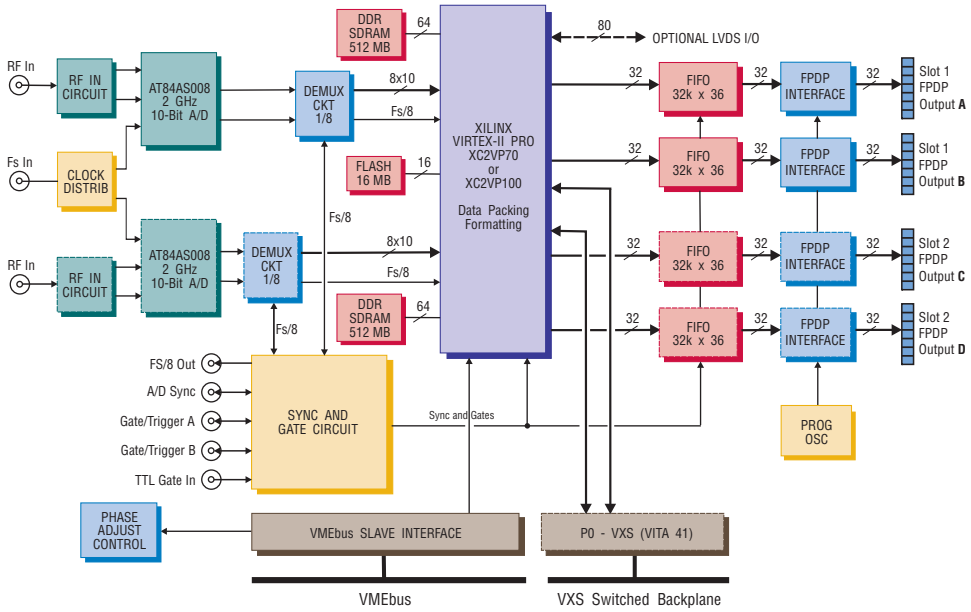
GateFlow

ReadyFlow Board Support Libraries

On-Board Signal Processing

With a density equivalent of more than 11 million gates, the Xilinx XC2VP100 Virtex-II Pro FPGA offers a powerful signal-processing resource for the stream of data from the A/D converters. This stream is first demultiplexed by a factor of eight to produce 80-bit words at a reduced data rate of 250 MHz for successful delivery to the FPGA. The FPGA then performs various functions on the data including gating, triggering, formatting, memory transfers, and delivery to FPDP and VME interfaces. It also handles the switched serial fabric VXS interface using the on-chip RocketIO gigabit serial transceivers.

Since most of the logic and DSP resources are available, developers can implement custom signal-processing algorithms to process data in real time. To simplify FPGA development tasks, Pentek offers its GateFlow FPGA Resources which include the GateFlow FPGA Design Kit, GateFlow IP Core Libraries, and GateFlow Factory Installed Cores. Pentek also offers the ReadyFlow Libraries that allow the user to control the Model 6826 across the backplane from SBC and DSP boards through high-level C-callable commands.



Extensive Memory Supports Transient Capture and Buffering

Dual 64-bit high-speed DDR SDRAMs provide a total of up to 1 GB of memory to store raw data in transient-capture mode. The memory can also be used as an elastic buffer for storing burst signals like radar pulses in real time for subsequent delivery to the I/O interfaces at a lower continuous rate. Custom FPGA configurations can take advantage of this large memory for more complex applications. Flash memory of 16 MB allows boot code storage for the two IBM 405 PowerPC microcontroller cores within the FPGA.

Output Interface Options

To support high-bandwidth data capture, the board includes several high-speed I/O channels to move data off-board for storage or processing. Two or four channels of FPDP-II data ports operating at up to 400 MB/second each deliver data to other VME cards. In addition, the board offers two serial switched-fabric VXS connections, each running full-duplex at 1.25 GB/second to support the new Xilinx Aurora, Serial RapidIO and PCI Express protocols. LVDS I/O is also available through P2 or on a second slot front panel.

For more information, click here: **www.pentek.com/go/pipe6826.** ❑

Product Focus

System RTS 2503

New Development Platform Handles Wideband Real-Time Recording

Features

- Dual-channel 12-bit, 215 MHz A/Ds
- 1 GHz G4 PowerPC
- Multiple Xilinx Virtex-II and Virtex-II PRO FPGAs
- Real-time recording to RAID or JBOD arrays up to 160 MBytes/sec
- SystemFlow™ API and development Libraries
- Highly scalable platform from 1 to 20 A/D channels
- Custom FPGA algorithm development
- Ethernet link to Linux or Windows
- High-speed interfaces available: RACE++, Gigabit Ethernet, VXS

SystemFlow API and Development Libraries

GateFlow

ReadyFlow Board Support Libraries

The Pentek RTS 2503 is a scalable real-time platform for acquiring, processing, analyzing and recording wideband signals. Integrating recently-introduced A/D converters, FPGAs and signal processors, this system allows the design engineer to take advantage of the latest technology for signal processing.

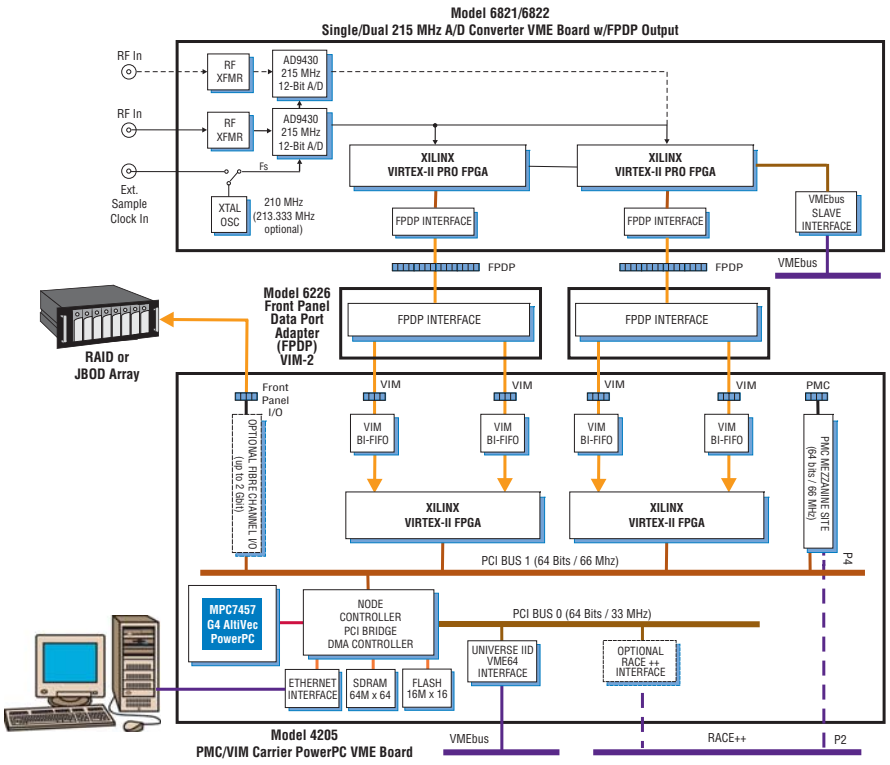
Scalable from 1 to 20 channels in a single 6U VMEbus chassis, the RTS 2503 serves equally well as a development platform for advanced research projects and proof-of-concept prototypes, or as a cost-effective strategy to deploying high-performance, multichannel embedded systems.

The RTS 2503 is equipped with Model 4990 SystemFlow API and Development Libraries for an out-of-the-box, GUI-enabled recording system. This software can also be used as a system example for building new applications.

Inside the RTS 2503

System RTS 2503 accepts signals through a Model 6822 Dual-Channel 12-bit D/A Converter sampling at a maximum frequency of 215 MHz. The digitized outputs are passed through two Xilinx Virtex-II Pro FPGAs for signal processing and data handling. A Pentek Model 4205 I/O Processor, featuring a 1 GHz MPC7457 G4 PowerPC and two Xilinx Virtex-II Pro FPGAs, manages data transfer tasks and performs signal processing or formatting functions.

Built-in Fibre Channel and optional RACE++ interfaces provide excellent I/O connectivity without sacrificing any of the board's mezzanine sites. Standard RS-232 and 100 BaseT Ethernet ports allow the PowerPC to communicate with a wide range of host workstations for control and software development applications.



SystemFlow API and Libraries

SystemFlow software has a modular design that includes API libraries for the target board as well as user-control libraries for the host PC. Windows DLL calls are written in Visual C++ and a GUI is provided as a front-end PC host system. The PC host front end communicates over Ethernet with the royalty-free eCos real-time operating system running on the system's G4 PowerPC board, which executes real-time application code.

API libraries for both host and target include full source code, allowing developers to easily modify both the platform front end and target code to meet their needs. The software package also includes a data viewer, written in LabView, that shows display plots of collected data in either time or frequency domain. Developers can use the viewer to preview data before storage or to review stored data.

For more information, click here: **www.pentek.com/go/pipe2503.** ❑