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## BAE SYSTEMS Develops Zero-Visibility Landing Guidance System

**B**AE SYSTEMS offers its customers a global capability in air, sea, land and space.

In the air, they take a leading role in joint programs for both military and commercial aircraft in partnership with the world's leading aircraft manufacturers.

For the world's navies, they offer an extensive ship design capability and build various ships, missiles, and communications systems.

On land, their systems include radar, communications networks and guided weapons.

In space, they offer satellite systems for civil and defense navigation and for communications and environmental monitoring.

### Autonomous Landing Guidance

One of BAE SYSTEMS' projects involves the development of an Autonomous Landing Guidance (ALG™) system. ALG is basically a "precision approach system" which enables pilots to fly aircraft and land successfully in conditions of zero visibility. Field tests of the ALG were conducted out of Edwards Air Force Base, CA, where test pilots successfully landed a C-130 Hercules transport aircraft in actual visibility and ceiling conditions below the Air Force's minimum allowed levels.

Test pilots also used the system to land in simulated zero-visibility conditions. To simulate zero visibility, the aircraft's cockpit windows were covered with a translucent orange plastic lining. During flight, pilots wore a blue visor that prevented them from seeing through the orange plastic, but allowed them to see inside the cockpit, so they could land the aircraft using the ALG system. This vision-restricting device was very effective in blocking the view outside the cockpit. As described by one of the test pilots, "You received no



visual clues at all about the runway environment. It was like landing on a pitch-black night without any lights."

Tests culminated with a landing in actual limited-visibility conditions at an airfield in Fresno, CA. Conditions were foggy and below minimums: the restriction for C-130s flying with typical landing systems is a ceiling of 200 feet and a runway visual range of about one-half mile. During the landing, the ceiling was 50 feet and the runway visual range was about 700 feet. The landing was successful.

### System Description

The ALG system uses short range imaging radar to send information to the pilot's head-up display. The pilot can then land the aircraft using a radar-generated image of the airfield.

The head-up display image shows areas of high reflectivity, such as buildings, approach lights and objects, in green. Areas of low reflectivity, such as the runway, are blank.

Besides allowing zero visibility landings, the system can help pilots land aircraft at simple airfields not equipped with landing lights or beacons.

The static images shown on Figure 1 provide a comparison between the actual view looking out the cockpit window in dense fog, and the ALG runway image on the head-up display. For the full actual "live" footage from one of the test flights, visit [www.aircraftcontrols.com/alg/lf.htm](http://www.aircraftcontrols.com/alg/lf.htm). Here, you can look at a streaming video of the landing sequence. To play the streamed video, you will need QuickTime version 4.0 installed on your computer. Once installed, the video will determine your connection speed to the Internet and optimize the delivery of this video. A JavaScript version of the video is also available on the same site.

### Signal Processing

Figure 2 is a simplified block diagram of the ALG System Configuration. The diagram also shows how it interfaces with some other aircraft systems. The output of the 94 GHz transceiver is sent to the ALG processor, where it is combined with the data out of the inertial navigation system. After appropriate signal processing, the output of the ALG processor is sent to the head-up

## Zero-Visibility Landing Guidance System

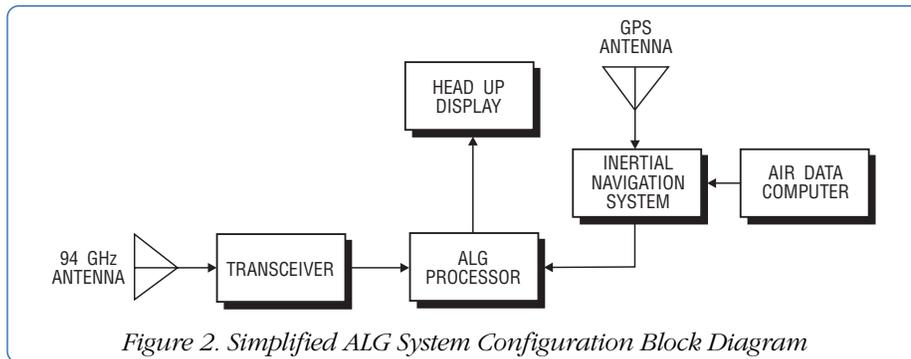


Figure 2. Simplified ALG System Configuration Block Diagram

[Continued from page 1]

display. The weather penetrating imaging radar mounted in the aircraft's X/W band radome, generates a real-time raster image of the runway. The combination of the head-up display control and guidance coupled with the real-time raster image of the runway provides the pilot the integrity needed to maintain the glidescope to touchdown, as if there were no visibility restrictions.

### The Test System

In order to test the integrity of the ALG system, BAE SYSTEMS developed the test system shown in Figure 3. The system includes boards from Pentek and DSPCon, plus other commercial components, and was integrated by DSPCon.

The DSPCon Model 9100 provides up to four high-speed multichannel serial interfaces and can pass data directly to and from DSP processor hardware via  $\text{C40}$  comm ports, thereby avoiding host and backplane bus bottlenecks. The channels of the 9100 have independent clocks and are capable of transmitting and receiving data at up to

160 Mbit/sec. On-board FPGAs provide for future customization.

The user supplies RS-232 differential data plus external clock to the 9100. When initiated by a front panel switch, synchronous data is streamed from the 9100 to a Pentek 4284 single  $\text{C40}$  DSP Processor via two comm port connections. The 4284 acts a system controller and responds to commands which are provided by a serial port connected to one of the two Pentek 4260 SCSI controllers (this connection is not shown in the diagram).

When commanded, the 4284 accepts data from the 9100 and routes it to the two SCSI disk drives via the two Pentek 4260s. When a data capture is complete, the DSP is commanded to copy the data from both disks onto the DLT-7000 tape drive. The tapes may then be read from another DLT-7000 tape drive connected to any workstation.

The test system was used by BAE SYSTEMS to simulate the input signals to the ALG processor and to observe and calibrate the patterns generated by the processor on the head-up display. □

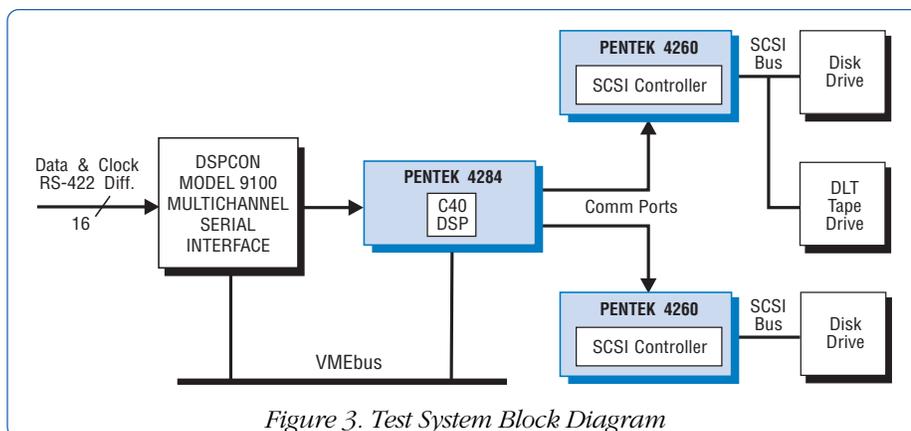


Figure 3. Test System Block Diagram

## Online Seminar

To register go to to  
[www.pentek.com/swradio](http://www.pentek.com/swradio)

An online seminar will be presented by Pentek on December 5, 2000 at 1:00 p.m. EST. The topic is *FPGAs Offload DSPs for High Performance Software Radio and Wireless Communications*.

By incorporating FPGA technology in a typical software radio system, processing tasks can now be judiciously split between the FPGA and the DSP. By freeing the DSP to concentrate on more complex and sophisticated tasks, the use of FPGAs can be a strategy for improving system performance and throughput, lowering total system cost, and shortening development time.

Some of the more popular functions now possible within FPGAs include FFT (Fast Fourier Transform) processing, an extremely critical function for radar and other applications. Pulse-matched filtering performed in the FPGA can greatly enhance the signal-to-noise performance of RF systems. Many new digital telecommunications standards such as CDMA can take advantage of FPGAs to encode and decode transmission streams.

Typical DSP software radio systems and product solutions will be discussed during this seminar.

### Learn how:

- Standard logic cells are now faster and more capable of handling complex functions
- New software tools for designing, testing and reconfiguring FPGAs significantly reduce algorithm development time
- To lower your cost per channel
- Typical signal processing functions are best allocated to hardware, FPGAs or DSPs
- To increase your product density  
... plus lots more! □

## 8-Channel 16-bit A/D Converter VIM-2 Module

[From page 4]

THD is less than 85 dB below full-scale, while SFDR is better than 85 dB.

### Sampling Clocks & Support

The 6215 comes with a standard internal reference clock of 30 MHz which allows sample rates from 4.7 kHz to 234 kHz. Other internal references are available for various applications, such as those that require a precise 8 kHz sampling rate.

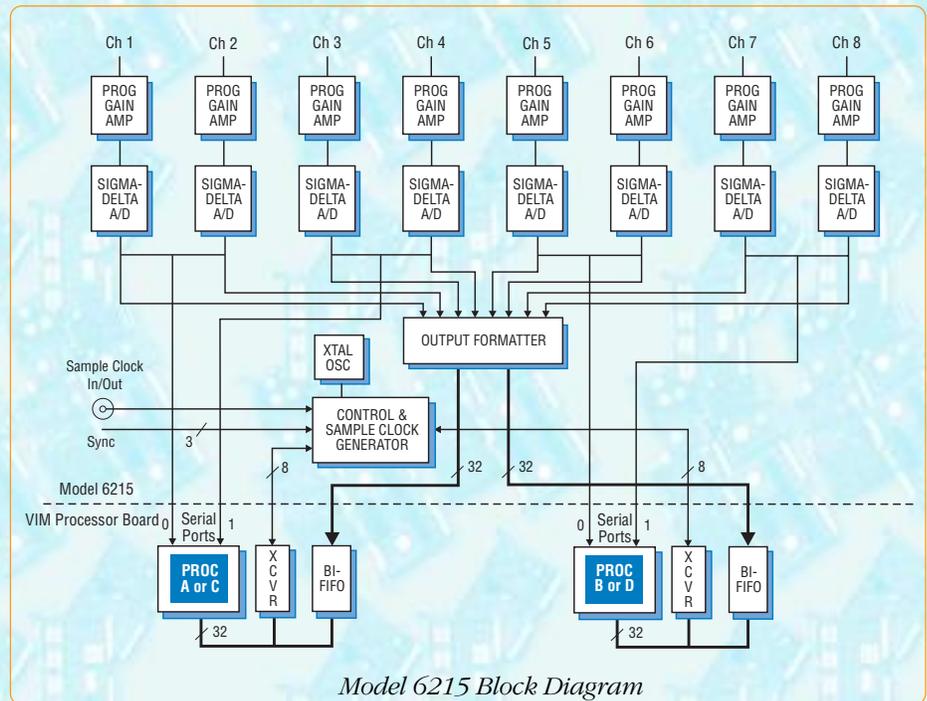
The 6215 also accommodates TTL-compatible external sampling clocks with minimum frequency of 600 kHz and maximum frequency of 30 MHz.

The sample rate  $f_s$  is defined by:

$$f_s = \text{Ref. Clock} / [128 * (N+1)] \text{ where } N = 0 \text{ to } 49.$$

Pentek's ReadyFlow Board Support Libraries are available for this product.

For more information, visit our web-site at <http://www.pentek.com> □



## Pentek's New Website Has More Technical Information And Is Easier To Use

Recognizing that the Internet is often an engineer's first contact, Pentek has invested heavily to improve the layout, content and navigation of our [www.pentek.com/](http://www.pentek.com/) site.

### New Applications Design Form

We realize that your needs change quickly and so does the technology that we use. Pentek has added an Applications Design Form to the site to make it much easier to select the right product for your application. You simply fill out some essential questions on an online form so we can get back to you with suggested system configurations to meet your needs. You don't have to spend time online trying to figure out which products will work best for you, we'll do it for you!

### Technical Support

Online technical support is now available via the web! Online support forms can now be submitted easily, expediting your requests and saving you time. Plus, customer Knowledgebase cases can be sent to you automatically

by setting up or updating your *YourPentek* account. Both of these new tech support web features will provide you with additional, quicker access to the answers you need.

### The Centrals

New "Central" areas have been created to make it easy for you to find the relevant information you need all in one place. A "Central" site consists of all technical documents, brochures and manuals, presentations, online seminars, FAQs, related software, and third party information. New "Central" areas include DSP Central, VIM Central and Software Radio Central.

### More Improvements

Page design has been optimized for both display and printing and a new search tool has been implemented for a more thorough search throughout the site. A new feature in the technical



documentation section, "Forward to a Colleague", allows you to easily forward key information to someone else.

### Automatic Email Updates

As always, don't forget to set up a *YourPentek* account to receive automatic email updates for all new postings relevant to the products you select.

### Now Available!

Log on today to check out all the new features. □

# Product Focus

**Model 6215**

## 8-Channel 16-bit A/D Converter VIM-2 Module Features Eight Sigma-delta A/Ds with Inherent Anti-alias Filtering



Intended for Pentek's VIM-compatible processor boards, Model 6215 is a VIM-2 module that includes eight 16-bit sigma-delta A/D converters, with 4.7 kHz to 234 kHz sample rate. Two of these modules can fit on a processor board to provide 16 A/D channels which utilize all four processors while occupying just one VMEbus slot.

### A/D Converters

Analog inputs are accepted on multipin front panel connectors with provisions for either single-ended or differential signals. Programmable-gain input amplifiers cover a range of 0 to 20 dB.

The A/D converters utilize sigma-delta technology and include anti-alias filters with a cutoff frequency that tracks at 46% of the sampling rate.

The eight channels of A/D converters are arranged in two groups of four converters each, with each group assigned to one processor. Within each group, one pair of A/D converters is attached to one of the processor's serial ports and the other pair to the second serial port. Alternately, both pairs may be connected to the processor BI-FIFO. In this mode, output data flow may be user-configured with data from any combination of A/D channels routed to either BI-FIFO.

### Input Characteristics

The 6215 features differential inputs with  $\pm 1$  Volt to  $\pm 10$  Volt range and 10 kohm input impedance. All inputs feature  $\pm 40$  Volt overvoltage protection, while input gains are independently selectable in steps of x1, x2, x5 and x10. ➤

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