

# The Pentek Pipeline

A quarterly publication for engineering system design and applications.

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- **Feature:** Learn about creating an SDR system from the latest hardware, firmware, software, and design tools available from COTS vendors that can be used as a 5G development platform.



*“These SDR platforms provide superior signal integrity performance, high test repeatability, and modular assemblies that comply with the constantly changing 5G design requirements. Future 5G implementations will require many development platforms for experimentation, and the use of a COTS system as a starting point will ensure an accelerated time-to-market.”*

~ Bob Muro, Application Specialist, Pentek

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## Accelerating 5G Product Development by Using a COTS-Based SDR System for the Development Platform

by Bob Muro

Commercial-Off-The-Shelf (COTS) Software Defined Radio (SDR) products have been traditionally used for military radar and communication applications because of their high performance and design flexibility. The latest SDR products offer solutions with integrated I/O, ARM processors, and large FPGAs that include intellectual property (IP) for accessing, routing, and processing digital data. Combining these attributes with superior signal integrity, phase-coherent sampling, and multi-channel transceivers, a COTS SDR system is an ideal choice for your 5G development platform. This article is designed to familiarize a new user about Software Defined Radio in a multi-purpose COTS platform that can reduce the time-to-market of your 5G products.

## A Brief History of COTS

During the early 1990s, congressional spending cuts meant the US military had to reduce R&D spending but had to retain global technological leadership for America's security. In 1994, then Secretary of Defense, William Perry, wrote a memo requesting that the military increase the purchase of commercial products and the use of commercial practices and specifications. The memo was officially enacted into law as part of the Federal Acquisition Streamlining Act (FASA) of 1994 and was a departure from the more stringent military specification requirements of the past that prohibited the purchase of more general-purpose commercial products. This created a new industry based on commercially ➤

available high-performance products that could be re-purposed for “dual-use.” As a result, an abundance of COTS products are available today with the latest technology available for both military and commercial purposes.

## COTS SDR Defined

Each section of this article is divided into hardware, firmware, and software sub-sections for additional clarity. The hardware is the SDR PCB, including components; the firmware is internal FPGA code used to create a logic design and

implement digital signal processing (DSP) functions; and the software is C code to control an FPGA with firmware and to perform any additional DSP functions.

## Hardware

SDR replaces legacy analog systems that consisted of an RF filter, analog down-converter (Lo + Mixer), band-pass filters, and a demodulator (see **Figure 1a** below). These fixed analog systems were limited to a specific platform like AM or FM radio and needed to be replaced if another platform was required.

The primary function of SDR is to exploit digital signal processing techniques to support the ever-increasing complexity, precision, and bandwidth of today’s radio traffic. Suitable data conversion is required between the antenna signals and the DSP operations for both receive and transmit functions.

An SDR receiver converts an RF signal from an antenna into digital samples with an A/D converter and uses subsequent DSP operations to extract the required information from the signal (see **Figure 1b** below). ➤

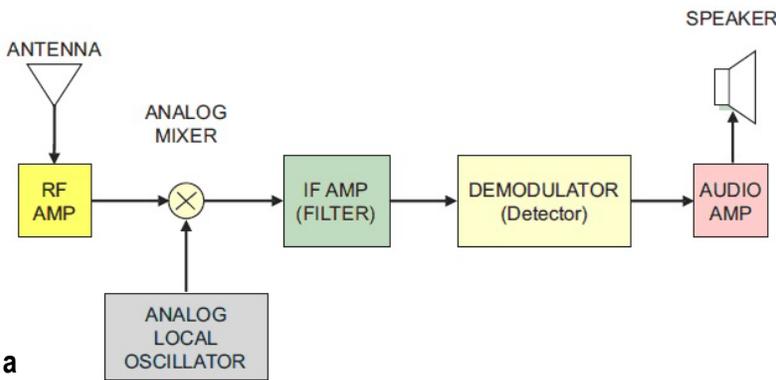


Figure 1a

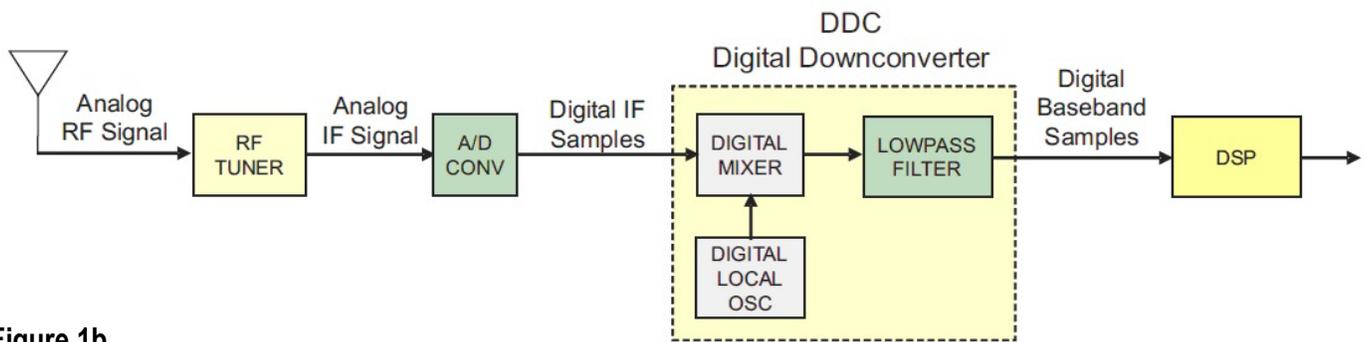


Figure 1b

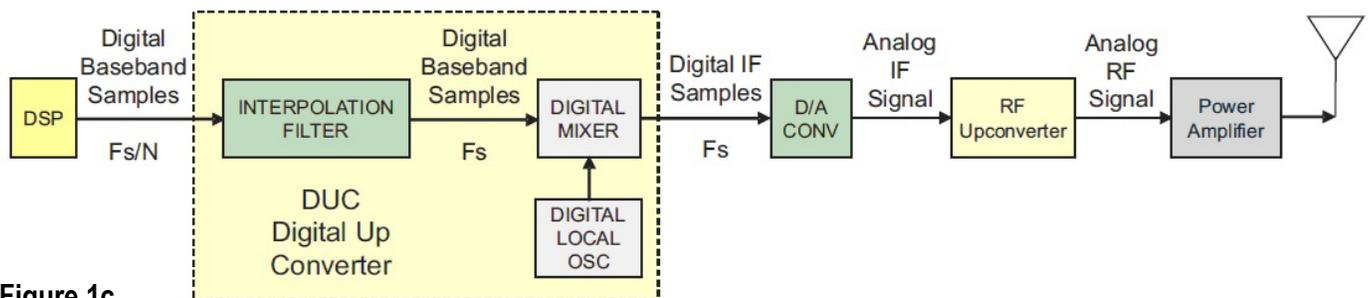


Figure 1c

An SDR transmitter accepts digital information to be transmitted and then performs the necessary DSP operations to produce digital samples for a D/A converter, whose analog output signal drives a PA for delivery to the antenna (see **Figure 1c** on the previous page).

Because these radios are software defined, they can be programmed on-the-fly with new parameters in microseconds, or re-configured for many different purposes by simply loading a new firmware image from internal or external memory.

An SDR is often implemented on a specialized PCB board designed for superior signal integrity and precision timing. The current generation of these cards is a switched-fabric mezzanine card, an XMC, or an FPGA mezzanine card, an FMC. **Figure 2** (below) shows both of the card types with the key difference that the XMC mezzanine includes the FPGA, and the FMC

requires a more complex carrier with an FPGA. In this example, each card is connected to a 3U OpenVPX™ carrier that fits into a 3U VPX chassis.

Either of these mezzanine cards can be combined with a different form-factor carrier and installed into a different chassis, or PC motherboard. This allows the same software radio functions to be used on different platforms in multiple systems.

**Figure 3** (on the next page) contains images of XMC and FMC mezzanine cards, with the corresponding functional block diagrams to the right. **Image A** (in **Figure 3**) is an XMC card with four 200 MHz A/D channels, and **image B** is an FMC card with two 3.0 GHz A/D channels and two 2.8 GHz D/A channels. These cards can have an analog or digital interface and are only two of the many different multi-channel SDR mezzanine cards available from a COTS manufacturer. For sim-

licity we will describe the XMC card in detail because it contains both the analog I/O and an FPGA. Details of the 2-channel A/D, and 2-channel D/A FMC card (**Model 3320**) can be found on the Pentek website by following [this link](#).

At the core of this example SDR board is a precision timing system with a multi-bit, fractional synthesizer for variable sampling rates locked to an on-board OCXO, or a reference input signal (see **Figure 3**).

These timing systems usually accept external synchronization signals from an NTP (Network Time Protocol) server or GPS receiver for the highly precise timing requirements of a radar or cellular system. This level of precision is also required for phase coherent sampling of the A/Ds, FPGA DSP data synchronization, and D/A signal transmission. ➤

**Figure 2**

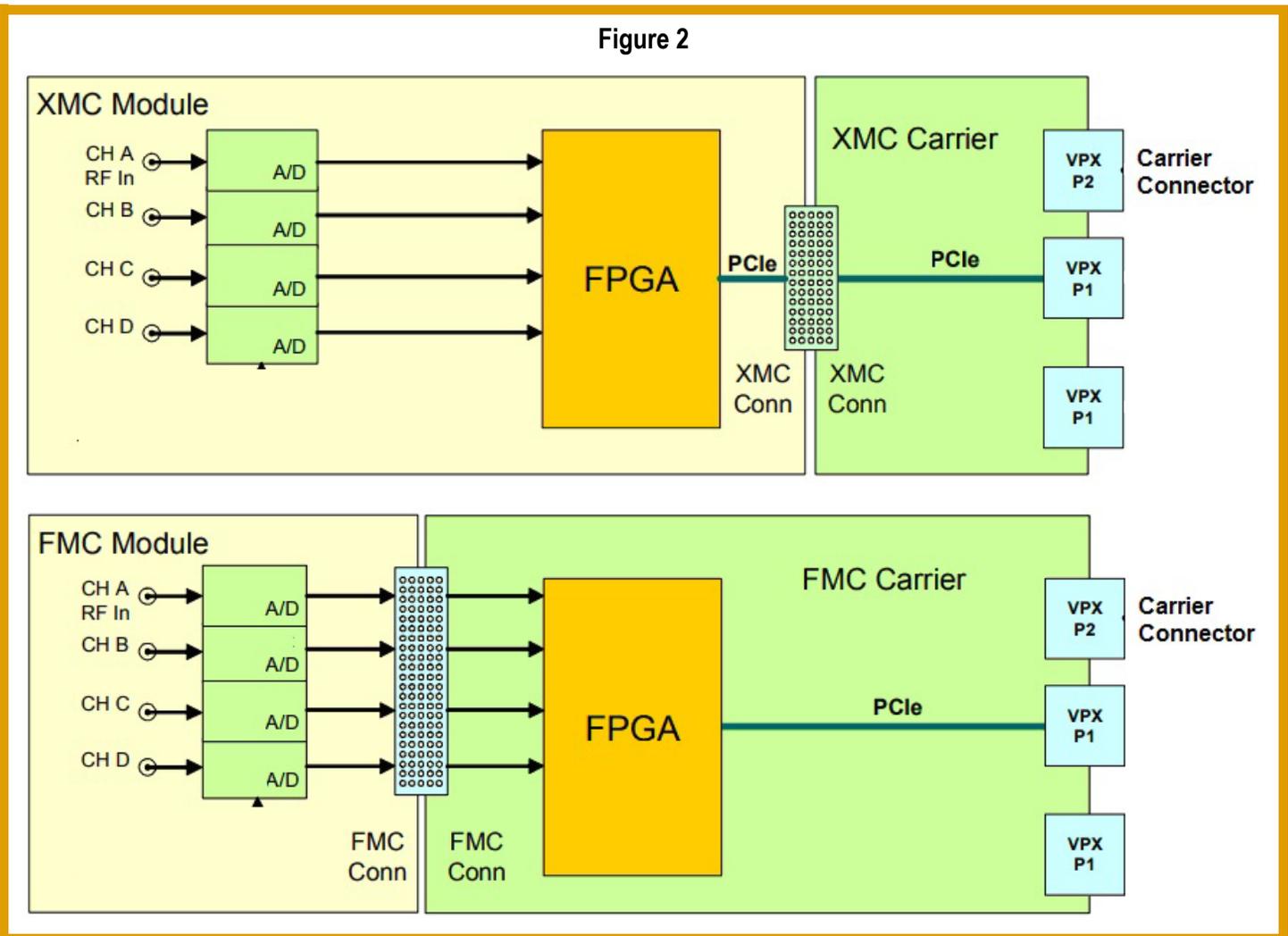
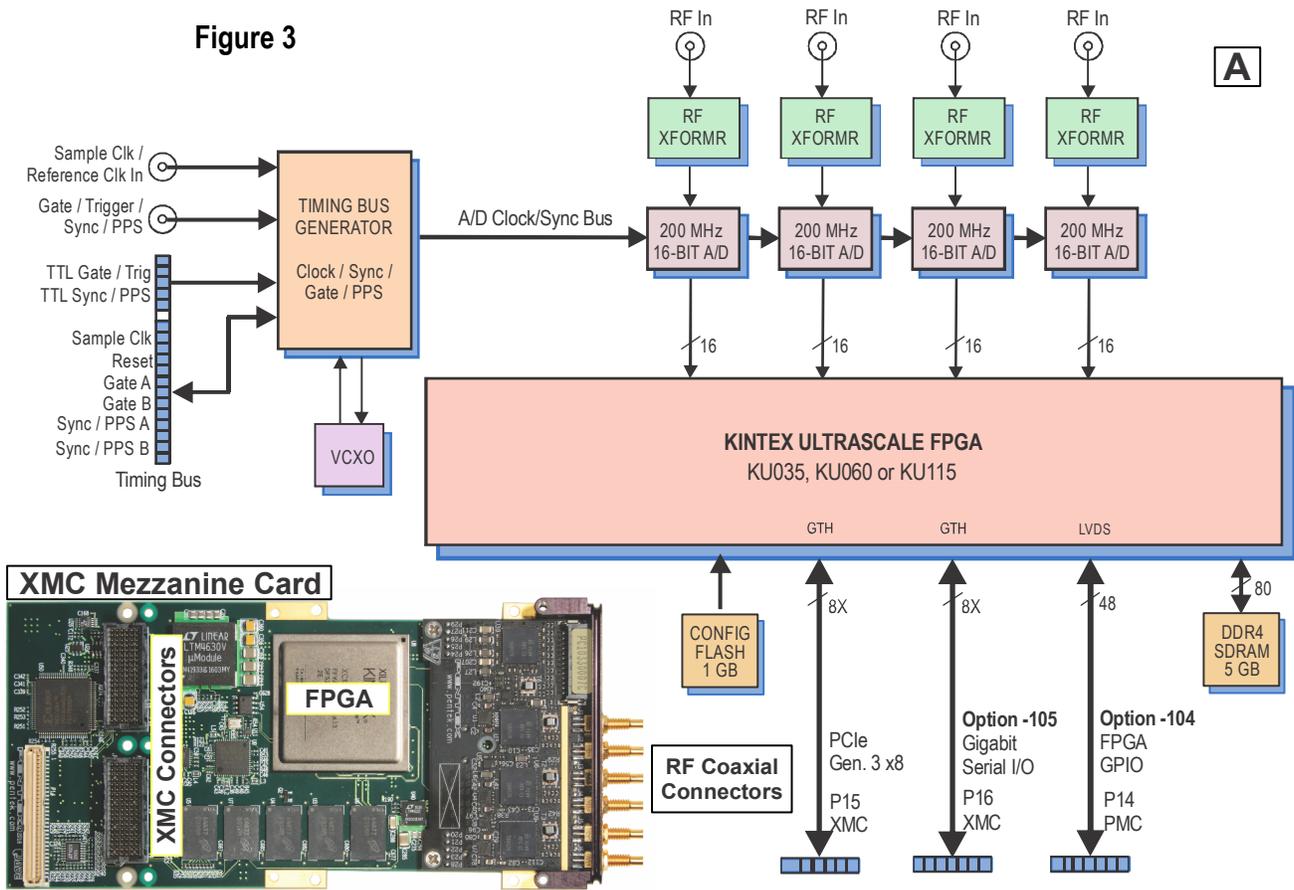
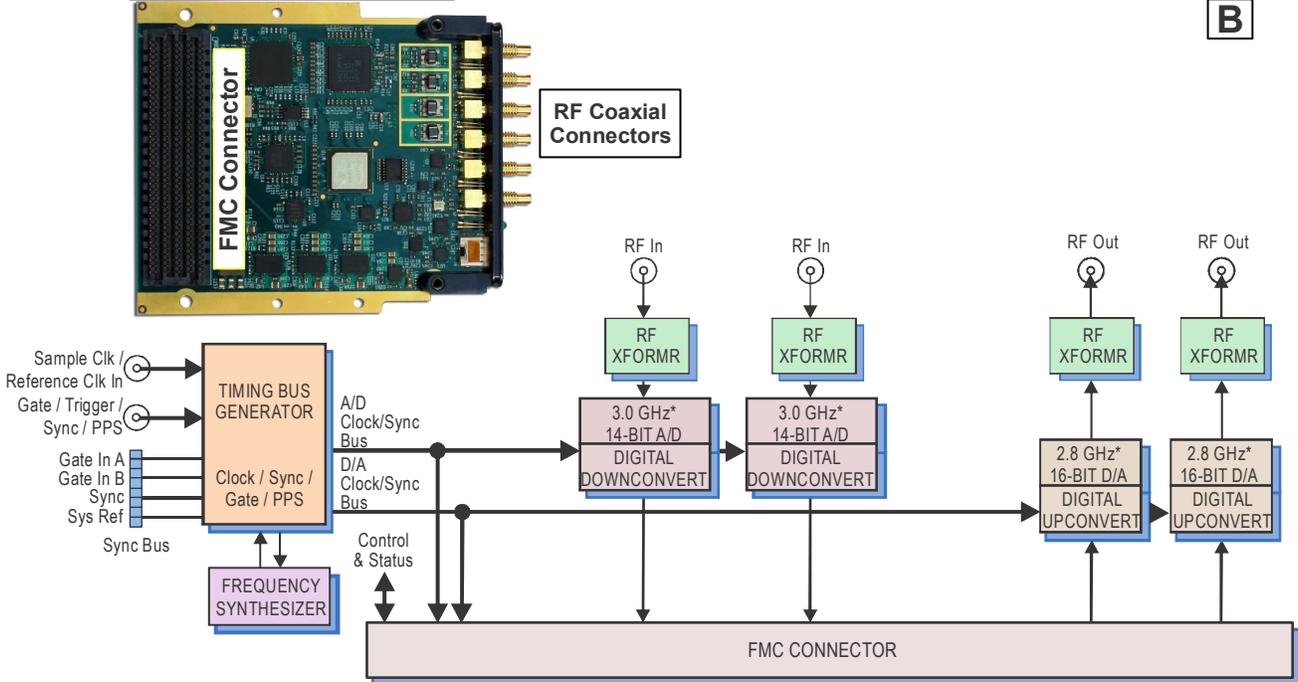


Figure 3



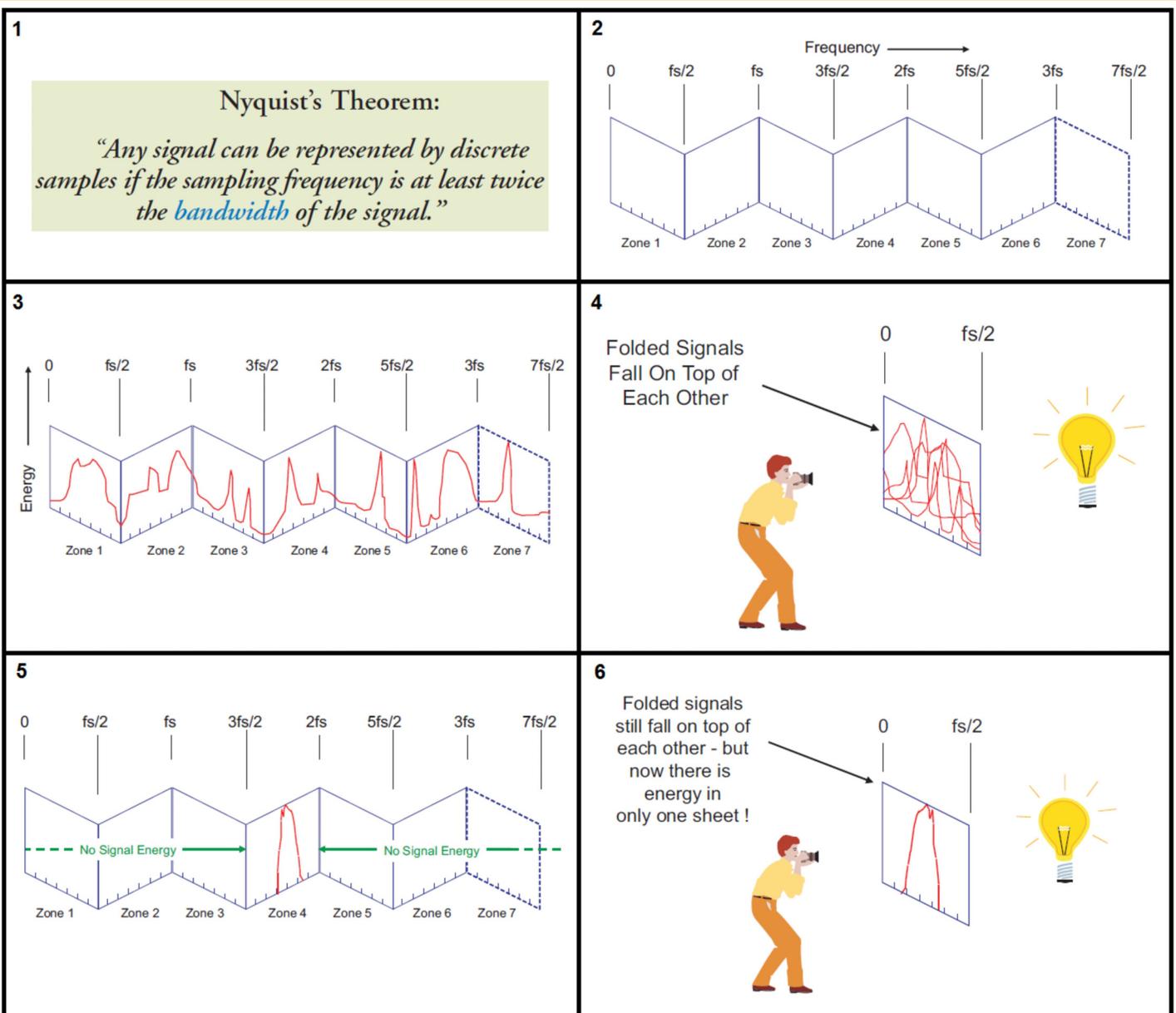
FMC Mezzanine Card



## Nyquist Zone Sampling

- 1) "Bandwidth" is highlighted in the Nyquist theorem below to distinguish it from frequency when explaining the concept of under-sampling.
- 2) Traditional fan-fold printer paper illustrates the location of "Nyquist Zones", which are defined as multiples of half the sampling frequency,  $F_s$ . In our XMC example  $F_s = 200$  MHz, and  $f_s/2 = 100$  MHz, so successive Nyquist zones occur every 100 MHz.
- 3) All signal energy must fall within one Nyquist zone to satisfy both the bandwidth and frequency requirements of the Nyquist Theorem. This example of a wideband signal (shown in red) crosses multiple zones and violates the "single zone" rule.
- 4) To illustrate the result of sampling this signal, collapse the fan-fold paper and back light it. All the signal energy above  $f_s/2$  is aliased into the first zone. This can be corrected by using a LPF to remove all signal energy above  $f_s/2$ .
- 5) Another example is a narrow-band signal that falls entirely within Nyquist zone 4 (between 300 MHz to 400 MHz in our case). The signal can be properly sampled using a suitable band-pass filter that eliminates signal energy from all other zones.
- 6) Although the signal frequency is  $> F_s/2$ , all the energy is contained within one zone, satisfying the Nyquist Theorem. Sampling above Zone 1 is called "under-sampling."

For a more detailed explanation of this technique, refer to Pentek's [Software Defined Radio Handbook](#).



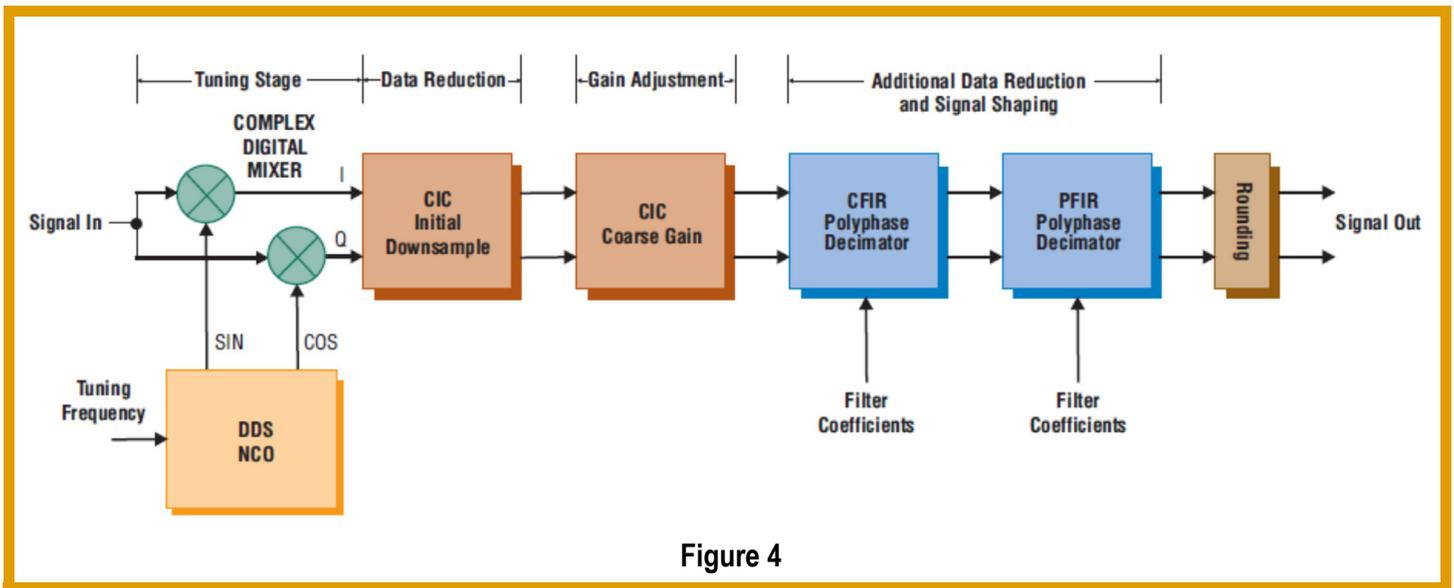


Figure 4

Each A/D has a 200 MSPS maximum sampling rate that can capture a 100 MHz Nyquist bandwidth, excluding filtering. A common technique with digital radio is to acquire channel information, or intermediate frequency (IF) bandwidth, by under-sampling the signal. For an explanation of the "Fan-fold" concept using multiple Nyquist zones, see [Nyquist Zone Sampling](#) on page 5.

Under-sampling allows an A/D with a lower sample rate and higher dynamic range to capture a narrow bandwidth signal centered at a higher frequency without loss of information. In order for this to work correctly, the RF input path and the A/D must accommodate these higher frequency signals. Our previous 200 MHz A/D example requires an A/C transformer with > 400 MHz pass-band and adequate Band-Pass-Filtering (BPF) to reduce noise and additional harmonics from all Nyquist zones, excluding the fourth.

After meeting the Nyquist criterion for A/D sampling, the next stage is typically the DDC (Digital Downconverter). The DDC is often implemented as IP firmware within the FPGA. It performs frequency translation and bandwidth reduction as described in detail in the next section.

## Firmware

An FPGA consists of unconnected logical, arithmetic, and signal processing building blocks that must be configured

### SNR and Digital Process Gain

The calculation for theoretical SNR of an ADC:

$$\text{SNR} = 6.02 * N(\text{bits}) + 1.76 \text{ dB}$$

or, for our 200 MHz 16-bit A/D,

$$\text{SNR} = 6.02 * 16 + 1.76 \text{ dB, or } 98 \text{ dB}$$

Due to A/D non-linearity, additional noise from the LNA input, and sample clock jitter the measured SNR for a good quality A/D is limited to  $\approx 75$  dB. This calculation also assumes the input signal is full-scale, which often varies because of the reduced gain, or back-off setting of the front-end LNA to compensate for high crest-factor communication signals. The dynamic range can be improved by reducing the full Nyquist BW down to the channel bandwidth of interest using a DDC. Our 200 MHz A/D, with  $F_s/2 = 100$  MHz, and an example 5 MHz LTE channel has the following calculated process gain, or reduction in RMS noise:

$$\text{SNR}_{\text{pg}} = \text{SNR}_{\text{nyquist}} + 10 * \log_{10} \left( \frac{F_s/2}{F_{\text{filter}}} \right) = 75\text{dB} + 10 * \log_{10} \left( \frac{100 \text{ MHz}}{5 \text{ MHz}} \right) \approx 88 \text{ dB, or a } 13 \text{ dB improvement.}$$

with firmware (IP) for operation. This is ideal for extreme programming flexibility, but complex because it requires development of the firmware. Some COTS SDR manufacturers provide FPGA IP for basic operation of their board to simplify the development process. This usually includes analog and digital I/O functions for acquiring and transmitting data, along with DSP IP for specific radio functions like DDCs, filters, channelizers and engines to transfer data to the system.

The DDC function requires three IP building blocks: the NCO local oscillator, a complex mixer, and digital filters to replace those functions of the legacy analog radio system (see [Figures 1a and 1b](#) on page 2).

[Figure 1b](#) is a functional block diagram of the SDR with the DDC. The tuning stage of this DDC uses a complex digital mixer to translate the frequency of interest down to baseband. A pair of multipliers driven by a direct digital synthesizer (DDS) numerically controlled oscillator (NCO) allows the user to "tune" the receiver to the desired frequency. The samples are then passed through a LP FIR filter to decimate the signal for a finite (channel) bandwidth.

[Figure 4](#) (see above) is a more complex version of the classic DDC with additional stages for fine decimation and gain adjustment. The cascaded integrator comb (CIC) filter decimates the data, ➤

reducing the sample rate and effective bandwidth. The second CIC further reduces bandwidth and provides coarse gain adjustment, while the two polyphase filters provide final bandwidth reduction, additional decimation, and signal shaping.

The CFIR (compensation FIR) helps flatten the pass-band and the PFIR (programmable FIR) helps eliminate ripple. The complex I&Q data is now ready for streaming to another section of the FPGA to be processed further or delivered to the system.

Two key benefits of the DDC are higher SNR as a result of decimation, and the ability to tune to the narrow-band signal center frequency. Decimating the signal effectively lowers the sample rate and reduces uncorrelated, white noise, referred to as process gain, and the NCO digitally tunes to a specific carrier frequency within a single Nyquist zone.

## Software

Depending upon the application, the vendor-provided FPGA IP might meet the application specifications, but requires controlling software to operate the radio. The FPGA IP needs operational parameters sent across the system interface from a software program. This is the function of a board support package (BSP) normally written as “C” callable routines for a Windows or Linux operating system environment. The BSP contains library functions and pre-compiled example code that can be executed to test board functionality.

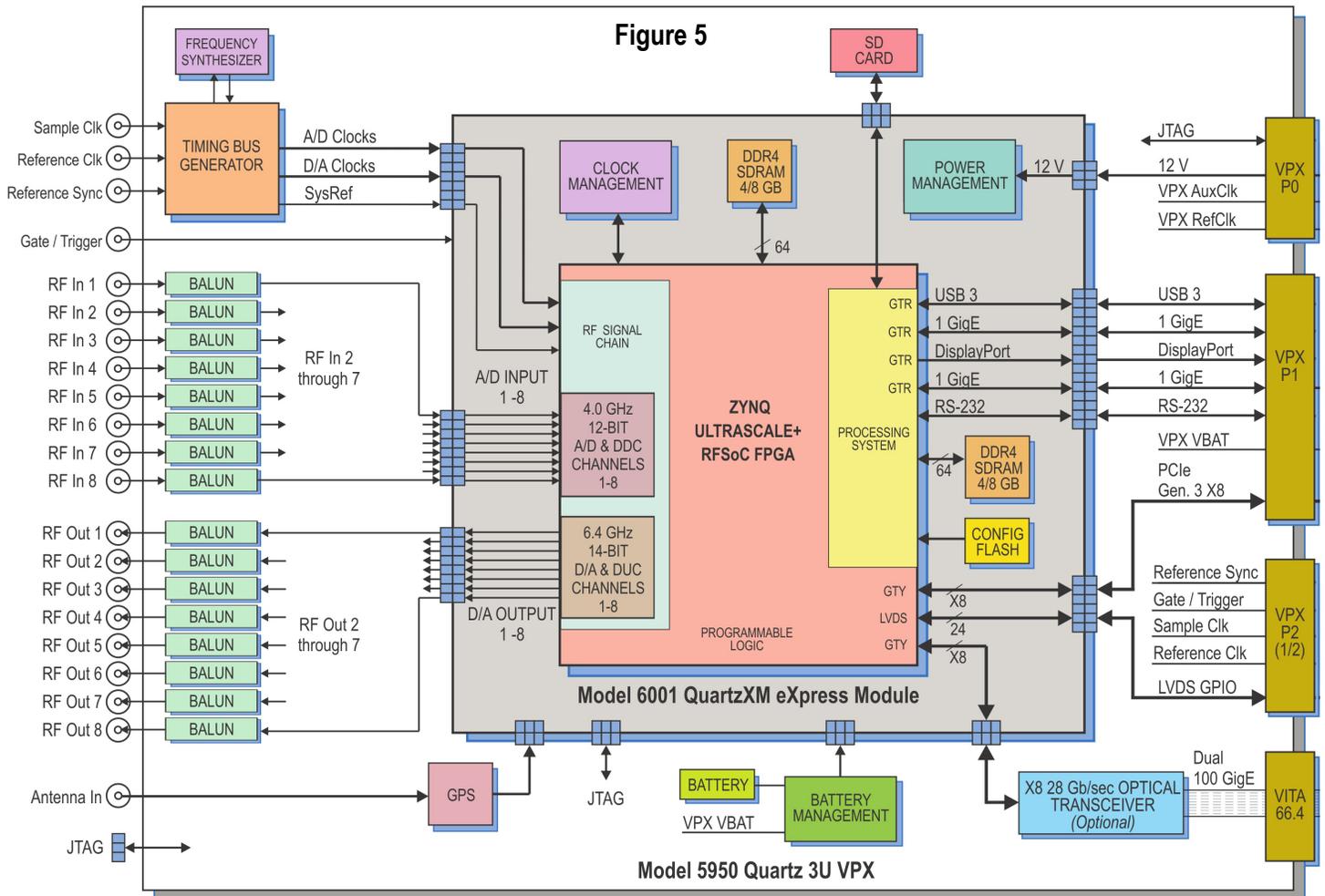
An example case for SDR is commanding the A/D to capture and transfer data to the FPGA for further processing in the DDC. This processed data can be stored to memory or transferred to the D/A section for conversion back to an analog signal and output for transmission. This is an

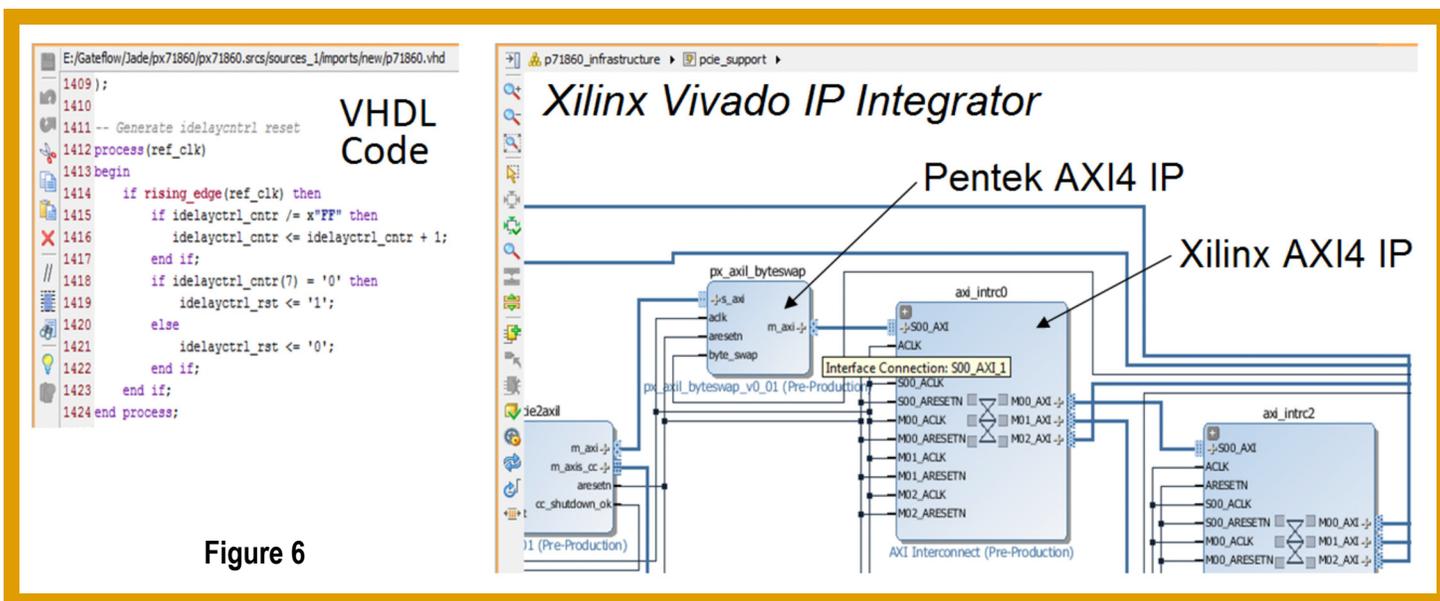
example of a software program developed using the BSP software library functions and drivers. If any new FPGA IP is created by the user, additional control software must be written for inclusion in the BSP package.

## The Latest COTS SDR Technology

### Hardware

Over the past 10 years, FPGA manufacturers like Xilinx have been improving technology by reducing the silicon fabrication structure size, and as a result the device size, weight and power (SWaP) values were reduced. In late 2008, the Xilinx Virtex-6 family was constructed using a 40nm process, and had an average 2000 DSP slices per FPGA. By 2017 the Ultra-scale family used a 20nm process and ➤





**Figure 6**

the FPGA DSP slices had increased to approximately 5.5K. The latest System-on-Chip (SoC) device from Xilinx, the RFSoc, consists of FPGA fabric with ARM processors, A/Ds, and D/As, all on the same chip. The 16nm technology has over 4.2K DSP slices, four 1.5 GHz A53 ARM processors, two 600 MHz R5 ARM processors, eight 4 GHz, 12-bit A/Ds, and eight 6.4 GHz, 14-bit D/As per device. This game-changing technology is being used by COTS manufacturers to provide multi-channel SDR transceivers for engineers developing 5G radio products.

**Figure 5** (on the previous page) is a functional block diagram of one COTS implementation of the Xilinx RFSoc and

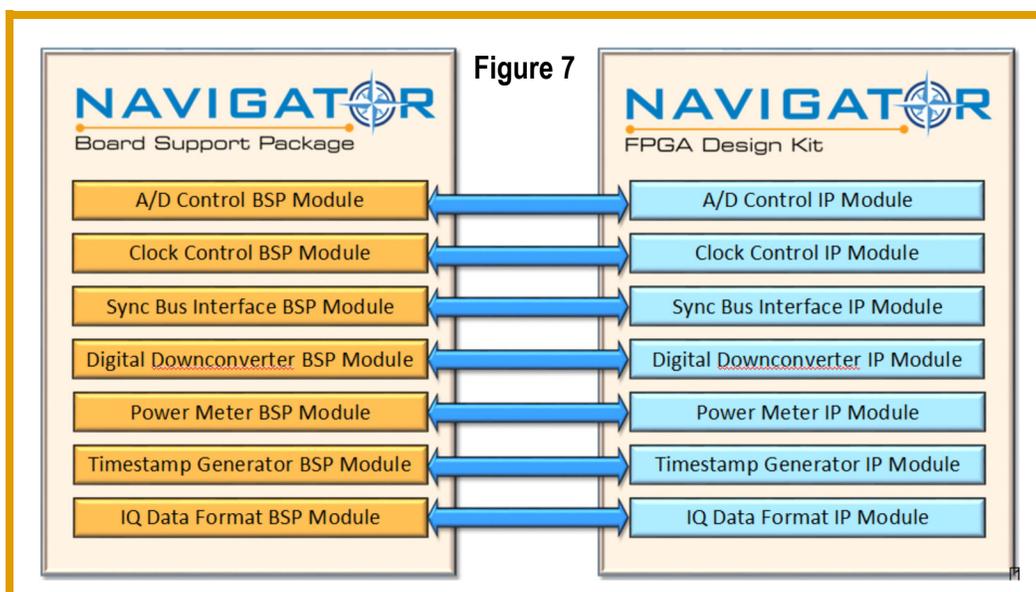
is the central component of the **Model 5950 3U VPX board from Pentek**. The gray area is a fully connectorized RFSoc or System-on-Module (SOM) that plugs into the 3U VPX carrier. This device can be controlled via a Gigabit Ethernet port, similar to the previous generation FPGA, but the on-board ARM processors allow autonomous operation and the ability to communicate with, or control devices locally, or on an external network.

### Firmware

Previous generation FPGAs were programmed using a textual hardware description language (HDL) like VeriLog,

or VHDL. The latest AXI4-compliant IP blocks are included in Vivado® from Xilinx. The IP Integrator tool from Xilinx has virtual graphical blocks that represent HDL code, which can be connected to one another via drag-and-drop wiring.

**Figure 6** (above) shows VHDL code on the left in contrast to the graphical block representation on the right. This more intuitive way to program allows someone new to FPGAs to wire together logical blocks that represent hardware like FIR filters and DDCs, to create an SDR. This programming method supports fast integration of vendor-supplied, hardware-specific IP blocks with IP blocks from the main Xilinx library.



**Figure 7**

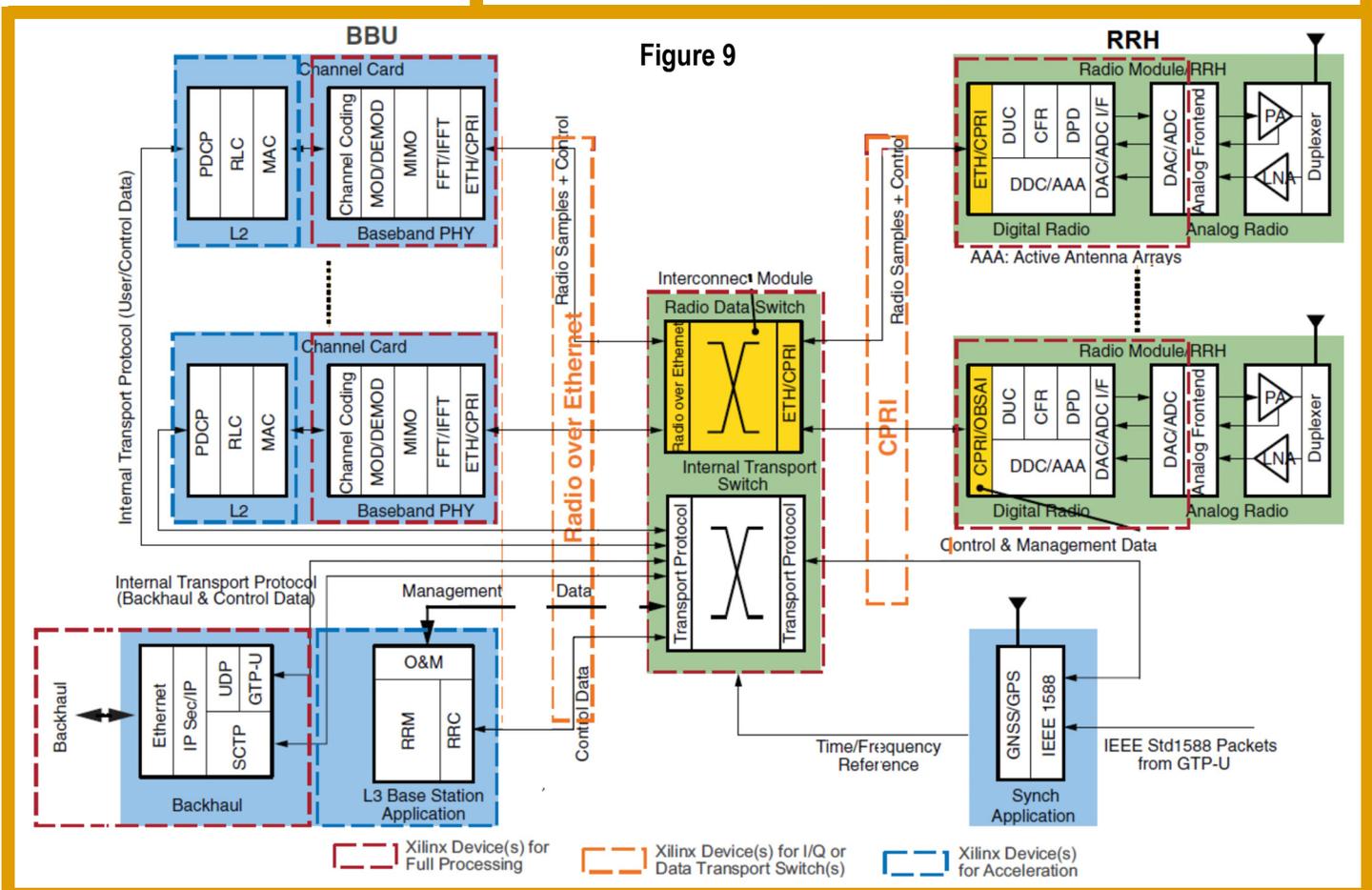
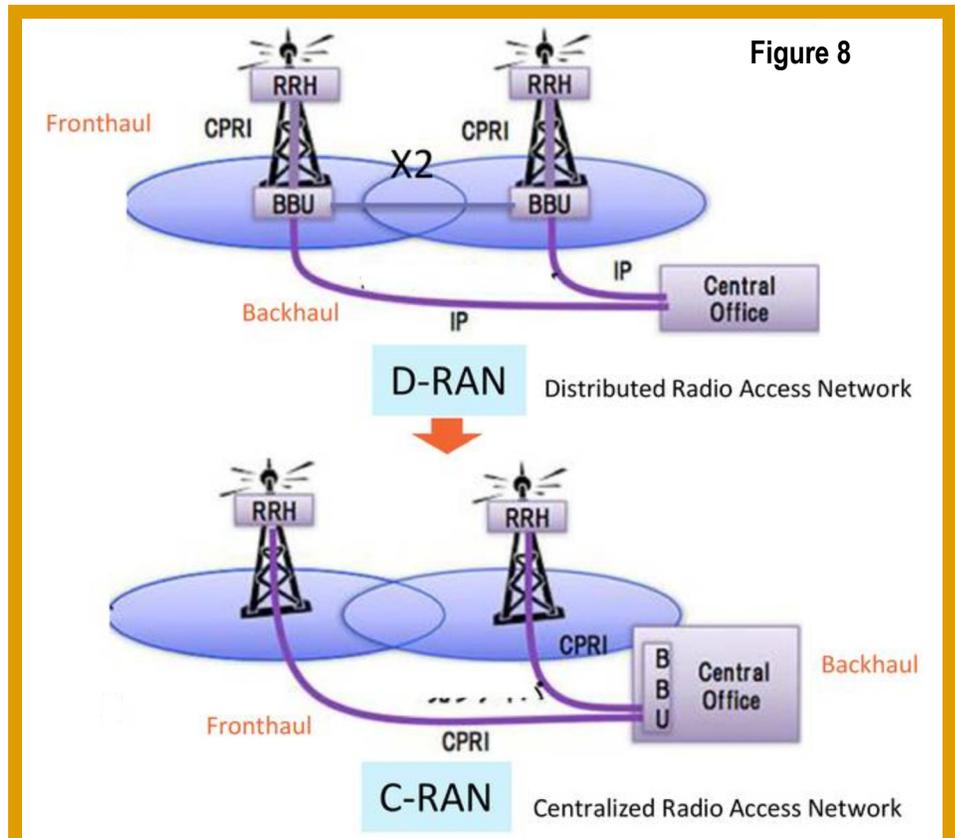
### Software

These latest IP programming advances provided an opportunity for COTS vendors to deliver all the related IP and BSP modules together. **Figure 7** (to the left) illustrates how each IP module has a single corresponding BSP module that contains all of the associated FPGA program parameters in one location. **Figure 7** shows an example listing of the **Pentek Navigator BSP** and **Navigator FDK IP** modules. ➤

## 5G Application-Specific Example

**Figure 8** shows the difference between a Distributed and a Centralized Radio-Area-Network. The traditional D-RAN “cell sites” are being replaced by newer C-RANs, initially to replace coaxial copper cable with optical fiber for signal quality, and from circuit switching to IP packet switching to combine voice and data in one system. The latest 5G millimeter wave and massive MIMO applications also require this network and radio separation.

**Figure 9** is a functional block diagram of a Centralized-Radio-Area-Network, or C-RAN, consisting of a base-band-unit (BBU), remote-radio-head (RRH), GPS time and frequency reference, and an interconnection switch. The BBU is normally located at a central office, or a virtual network (“the cloud”) with access to multiple optical data lines for back-haul, and the RRH is in an external location closer to the end user. The BBU and the RRH can



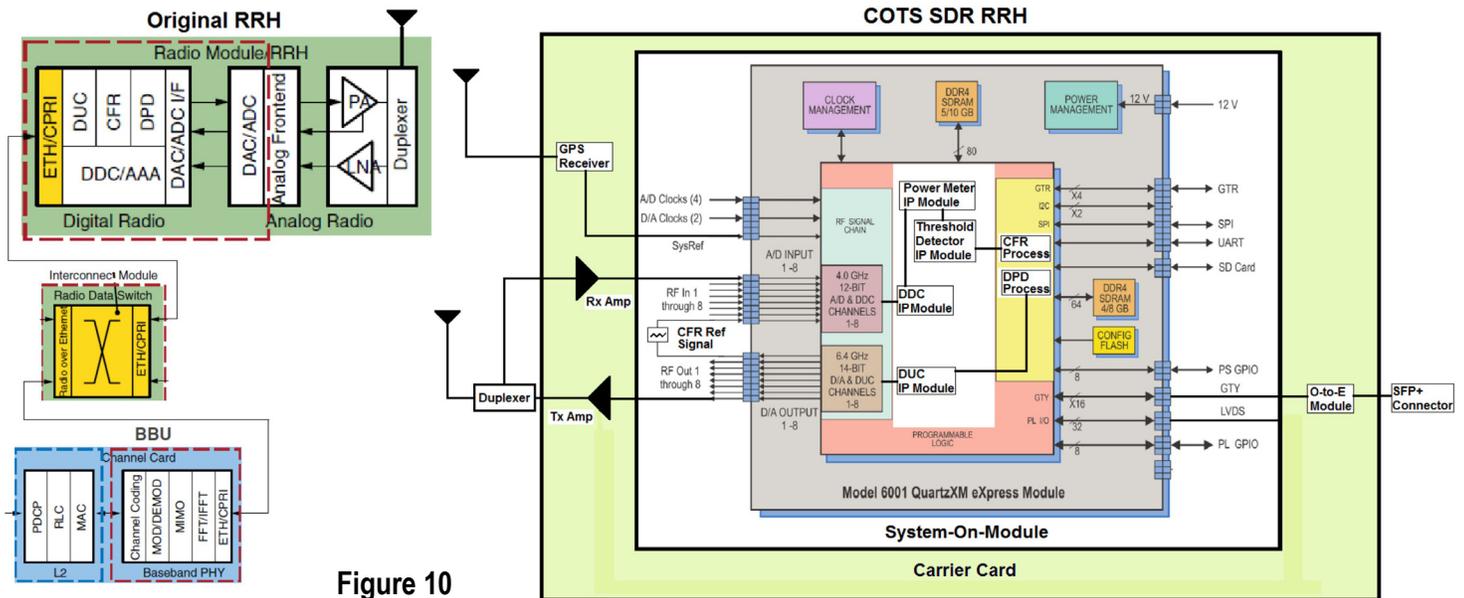


Figure 10

be connected using a Common-Public-Radio-Interface, or CPRI, Open-Base-Station-Architecture-Initiative, or OBSAI, or standard Ethernet, depending upon system requirements. These various transfer mode options, combined with legacy cellular, 5G TF (Verizon specification), or the 3GPP 5G NR specification, can be combined to form a complex heterogeneous network. Selecting a COTS SDR platform from the many multi-channel versions available is valuable because of the many solutions that require testing. Figure 9 (on the previous page) is an example COTS SDR board used to emulate an RRH.

## Hardware

A user equipment, or UE, OTA signal is received by the LNA via the antenna in the RRH. This RF signal is then filtered and adjusted for gain before input to the A/D. The digitized I/Q sample data from the A/D is packetized in the digital radio for front-haul transport to the BBU via a radio data switch. The packetized data is converted into a bit-stream for FFT, MIMO algorithm, demodulation, and channel coding. This data is then managed by the internal transport switch, and re-packetized for back-haul transport to the main cellular network for identification

and further processing. If a phone call is in progress, the user data will be sent out to another RRH using a CPRI or Ethernet protocol over fiber for OTA transmission to the other party by the reverse process. The previous explanation is a “very” simplified version of this process.

Figure 10 (above) is a sub-section of the original C-RAN with the RRH, radio-

### Maximum Data Transport Requirements

#### Example 1

A remote RRH with two antennas and a 5 MHz LTE channel bandwidth will have the following data transfer requirements:

- The 5 MHz channel requires at least 10 MHz sampling, or 10 MSPS to capture the information. There are two bytes per 16-bit sample, and two samples for I & Q.
- **SR<sub>max</sub> = 5 MS/s x 2 bytes/S x 2 for I & Q = 20 Mbytes/s x 8 bits/byte = 160 Mb/s**
- We have two antennas, so 160 Mb/s x 2 = 320 Mb/s data throughput is required and no issue for a CPRI port with a 10 to 25 Gb/s capacity.

### Maximum Data Transport Requirements

#### Example 2

A new 5G link with a 100 MHz channel and 8 antenna inputs increases the data transfer requirement to  $\approx 52$  Gb/s requiring multiple CPRI ports.

The preceding calculations ignore encoding variations.

data-switch, and BBU pictured on the left side of the figure and the COTS SDR RRH to the right. The custom modular carrier card (light green area) contains RX, and TX amplifiers, a GPS receiver, and an O/E transceiver module. The SOM (gray area) contains the RFSoc and all the connections for power management, data storage, and analog and digital I/O.

The incoming RF signal from the antenna is connected to the RX LNA via a duplexer, isolating it from high-power amplifier (PA) transmit levels, and connecting it to one A/D channel. This SOM and custom carrier combination can emulate the original RRH, provided it has the necessary IP described in the next section. ➤

## Firmware

Once inside the FPGA fabric, the digital samples are decimated, frequency selected, or tuned, and filtered in the DDC. The DDC output samples can be streamed to the power meter module for measurement, and sorted in the threshold detector IP module. These processed samples can be streamed to the ARM processors for crest factor reduction and digital pre-distortion routines before being up-converted in the DUC for re-transmission. The DUC is the reverse of the DDC, using frequency translation and interpolation instead of decimation. The digitized I/Q sample data is packetized in the digital radio for transport to the BBU via a radio data switch as in the previous description. Because of the variety of channels and various data transfer protocols, it is necessary to calculate the maximum data throughput of your signal.

## Software

Depending upon the desired level of control, either BSP routines need to be created for the new IP and ARM processors, or the ARM processors in conjunction with the FPGA can be programmed to operate autonomously.

## Conclusion

The purpose of this article was to familiarize a traditional radio engineer about the latest hardware, firmware, software, and design tools available from COTS vendors to create an SDR system that can be used for a 5G development platform. These SDR platforms provide superior signal integrity performance, high test repeatability and modular assemblies that comply with the constantly changing 5G design requirements. Future 5G implementations will require many development platforms for experimentation and the use of a COTS system as a starting point will ensure an accelerated time-to-market.

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# podcast

## The Art of (Rugged) Communication RFSocS, Radar, and Reliability

In this episode of **Fish Fry**, we are delving into the world of RFSocS, radar, ruggedization, and reliability. Rodger Hosking (Pentek) joins us to discuss the details of the Zynq UltraScale+ RFSoc and we take a closer look at the benefits and challenges of this unique single-chip adaptable radio platform.

To listen to  
the podcast,  
click here.



# Product Focus

## Model 71810

Pentek recently added a new member to the Jade™ family of data converter XMC modules. **Model 71810** is based on the Xilinx Kintex UltraScale FPGA and features LVDS digital I/O to meet custom requirements. The Model 71810 routes 38 pairs of LVDS connections from the FPGA to an 80-pin connector on the front panel. When mounted on a compatible single board computer or other XMC carrier, the Model 71810 provides a fully customizable I/O signal status and control interface.

*“The Jade Model 71810 is a fundamental FPGA engine with a choice of FPGA resources to meet needs from low cost to high performance,”* said Robert Sgandurra, director of Product Management. *“Pentek’s modular approach to*

*product design lets us quickly tune our products to our customer’s needs.”* The Jade XMC line uses personality modules to enable customization of XMC front end functions to meet customer I/O needs.

The **Model 71810** can be populated with a range of Kintex UltraScale FPGAs to match specific requirements of the processing task, spanning from the entry-level KU035 (with 1,700 DSP slices) to the high-performance KU115 (with 5,520 DSP



slices). The KU115 is ideal for demanding modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

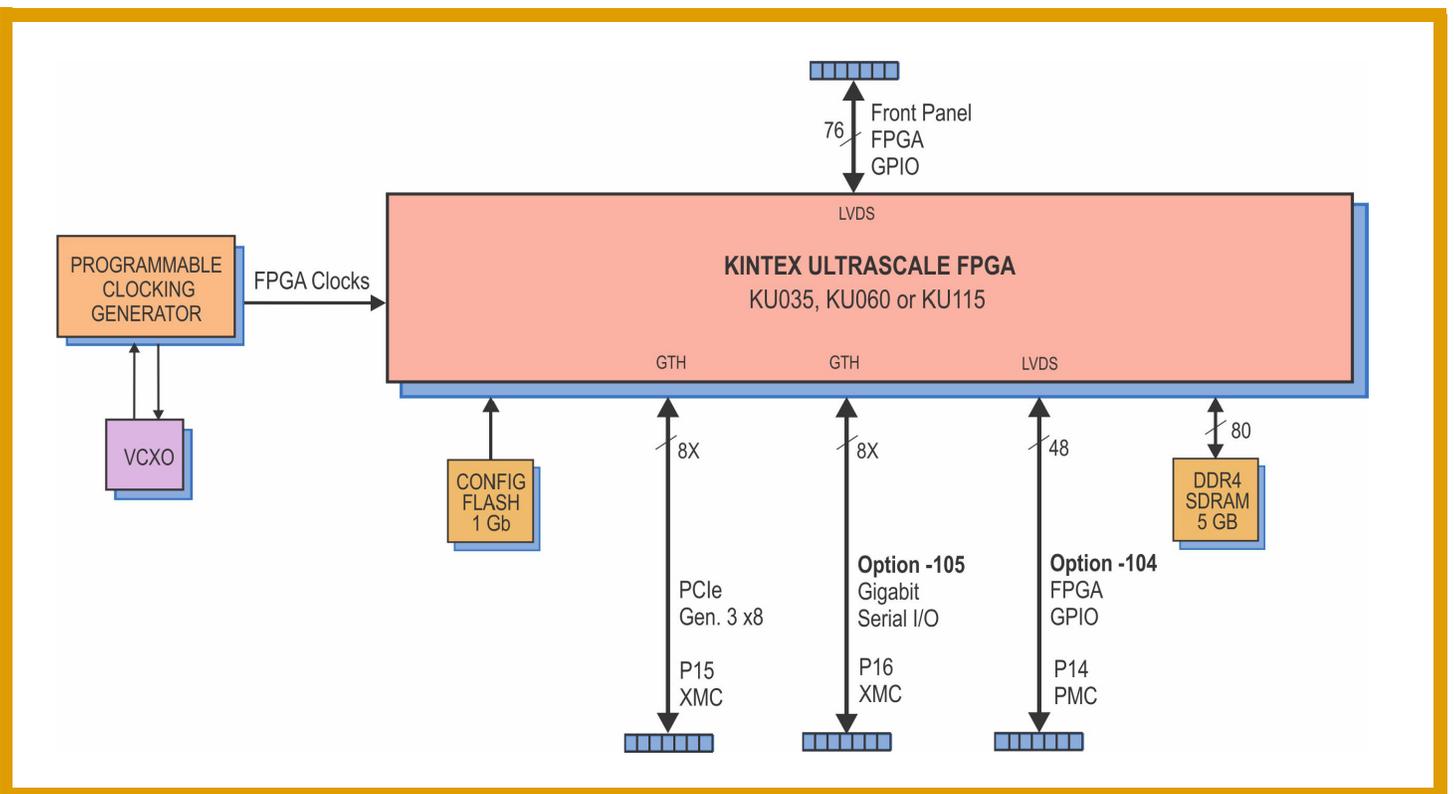
The Model 71810 can be optionally configured with a P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O to the carrier board

or backplane. An additional option for a P16 XMC connector with an 8X gigabit link to the FPGA supports serial protocols.

With the Xilinx Kintex UltraScale FPGA, LVDS digital I/O and gigabit serial I/O, the Model 71810 becomes an excellent high-performance off-load co-processor to fit a wide assortment of processing needs in the most demanding of applications.

### The Jade Architecture

The Pentek Jade architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by over 50% with equally impressive reductions in cost, power dissipation and weight. Its PCI Gen.3 interface allows access to control and status registers for controlling algorithms, state machines, and data flow across the LVDS I/O front panel and carrier board interfaces. A 5 GB bank of DDR4 SDRAM is available for additional functions. The factory-installed DMA controller can sustain 6.4 GB/s data transfers across PCIe. ➤





**Model 71810**

## Navigator Design Suite for Streamlined IP Development

Pentek's Navigator<sup>®</sup> Design Suite was designed from the ground up to work with Pentek's Jade architecture and Xilinx's Vivado Design Suite<sup>®</sup> providing an unparalleled plug-and-play solution to the complex task of IP and control software creation and compatibility. Graphical design entry for Xilinx and Pentek AXI4-compliant IP modules using the Xilinx IP Integrator greatly speeds development tasks.

The Navigator Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and Navigator BSP (Board Support Package) for creating host applications. Users can work efficiently at the API level for software development and with an intuitive graphical interface for IP design. The Navigator BSP is available for Windows and Linux operating systems.

### For More Information ...

For more information about **Model 71810**, [click here](#). You also can email us at [sales@pentek.com](mailto:sales@pentek.com), contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. □

## Pentek's Jade Architecture SOSA™ Aligned LVDS XMC Module with Optical I/O



Pentek's other new Jade family product is also an LVDS XMC module. However, the **Model 71813** is designed to meet the requirements of emerging standards from The **Open Group Sensor Open Systems Architecture (SOSA™)** Consortium of which Pentek is a member. The Model 71813 is also the industry's first such XMC to implement an optional front panel optical interface supporting four 12 Gbps lanes to the FPGA.

The Model 71813 routes 28 pairs of LVDS connections from the FPGA to the XMC P16 connector for custom I/O. When mounted on a compatible single board computer, the Model 71813 provides a customizable I/O signal status and control interface. In the case of a VPX implementation, the I/O is routed to the backplane where it can handle control and command signals to the chassis being defined in the evolving SOSA initiative.

*"Model 71813 directly addresses I/O needs called out in the emerging SOSA standards,"* said Paul Mesibov, Pentek's chief technical officer and SOSA standard contributor. *"Pentek is working with other SOSA members and is committed to lending our experience in meeting open system architecture challenges."*

The Model 71813 can be optionally configured with a front panel MPO optical connector for supporting four lanes of 12Gbps to the FPGA. With user-installed FPGA IP, the Model 71813 can be used as an optical interface for 10GigE, 40GigE, Aurora or custom protocols.

With the Xilinx Kintex Ultrascale FPGA, LVDS digital I/O and optical I/O, the **Model 71813** becomes an excellent

high performance off-load co-processor to fit a wide assortment of processing needs in the most demanding of applications.

## Customer Adoption and Applications

The Model 71813 is already being used by Kontron, a leading global provider of IoT/Embedded Computing Technology, with their new VX305C-40G 3U VPX single board computer (SBC). These products were developed in alignment with the SOSA technical standard and designed specifically to meet the needs of the U.S.

defense community in their drive for Open System Architecture (OSA) computing platforms.



*"Herrick Technology Laboratories, Inc. of Germantown, MD, and another major U.S. system integrator have received shipments of this Kontron SBC for U.S. defense community applications,"* said Mark Littlefield, Kontron's vertical product manager for Defense and SOSA standard contributor. He added, *"Herrick is integrating the VX305C-40G SBC with a Model 71813 XMC board from Pentek, which will provide customizable I/O signal status and control for their new SOSA C4ISR demonstrator system for the U.S. Army."*

For a description of the **Jade architecture** and **Navigator Design Suite**, refer to those topics in the Model 71810 article. For more information about **Model 71813**, [click here](#). You also can email us at [sales@pentek.com](mailto:sales@pentek.com), contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. □

## Pentek Expands the Talon Extreme Rugged 1/2 ATR Recorder Family

Pentek recently added a new model to the Talon RTX 25xx series, a new high-performance **small form factor (SFF)** recorder product line for extreme operating environments. Optimized for SWaP (size, weight and power), the rugged sealed 1/2 ATR recorders are available with multiple input options and up to 30.7 TB of removable SSD storage. These SFF recorders provide real-time streaming data rates up to 4 GB/s for multi-channel, wide bandwidth RF signal recording.

The **Model RTX 2590** provides eight phase-coherent 250 MHz 16-bit A/D channels, for recording up to 100 MHz of RF/IF signal bandwidth per channel with excellent dynamic range. It can sample RF/IF signals up to 700 MHz and provides digital downconverters (DDCs) with output bandwidths selectable from 5 kHz to 100 MHz.



*“Our new extremely rugged 1/2 ATR recorder provides real-time sustained recording rates up to 4 GB/s,”* said Chris Tojeira, Recording Systems director, Pentek. He added, *“We can capture the full bandwidth of all eight 250 MHz 16-bit phase-coherent A/Ds in this single compact chassis.”*

### Extremely Rugged, Sealed Design

Engineered to operate in the toughest environments with high levels of shock and vibration, the RTX recorder's chassis keeps all electronics sealed from the external environment. The 1/2 ATR chassis uses military standard circular I/O connectors to control RF emissions while protecting the recorder's electronics from humidity, water, dust, sand, and salt fog.

The Talon RTX SFF chassis further seals the internal electronics from the outside environment by extracting heat through conduction to an air-cooled inner plenum. A thermostat-controlled, removable fan pulls air into the front of the chassis, through the plenum and then out the back of the chassis. Only the fan is exposed to the outside environment, assuring all system electronics are protected in the sealed chassis. The inner plenum can be replaced to provide other cooling options, such as liquid or conduction cooling.

Designed to operate from -40° C to +55° C, these recorders can handle most thermal environments, making them ideal for UAVs, aircraft pods, tight equipment bays, military vehicles, and most outdoor environments. ➤



## High-Speed Data Storage and Security

Pentek's QuickPac® drive pack is easily removed from the recorder via a set of captive thumb screws on the front panel. An empty QuickPac drive pack can replace a full one for short down times and extended missions. A companion offload system for the QuickPac drive pack is available so the recorder can be redeployed while the recorded data is transported and reviewed via the offload system at a ground facility. The QuickPac drive pack holds up to 30.7 TB of SSD data storage and supports RAID levels 0, 5, or 6.

For secure applications, a separate operating system drive can be removed, allowing users to extract all non-volatile memory from the system in just a few seconds.



### Development Tactics and Techniques for Small Form Factor RF Signal Recorders

This white paper describes engineering considerations and design techniques used to develop small form factor rugged recorders that can handle extremely high data rates associated with very wide bandwidth RF signal recording.

It is intended to provide engineers with ideas on how to bring this capability into confined and often extreme environments while focusing on military specification compliance, SWaP and ease of use with confidence.

To download it, click [here](#).

## Mission Computer Capable

Talon RTX 25xx series recorders with the Intel Core i7 7700K, 7th Generation Quad Core 4.2 GHz processor and 8 GB DDR4 DRAM, are expandable to 16 or 32 GB with enough processing power to act as the primary mission computer when needed. Utilizing the processing power adds slightly to the power budget, but delivers state-of-the-art processing for mission applications and control.

## Ease of Operation

Pentek's SystemFlow® software interface is integrated into every Talon recorder. The software includes the graphical user interface (GUI) that is used to control the recorder with point-and-click configuration management, a client/server communication interface. NTFS file system support and an application programming interface (API) for custom user applications and control. Signal analysis tools include a virtual oscilloscope, spectrum analyzer, and spectrogram to monitor signals before, during and after data

collection. The system can be controlled remotely via the Gigabit Ethernet interface available on one of the MIL-STD circular connectors.

## Available Options and Simulation Package

The Talon SFF recorders offer an optional GPS receiver for precise time and position stamping. Additional QuickPac drive packs with 3.8 to 30.7 TB are available. Computer I/O on all models includes Gigabit Ethernet, USB 3.0, RS-232 and HDMI.

Pentek's SystemFlow Simulator provides a "test drive" of the SystemFlow recording software installed on all Talon recording systems. The simulator allows users to operate the standard GUI and the SystemFlow API.

For more information about **Model 2590**, click [here](#). You also can email us at [sales@pentek.com](mailto:sales@pentek.com), contact **your local representative**, or contact Pentek directly [+1 (201) 818-5900]. □

## OpenVPX Technology: Roadmap to the Future

Thursday, April 25, 2019  
at noon U.S. EDT

The U.S. Department of Defense and other users are demanding the implementation of open standards and interoperability. VPX specifications have largely been focused at the board level, but there is also a need for considering system-level requirements to improve interoperability and reduce customization, testing, cost, and risk. Enter the OpenVPX Systems Specification.

This one-hour Technical Webinar from the editors of Tech Briefs Media will answer two important questions. Where is OpenVPX technology today? And where is it going? An audience Q&A is included.

### Speakers:

- Jerry Gipper, Executive Director, VITA
- Rodger H. Hosking, Vice President and Co-Founder, Pentek Inc.
- Ivan Straznicky, CTO, Advanced Packaging, Curtiss-Wright Defense Solutions

[Click to register](#)

## Rodger Hosking Joins the VITA Board of Directors



VITA, the trade association for standard computing architectures serving critical and intelligent embedded computing systems markets, announced that Rodger Hosking, vice-president and co-founder of Pentek, Inc., was elected to the VITA Board of Directors. With this election, the board will consist of four members.

*"We are very pleased to announce that Rodger has joined the Board of Directors, where his expertise will be a key asset,"* said Jerry Gipper, VITA's Executive Officer. *"Rodger has a solid understanding of the technology and business strategies that drive the critical embedded computing industry. He brings a unique perspective from a smaller company to the board and we look forward to benefitting from his extensive expertise in the industry and management as we continue to execute against our objectives and take action to create value for our members."*

Mr. Hosking is responsible for new product definition, technology development, and strategic alliances at Pentek. With over 30 years in the electronics industry, he has authored hundreds of articles about software radio and digital signal processing. Prior to his current position, he served as engineering manager at Wavetek/Rockland, and holds patents in frequency synthesis and spectrum analysis techniques. He holds a BS degree in Physics from Allegheny College in Pennsylvania and BSEE and MSEE degrees from Columbia University in New York.

### About VITA

Founded in 1984, VITA is an incorporated, non-profit organization of suppliers and users who share a common market interest in critical embedded systems. VITA champions open system architectures. Its activities are international in



scope, technical, promotional, and user-centric. VITA aims to increase total market size for its members, expand market exposure for suppliers, and deliver timely technical information. VITA has Ameri-

can National Standards Institute (ANSI) and International Electrotechnical Commission (IEC) accreditation to develop standards (VME, VXS, VPX, OpenVPX, VPX REDI, XMC, FMC, FMC+, VNX, Reliability Community, etc.) for embedded systems used in a myriad of critical applications and harsh environments. For more information, visit [www.VITA.com](http://www.VITA.com).

## AOC International Symposium & Conference Awards

Military Embedded Systems Chose Pentek as a 4-Star "Best in Show" Winner at the recent AOC Conference!



### Radar & EW Category Winner: Model 6001 RFSoc Quartz eXpress Module

Pentek's new QuartzXM SoM speeds custom deployment of RFSoc in SWaP critical environments. Measuring only 2.5 by 4 inches, the QuartzXM Model 6001 includes all of the circuitry needed to maximize the performance of the RFSoc. The Model 6001 can be housed on the Pentek 3U VPX Model 5950 or it can be deployed on a custom carrier. Pentek's complete design kit ensures success for customers building their own carrier. [Go to product summary.](#)

### White Paper: Strategies for Deploying Xilinx's RFSoc FPGA

Xilinx's new RFSoc brings a powerful and unique solution for addressing some of the most demanding requirements of high bandwidth and high channel count system. This paper provides a look at how RFSoc compares to the current trends in A/D and D/A converters and the strategies for getting the most performance out of this new family of FPGAs. [Download white paper.](#)



For more information, contact [sales@pentek.com](mailto:sales@pentek.com), or call (201) 818-5900.