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High-Speed A/Ds for Wideband Signal Processing Applications Reach 2 GHz

Critical mainstream signal processing applications, such as radar, wireless communications and networks, military radios, satellite communications, and medical imaging, require increasing signal bandwidths to handle new modulation techniques and carry more traffic.

With these large markets driving A/D converter technology towards faster and more accurate devices, wideband A/D converters have made significant advances in the last five years.

Although partly attributable to silicon process improvements, many A/D converter enhancements target specialized features including front-end input amplifiers, sample-and-hold amplifiers, and low jitter clock drivers. Multistage flash conversion techniques benefit from new techniques in digital error code correction and thermal compensation circuitry to help improve bit accuracy, linearity and gain.

Tough Requirements

Board level products using the new A/Ds must not only preserve the signal integrity and performance of these devices, but also effectively deal with the tremendous data rates they produce to support data acquisition, transient capture, data recording, radar processing, image processing, and real-time digital signal processing for software radio.

Most high-speed A/D applications require careful control of data collection for capturing pulse waveforms. Radar signals require external trigger or gate signals that define a precise time window for acquisition.

Beamforming and direction finding systems mandate digitizers with precise channel-to-channel phase alignment between signals from multiple antennas. Phase accuracy in these systems directly impacts signal-to-noise performance and operating range.

The Pentek 68xx series high-speed A/D converters meet all these needs for high-performance VMEbus system applications.

215 MHz A/D Converters

The Model 6821 12-bit, 215 MHz A/D Converter is a 6U VMEbus board with a single AD9430 A/D converter.

It features an extremely wideband input stage and sample-and-hold amplifier for direct IF sampling of input signal frequencies as high as 700 MHz.

The Model 6822 is the dual-channel A/D version shown in Figure 1.

Figure 1. Model 6822

Both boards offer a wealth of resources to cover virtually any high-speed application. As shown in Figure 2, two Virtex-II Pro FPGAs accept data directly from the A/D converters at up to 215 MHz providing several flexible options for dispatching this data.

Raw A/D data can be stored in real time in the two 128 MB SDRAMs, capable of holding up to 128 megasamples. At the full sample rate, each memory accommodates nearly 300 milliseconds of transient signals such as radar pulses.

When implemented as a circular buffer, the SDRAMs provide a digital delay element. In signal intelligence applications, for example, an input signal can be analyzed for content while it is propagating through the delay memory. Based on this analysis, the delayed signal can then be routed for additional processing or simply discarded.

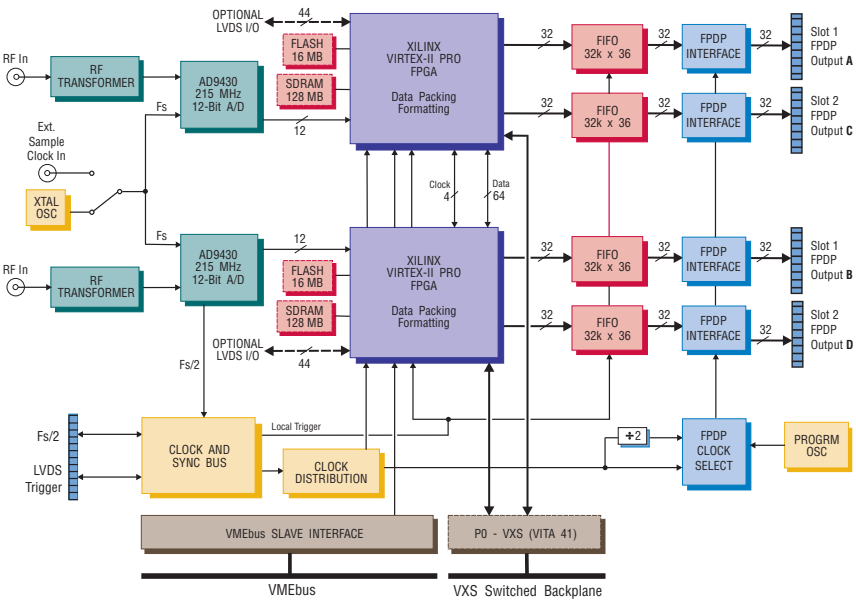

Figure 2. Model 6822 Block Diagram

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The two Xilinx XC2VP50 FPGAs are ideally positioned to perform real-time DSP functions such as the FFT for the signal analysis task described above. With the equivalent of more than 6 million gates, each FPGA can incorporate IP cores for digital downconverters, filters, demodulators, decoders, decryption engines, image processors and more.

Each FPGA is optionally equipped with two FPDP (front panel data ports) interfaces. This popular industry standard is used on hundreds of system components including processors, memory, storage and DSP boards. Compatible with the FPDP-II specifications, each port can send or receive 32-bit data over flat ribbon cable at rates up to 400 Mbytes/sec.

Each FPGA is also optionally equipped with a 40-bit parallel I/O port using LVDS (low-voltage differential signalling) levels delivering data at speeds up to 600 Mbytes/sec. Delivered either over front panel ribbon cable connectors or through the P2 backplane connector, this can be an effective interface to high-speed peripheral subsystems.

Synchronization, gating and triggering functions are all thoroughly addressed with powerful timing circuitry. A front panel LVDS timing bus distributes clock, gate, sync and trigger signals to ensure synchronous operation across multiple boards. Triggering resources include sample counters for capturing a specific number of samples for each trigger event.

Sampling Rates Boosted to 2 GHz

Shown in Figure 3, the new Model 6826 2 GHz Dual-Channel A/D Converter takes a major leap in sampling rates to digitize signal bandwidths of 800 MHz for extremely wideband applications. These include wideband radar and advanced communications systems previously handled by multiple A/Ds handling adjacent slices of the frequency band.

Using the new AT84AS008 2.2 GHz 10-bit A/D Converter recently announced by Atmel, the 6826 faces an even greater challenge in handling data rates than the 6821 or 6822. As a result, some architectural changes are required, as shown in Figure 4.

Immediately following each A/D converter is an 8-to-1 demultiplexer circuit that accepts 8 consecutive 10-bit samples from the A/D and packs them into an 80-bit word for delivery to the FPGA. This packing reduces the data clock by a factor of 8 to a more reasonable 250 MHz which can be accommodated by the FPGA.

Figure 3. Model 6826

The FPGA on the Model 6826 is the XC2VP70 or XC2VP100 device with the equivalent of 11.3 million gates, offering a significant resource for real time signal processing. Like the 6821 and 6822, it's also equipped with memory, FPDP interfaces and LVDS interfaces for efficient data handling.

SDRAM memory is enhanced in three ways: double data rate (DDR) devices are used, the data bus width is doubled to 64 bits, and the size is quadrupled to 1 GByte. These changes support real-time storage of 500 milliseconds of 8-bit data samples in memory at the full 2 GHz rate for transient capture and delay functions.

At these frequencies, multiboard synchronization is difficult due to the extremely high clock speeds. A special timing system on the 6826 uses front panel coaxial connectors for clock, gate, trigger and sync signals. Phase alignment between boards for the clock and the other data collection signals is accomplished with precision phase adjust circuits controlled and calibrated by software during system initialization.

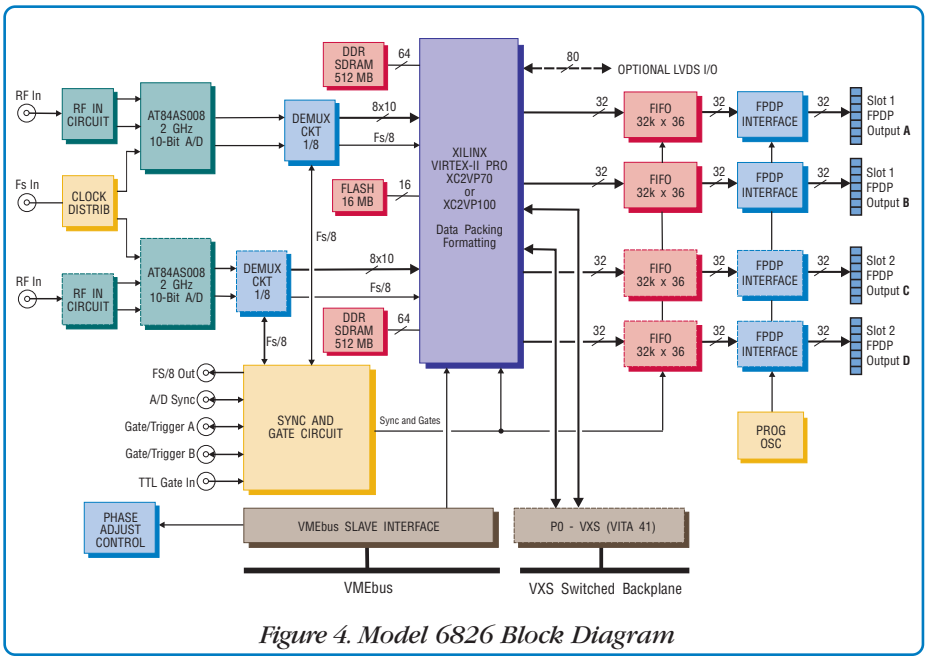

Figure 4. Model 6826 Block Diagram

VXS Switched Serial Fabric Interface

Covered fully in the Summer 2003 issue of The Pentek Pipeline and available online at pentek.com/go/pipevxs, VXS is a new multigigabit switched serial fabric standard defined in the VITA 41 specification. It connects VMEbus boards across new ➤

Comprehensive Software Radio Transceiver CompactPCI Boards

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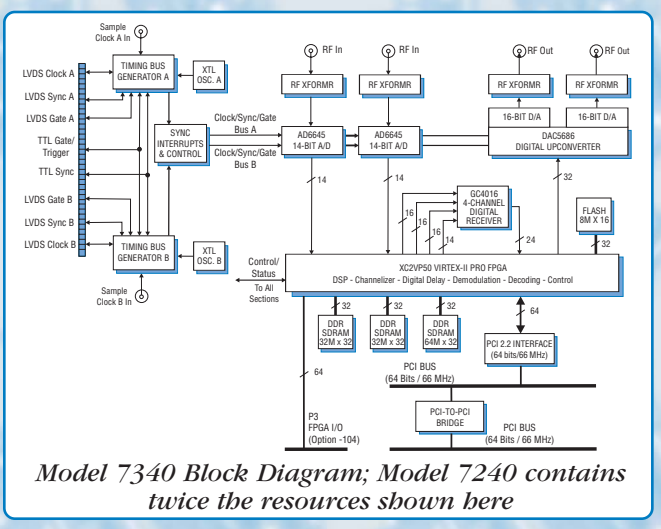
Because the FPGA controls the data flow within the board as well as providing signal processing, the board can be configured for many different functions. In addition to acting as a simple transceiver, it can perform user-defined DSP functions on the baseband signals, developed using Pentek's GateFlow and ReadyFlow development tools.

Digital Up/Downconverters

The board includes two TI/Graychip GC4016 quad digital downconverters along with two TI DAC5686 digital upconverters with dual D/A converters. Each channel in the downconverter can be set with an independent tuning frequency and bandwidth. The upconverter translates real or complex baseband signals to any IF frequency from DC to 160 MHz and can deliver real or complex (I+Q) analog outputs through its four 16-bit D/As. The upconverter can be bypassed for interpolated D/A outputs with sampling rates to 500 MHz.

Synchronization

A clock/sync bus allows synchronization of local oscillator phase, frequency switching, decimating filter phase and data collection among multiple 7240s. One board acts as a master driving clock, sync and gate signals out to a front panel flat cable bus using LVDS differential signaling. The master alone can drive as many as seven slaves. By using a Pentek Model 9190 Clock and Sync Generator to drive these signals, as many as forty boards can be configured to operate synchronously.



Model 7340 Block Diagram; Model 7240 contains twice the resources shown here

Model 7340 is a 3U cPCI dual version of the 7240. It offers one-half the resources of the 7240.

For more information on these transceivers visit pentek.com/go/pipe7240 or penek.com/go/pipe7340. ❑

➤ backplane links and delivers several orders of magnitude improvement in aggregate data rates to meet the needs of advanced high-performance systems.

In all of the 68xx A/D boards, RocketIO gigabit serial interfaces on the FPGA implement dual 4x switched serial fabric ports to the new P0 Multi-Gig RT2 backplane connector defined in the VXS specification. Each 4x port uses four ganged serial bit lines for input and four more for output. With each serial line operating at clock rates up to 3.125 GHz, each full-duplex 4x port delivers data transfer rates of up to 1.25 GBytes/sec simultaneously in each direction.

Because VXS interfaces are implemented within the FPGA, any of the popular fabric protocols (including Serial RapidIO, PCI Express, Infiniband, etc.) can be accommodated by installing the appropriate IP core. For point-to-point connections, the lightweight Aurora link layer protocol from Xilinx is also available.

For more information about any of these exciting new products, simply visit our website at pentek.com and enter the Model number in the search window or call us at 201-818-5900. ❑

New Handbook is Now Available

Because of data throughput limitations, the most difficult problem for designers of high-performance real-time digital signal processing systems is simply moving data within the system. With new high-performance A/Ds in the GHz range, board designers need new strategies to eliminate bottlenecks. This handbook speaks to the innovative ways to capture, process and store data for high-speed applications. Data flow options, memory optimization, FPGA usage, VXS, serial fabrics and other solutions will be discussed.

To keep data flowing with the array of high-powered solutions outlined in this new handbook, download *"Critical Techniques for High-Speed A/D Converters in Real-Time Systems"* today at pentek.com/go/pipeAD. ❑

Helpful System Design Reference Documents on the Web

- Pentek "Central" Sites: on the left bar of the Pentek homepage pentek.com highlight Products by Function and then make your selection. This will bring you to a summary page outlining real-life customer applications, brochures, handbooks, overviews, tutorials, webcasts, white papers and product offerings. For example, "I/O Central" includes tutorials such as *"Putting Undersampling to Work", "FPGAs Tackle DSP Applications for Communications"* and many more...
- I/O Selection Guide: Pentek offers more than 60 I/O products. This chart outlines and compares specs for our latest I/O boards; go to pentek.com/go/ioselect. If you don't see the product you need, go to pentek.com/go/suggest and submit a product suggestion.
- Manuals, FAQs and white papers are also available to registered users. ❑

Product Focus

Models 7240, 7340

Pentek Offers CompactPCI Software Radio Transceivers

Quad or Dual Units with 14-bit 105 MHz A/Ds and FPGAs

Model 7340 is a dual digital up/ downconverter in 3U cPCI format

Model 7240 is a quad or dual digital up/ downconverter in 6U cPCI format

Features

- Available in 6U (Model 7240) and 3U (Model 7340) cPCI formats
- Quad or dual digital upconverter/ downconverter handles 40 MHz bandwidth RF or IF signals
- Configurable data routing puts FPGA processing in the baseband data stream
- Dual timing buses for independent input and output clocks
- LVDS clock/sync bus for multiple module synchronization
- Up to 1024 MB memory to buffer data for digital delay or data capture
- Compatible with Pentek GateFlow® IP Cores and FPGA Design Tools
- Pentek ReadyFlow® Board Support Libraries for quick board setup

The Model 7240 CompactPCI board combines both transmit and receive capability with two high-performance Virtex II-Pro FPGAs.This board is also available in a variety of form factors including PCI (Model 7640) and a PMC/ XMC commercial or conduction-cooled version (Model 7140).

The front end accepts four +4 dBm full-scale analog RF inputs and transformer-couples them into four 14-bit A/Ds sampling at up to 105 MHz. The digitized output signals pass to two Virtex-II Pro FPGAs for signal processing or routing to other board resources. These include two quad digital downconverters, two digital upconverters with dual D/As, 1024 MB DDR SDRAM delay memory and the PCI bus. The FPGAs also serve as control and status engines with data and programming interfaces to the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Application-Ready Systems

If you need a system that's ready for your application development, go to pentek.com/go/piperts for our latest real-time signal processor and recorder development systems.

Our RTS offerings are highly scalable embedded systems for acquiring, downconverting, upconverting, processing, analyzing and recording a wide range of signals.