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Georgia Tech Develops a Software Radio Platform for Wireless Communications

Researchers at the Georgia Institute of Technology have been collaborating in the development of a wireless prototype test system in a program supported by the Georgia Electronics Design Center (GEDC) and the Georgia Research Alliance. The goal of this investigation is to demonstrate the feasibility of Gigabit wireless communications.

The research team has made major advances towards this goal by using a programmable software radio testbed to implement Multiple Input Multiple Output (MIMO) systems employing Orthogonal Frequency Division Multiplexing (OFDM). MIMO systems utilize multiple antennas at the transmitter and receiver to achieve increased data throughput in high-speed data applications. In an OFDM system, a single high-speed bit stream is separated into several low-speed bit streams, with each of the slower bit streams used to modulate one of several carriers.

Key subsystems integrated into the testbed include smart antennas with switched element architecture and with provision for switched beams; wideband digital downconverters; wideband digital upconverters; wideband A/Ds and D/As; signal processor boards; I/O interfaces to PCs; and FPGAs for more computationally-demanding algorithms such as Forward Error Correction (FEC) coding/decoding and matrix inversion.

For more information on MIMO systems see The Pentek Pipeline Summer 2001 issue, *Smart Antenna Experiments for 3G and 4G Cellular Systems*. For more information on OFDM, see the Spring 2001 issue, *AT&T Labs-Research Designs a Broadband Radio Link for Internet Access*.

The programmable software radio testbed is housed in the VMEbus enclosure shown in Figure 1. With the exception of RF and IF sections, the signal processing boards in the enclosure are from Pentek.

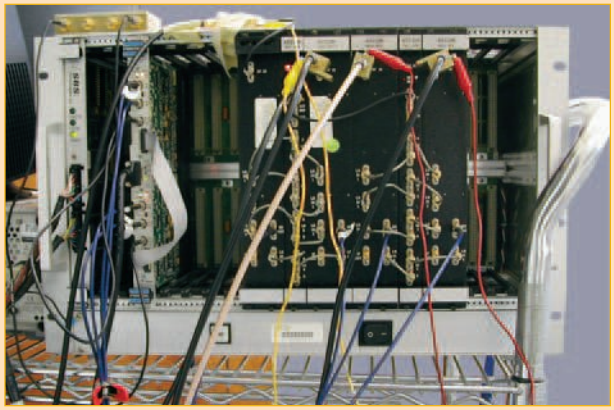

Figure 1. Software Radio Testbed (Courtesy of Georgia Tech)

The testbed is used in two distinctly different modes of operation:
I. Real-time data capture and offline processing and analysis.
II. Wireless Gateway between two Ethernet networks.

Operating Mode I

Mode I serves as a means to efficiently conduct wideband wireless testing to evaluate antenna selection algorithms, MIMO antenna designs, and receiver processing algorithms such as channel estimation, signal detection, synchronization, demodulation and decoding.

In addition, this mode permits the demonstration of high bit rate communications using arbitrary waveform generators at the transmitter and wideband multichannel digital downconversion and recording for offline processing at the receiver.

This mode has the advantage of offering a highly flexible and convenient architecture to test a broad range of waveforms and receiver processing algorithms, without the time-consuming tasks associated with developing real-time implementations of the desired algorithms in DSPs or FPGAs.

Currently the system operates in a 4x4 configuration (4 transmit x 4 receive antennas), with a spectral occupancy ➤

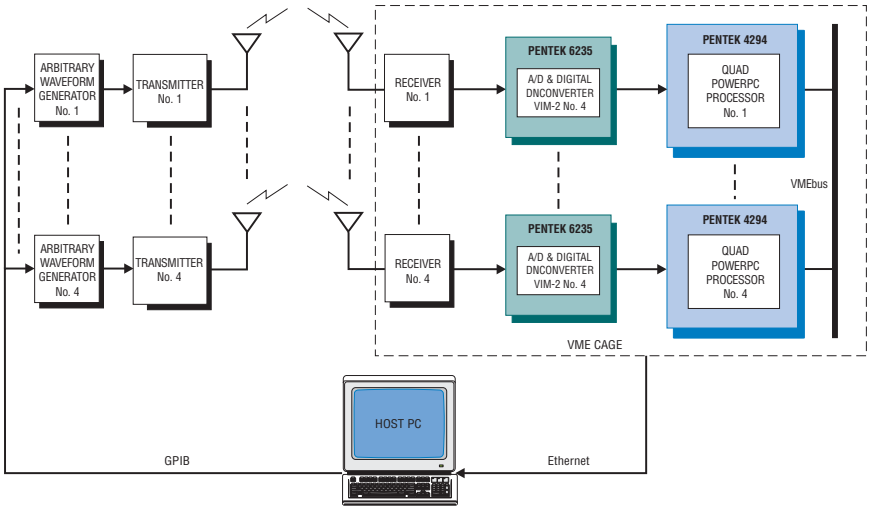

Figure 2. Software Radio Testbed in Mode I, 4 x 4 MIMO Data Capture

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of 28 MHz yielding peak bit rates of 672 Mbps. The goal of future development is to extend the system bandwidth to 40 MHz and achieve peak bit rates of 960 Mbps.

Signal Processing

In Mode I operation, the system employs synchronized arbitrary waveform generators to create spatially multiplexed data streams which have been optionally encoded using FEC coding schemes and Quadrature Amplitude Modulation (QAM) signaling constellations of OFDM subcarriers.

As shown in Figure 2, the waveform generators upconvert the complex baseband signals to the RF carrier frequency. They can then replay the sampled data at variable rates to achieve the desired modulation, width and data transmission rate. Data captured in the Pentek 4294 Quad PowerPC Processor boards is transferred to a PC for offline processing and analysis.

Operating Mode II

In the second mode, the testbed operates as a Wireless Gateway between two Ethernet networks. It incorporates physical layer, Media Access Control (MAC) layer, TCP/IP and application layer functionality. MAC is a hardware address that uniquely identifies each node of a network.

As shown in Figure 3, the system block diagram includes Ethernet hubs to independent networks; PCs providing MAC functionality; VME systems serving as physical layers; and host PCs at both ends of the wireless gateway. The system supports multiple servers and clients. Utilizing TI DSP Processors, the system has achieved real-time speed with testbed sampling rates of 8 MHz.

Real-time Data Flow

Multiple clients on one network can access servers on a separate network through the wireless gateway by generating a request on the associated client host PC. The request is passed via Ethernet through the hub to the terminal of the wireless gateway. The MAC layer in the gateway strips the Ethernet header and adds a header for the gateway. A preamble that permits packet detection, synchronization, channel estimation and demodulation at the receiving terminal of the wireless gateway is added by the DSP processor prior to transmission.

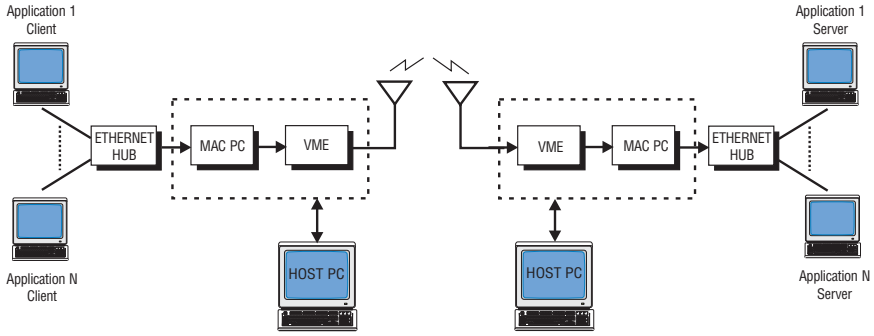


Figure 3. Software Radio Testbed in Mode II, Wireless Gateway

At the receiving end, demodulated data packets are reformatted for Ethernet transmission, forwarded to the Ethernet hub, and routed to the appropriate server.

Transmitter Signal Processing

The baseband processing at the transmitter includes QAM mapping, space-time coding and OFDM signal generation. As shown in Figure 4, this processing is achieved in the Pentek Model 4291 Quad C6701 DSP Processor board and associated VIM-2 modules.

Forward Error Correction coding and decoding can be integrated using the FPGAs of the Pentek 6250 Configurable Logic FPGA VIM-2 module. Cores for Reed Solomon coding and decoding have been successfully implemented in the user block of the 6250 FPGA. In their present configurations, the coder and the decoder can accommodate data rates up to 240 Mbps.

Two of the four DSPs perform the QAM and space-time coding, while the other two perform an inverse Fast Fourier Transform (IFFT) and add the information necessary to enable proper processing by the receiver. The I and Q outputs of the 4291 are then upconverted to IF by a Pentek Model 6229 Digital Upconverter VIM-2 module with dual D/A converters.

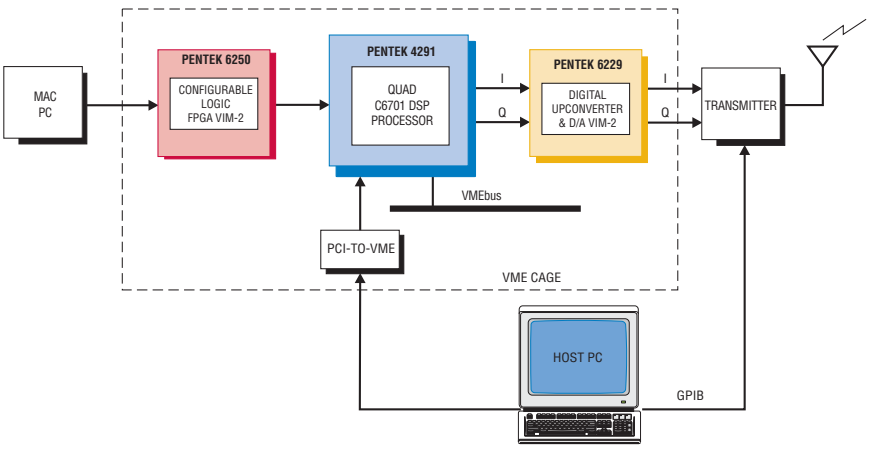


Figure 4. Wireless Gateway Transmitter Signal Processing

16 or 32-Channel Multiband Digital Receiver cPCI Boards

[From page 4]

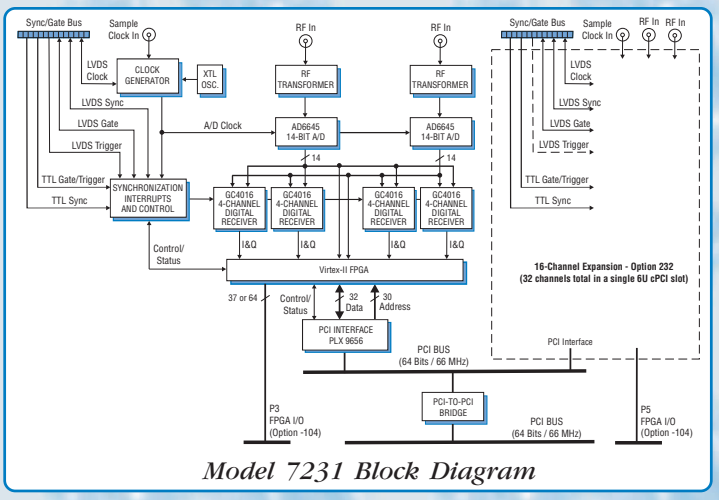
configured to perform various modes of data packing, data formatting and channel selection. Dual port memories in the FPGAs provide efficient cPCI bus transfers by buffering receiver and A/D data. The A/D outputs may also be delivered directly to the FPGAs for processing wideband data.

Output Bandwidth

With a 100 MHz clock, the usable bandwidth of each receiver channel is 2.5 MHz. However, users can take advantage of the GC4016 channel combining mode to join two or four receiver channels into a single channel with 5 or 10 MHz resulting bandwidth.

cPCI Interface

The FPGA outputs are connected to a pair of 66 MHz, 64-bit cPCI interfaces capable of 528 MB/sec peak data rates. Industry standard PLX9656 interface chips ensure full conformance to all cPCI bus timing specifications. A PCI bridge connects the two interfaces to the cPCI backplane.



Model 7231 Block Diagram

Synchronization

The front panel clock and sync bus allow one 7231 to act as a master for synchronizing multiple slave boards. Up to 1280 channels may be synchronized with the Pentek 9190 Clock and Sync Generator.

Configurations

Model 7231 is optionally available as a 16-channel unit in 6U cPCI format. The Model 7331 offers 16 channels in 3U format.

For more information on the Models 7231 and 7331 Multiband Digital Receivers, visit pentek.com/go/pipe7231 and pentek.com/go/pipe7331.These receivers are also available in PMC (Model 7131) and PCI (Model 7631) formats. ❑

Receiver Signal Processing

As shown in Figure 5, the receiver end complements the processing at the transmitting end. A Pentek Model 6235 A/D and Digital Downconverter VIM-2 module receives the IF signal from the RF receiver and downconverter. A Pentek Model 4291 Quad DSP processor performs a forward FFT to convert the received time domain signal back to the frequency domain. Channel estimates, demapping and data transfers are also performed by this processor. When FEC is employed, a Pentek 6250 with the Reed Solomon decoder core can be added to the processing chain.

The output is then transferred through to the wireless gateway PC for MAC coding and decoding and subsequent transfer to the Ethernet hub and the corresponding server.

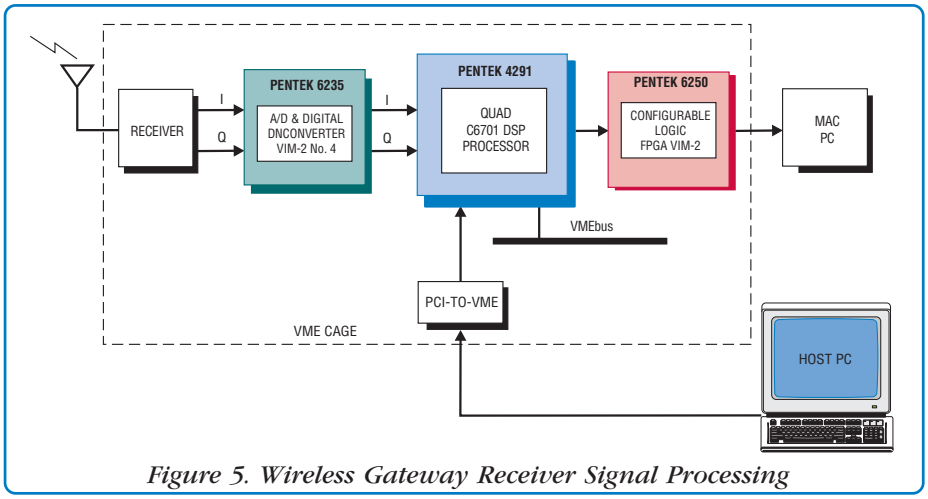


Figure 5. Wireless Gateway Receiver Signal Processing

Software

Among others, the application software includes the Pentek SwiftNet DSP Networking and Communication Software, MPI Software Technology's VSI/Pro, the Texas Instruments Code Composer Studio and the Wind River Tornado Tools. Also included are the Pentek ReadyFlow Board Support Libraries and the Pentek GateFlow FPGA Design Kit.

Future Work

Work on the wireless gateway is proceeding toward the development of a real-time system with 20 MHz sampling rate that could eventually achieve peak bit rates of 384 Mbps in the physical layer. This system will utilize the Pentek 4294 PowerPC processor and the higher speed Pentek Model 6228 Quad Digital Upconverter and D/A VIM-2 module.

For more information on MIMO research conducted at the Georgia Tech Software Radio Lab, contact Dr. Thomas G. Pratt at the Information and Technology Telecommunication Laboratory at the Georgia Tech Research Institute, thomas.pratt@gtri.gatech.edu. ❑

Product Focus

Models 7231, 7331

Pentek Introduces cPCI Multiband Digital Receivers: Up to 32 channels with 14-bit 100 MHz A/Ds and FPGAs

Model 7331 offers 16 digital receiver channels with a Virtex-II FPGA.

GateFlow

Model 7231 offers 32 multiband digital receiver channels with two Virtex-II FPGAs.

Features

- Available in 6U (Model 7231) and 3U (Model 7331) compact PCI (cPCI) formats
- Includes four or two 80 or 100 MHz A/D converters
- 5 kHz to 10 MHz output bandwidth with 100 MSPS sampling
- 250 MHz input bandwidth
- User-configurable Xilinx Virtex-II FPGAs
- Compatible with Pentek GateFlow® IP Cores and FPGA Design Tools

The new 32-channel 6U cPCI board features eight quad multiband digital receivers, two Virtex-II FPGAs and four 14-bit 80 or 100 MHz A/D converters for signal processing. It accepts four analog inputs at +4 dBm full-scale into 50 ohms on front panel SMA connectors.

The sampling clock can be driven from an internal 80 or 100 MHz crystal oscillator, or from an external clock.

Digital Receivers

The 7231 includes eight TI Graychip GC4016 quad multiband digital receiver chips. Each device includes four receiver channels capable of center frequency tuning from DC to $f_s/2$ where f_s is the sample clock frequency.

Each chip accepts two out of the four possible A/D converter outputs. An onboard crossbar switch allows the first 16 receiver channels to select either of the first pair of A/D outputs. The second group of 16 receiver channels select from either output of the second pair of A/Ds.

Configurable FPGAs

The receiver outputs are delivered to two Virtex-II FPGAs which are ➤