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Single Board Computer Excels in High-Speed Recording System

Single Board Computers (SBCs) are rapidly redefining their traditional roles in embedded VMEbus systems. Instead of simply providing the basic Slot-One functions, SBCs are now invading entirely new classes of tasks.

With the advent of new high-speed system interfaces, denser memory, faster processors, and programmable logic, a single SBC can now tackle demanding applications that previously took up a significant percentage of the card cage hardware.

Evolution of SBC Technology

Early SBCs using Motorola's 68K family, devoted a significant portion of the board to discrete bus interface chips that buffered 68K processor data, address and control lines to the backplane. Other major sections of these early boards were dedicated to bus management, memory chips and memory controllers, disk controllers, UARTs and Ethernet interfaces.

In the late 1980s, a major development was the advent of VMEbus interface chip sets that encapsulated all VMEbus signal and interface functions into just a few ASICs. The chip sets saved significant real estate and boosted interoperability among board vendors.

Since the 68K, different types of microprocessors, microcontrollers, DSP and RISC processors have been used as SBCs for VMEbus. Because external data, address and control signals for virtually all modern processors are radically different from the legacy 68K definitions for VMEbus, the need for an efficient interface to the backplane became apparent.

Toward this end, the PCI bus became eminently suitable. By acquiring a bridge to the PCI bus, processors could gain access to high-volume, low cost peripherals. A new class of PCI-to-VMEbus bridge chips by Tundra soon became the defacto industry standard and improved vendor interoperability and performance.

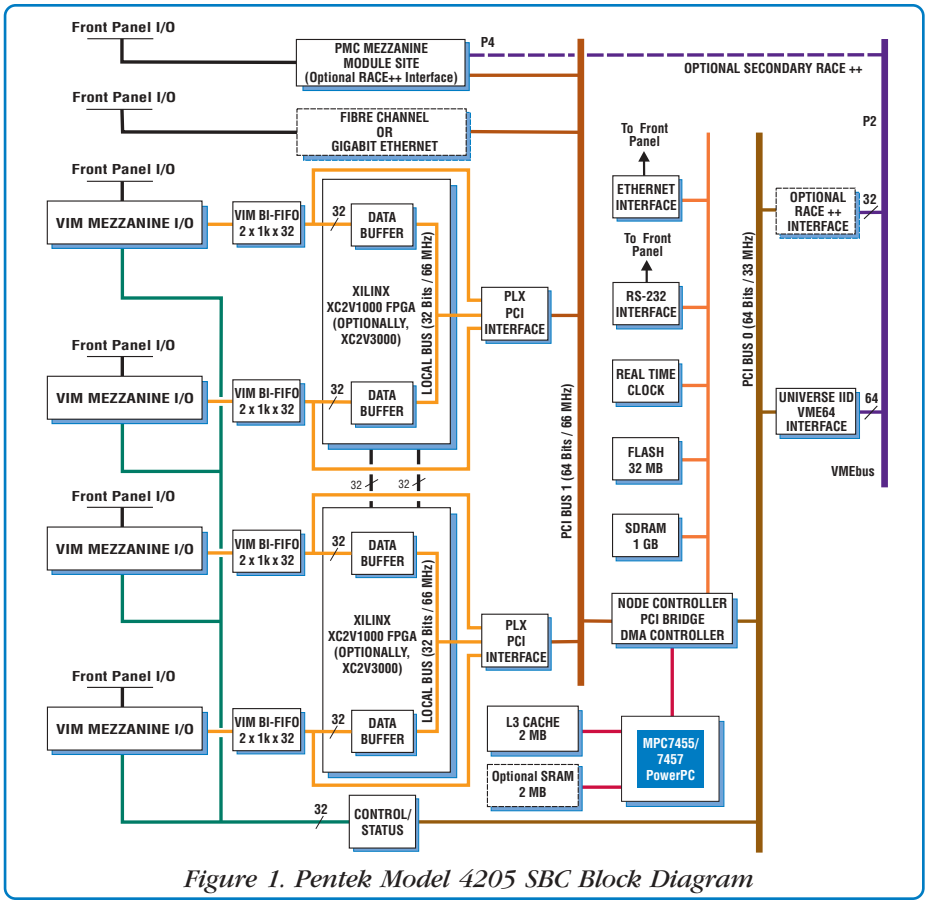

Figure 1. Pentek Model 4205 SBC Block Diagram

Single-chip ASIC PCI bus solutions for a wide range of SBC peripheral functions are now available for Fibre Channel, Gigabit Ethernet, RACEway, Firewire, ATA disks, modems, and a wide range of audio and video standards.

Leading the pack today in processors for embedded system SBCs is the PowerPC. Originally developed as a workstation processor for Apple, the PowerPC soon began proving its worth in real-time VMEbus applications. After the introduction of the G4 PowerPC with its powerful AltiVec vector processing engine, the PowerPC began earning its stripes as a DSP.

Since the G4 PowerPC features a general purpose 64-bit system bus, chip vendors like Marvell introduced system controller ASICs. These devices match the PowerPC system bus to SDRAM, a local bus, and one or two PCI buses. An onboard PCI bus offers an ideal link to the latest PCI-to-VMEbus interface bridges greatly simplifying PowerPC SBC board designs.

Another recent introduction is the Marvell Discovery II System Controller that supports the latest PowerPCs with dual PCI-X bus interfaces, three Gigabit Ethernet ports, a 72-bit DDR SDRAM controller and four DMA channels.

Some of the latest SBCs are now sporting FPGAs to provide custom ➤

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reconfigurable hardware for extra features. Specialized hardware interfaces, multiplexers/demultiplexers, decoders/encoders, etc. are all candidate tasks. Equipped with millions of user-programmable gates, hundreds of hardware multipliers and generous on-chip memory, the latest FPGAs are ideally suited for intensive, dedicated digital signal processing functions.

SBC Board Example

A current SBC product illustrating many of these technology trends is the Pentek Model 4205 G4 PowerPC I/O Processor shown in Figure 1. It includes all the standard Slot-One functions for VMEbus plus 100 BaseT and RS-232 ports for direct connection to a host. It runs a compact kernel OS to support booting and TCP/IP stack management.

A Discovery system controller ASIC links the 1 GHz MPC7457 PowerPC to two 64-bit PCI buses and up to 1 GB of global SDRAM. PCI Bus 0 operates at 33 MHz for compatibility with two PCI bridge ASICs: a Universe IID chip for VME64 backplane access and an optional PXB++ chip to handle RACE++ fabric access.

PCI Bus 1 operates at 66 MHz and supports three major resources:

- A 64-bit 66 MHz PMC mezzanine module site for a wide range of peripheral I/O functions.
- A 2 Gbit/sec serial interface module for front panel high-speed networks and peripherals.
- Two Xilinx Virtex-II FPGAs with up to three million system gates each.

Two high-performance VIM-2 modules can be attached to the Model 4205 I/O Processor. They deliver four 32-bit data streams, at up to 400 MB/sec each, through bidirectional FIFOs directly into the two FPGAs. Depending on the application, data is either passed directly through the FPGAs to PCI Bus 1 or processed inside the FPGA before delivery to the PCI bus.

Equipped with all these new features, this SBC can support a wide range of single-board solutions for high-performance applications.

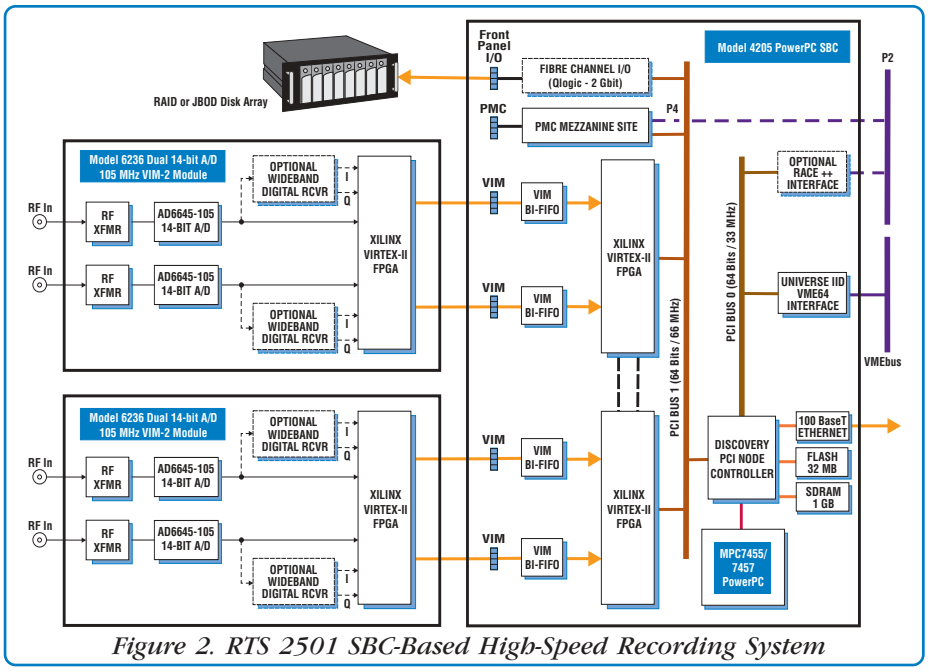

Figure 2. RTS 2501 SBC-Based High-Speed Recording System

High-Speed Recording System

As an illustration of an SBC-based system, consider a real-time data acquisition and recording application for a flyby test of a new airborne radar system. The mission requires digitizing four analog signals, each with 8 MHz bandwidth, and then storing them continuously onto disk for 10 minutes. Once the start command gets issued by the test engineer, it is imperative that no data be lost until the aircraft has completed its complex and expensive maneuvers over the test site.

The system architecture must be derived by first defining the data acquisition parameters. To avoid aliasing, an analog signal should be digitized by an A/D converter operating at a sampling rate greater than approximately 2.5 times its bandwidth. In this case, the 8 MHz bandwidth signals require a 20 MHz sampling rate. Since 14-bit A/D converters are desired to preserve signal quality, two bytes are allocated for each sample, thereby resulting in a 40 MB/sec data rate at the output of each A/D converter.

With four A/Ds, the four-channel system needs a total of 160 MB/sec of recording bandwidth to disk. Total storage capacity of the system for 10 minutes of recording is 10 x 60 sec x 160 MB/sec = 96 GBytes. Including allowance for overhead, a comfortable drive capacity is 120 GBytes.

Most new high-performance disk drives suitable for this application use Fibre Channel as the transport layer carrying the SCSI protocol for data and control. Three primary classes of Fibre Channel drives are available. They include a single hard disk, a JBOD (Just a Bunch Of Disks) array, or a RAID (Redundant Array of Inexpensive Disks) array. Adding additional drives to a JBOD or RAID array increases both the aggregate storage rate and capacity. The maximum storage rate is limited by the Fibre Channel interface speed or by the drive storage speed, whichever is lower.

In this application, an inexpensive JBOD disk system with four 30 GB drives and a 2 Gbit/sec interface nicely satisfies both the capacity and the data rate requirements.

SBC System Implementation

Figure 2 shows an architecture based on the Pentek Model 4205 Processor. Two Pentek 6236 dual 14-bit A/D converter VIM-2 modules are attached to the ➤

12-bit 210 MHz A/D Board with Dual Virtex-II Pro FPGAs

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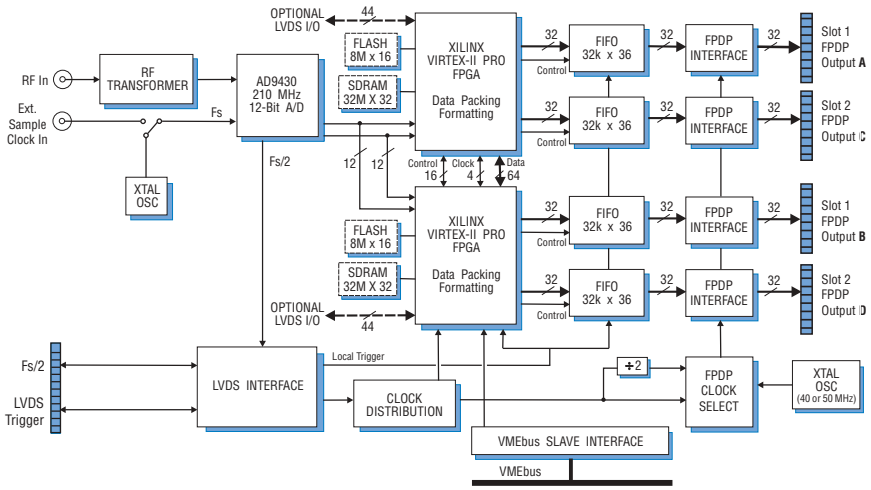
boards, ideal for applications such as multichannel radar systems.

Virtex-II Pro FPGAs

The 6821 features two XC2VP20 or XC2VP50 Virtex-II Pro FPGAs, each with up to 6 million system gates and as many as 232 hardware multipliers. The multipliers, along with generous on-chip configurable RAM, make these FPGAs ideal for handling real-time DSP algorithms at the 210 MHz sampling rate.

The two FPGAs are optionally equipped with 128 MB of SDRAM for data display and buffering. Two 16 MB FLASH memories support boot operations for optional use of the embedded FPGA microcontrollers.



Model 6821 Block Diagram

FPDP Outputs and LVDS I/O

Four FPDP ports deliver tremendous throughput to a wide range of third-party products. These FPDP ports support data transfer rates of 320 MB/sec. One port per FPGA is attached to the 6821 front panel, while the second is available on an optional second-slot panel. A data demultiplexing mode splits the data stream between each pair of FPDP ports reducing data rates by a factor of up to eight to support slower FPDP devices. Additional LVDS data I/O is available through either the VMEbus P2 connector or the optional second-slot front panel.

For more information visit our website at: www.pentek.com/go/pipe6821. ❑

Model 4205 providing four digitizer channels for the front end. The optional 2 Gbit Fibre Channel interface is included for direct connection to the JBOD disk system over copper cable.

Since efficient data movement is essential in this application, several strategies were investigated and implemented at each transfer path.

In order to improve efficiency at the front end, the FPGA on each 6236 module packs two 14-bit samples from the A/D converters into a 32-bit word for transfer across the VIM interface. This 32-bit path continues through the VIM FIFO and baseboard FPGA on the 4205. Further packing of these 32-bit words is accomplished within the PLX PCI interface to match the 64-bit data width of PCI Bus 1.

Most efficient Fibre Channel transfers occur when data is sent to the drives in large blocks to minimize protocol overhead. Therefore, the 1 GB global SDRAM is used as a staging area to create large data blocks.

Data from each A/D channel is written into 32 MB memory buffers arranged in a ping-pong architecture. When one buffer becomes full, it is delivered to the Fibre Channel interface while the alternate 32 MB buffer begins filling. There are four pairs of 32 MB ping-pong buffers in the SDRAM, one for each A/D channel.

In order to fill these buffers, the DMA controllers inside the PLX PCI interface proved to be the most effective mechanism. These DMA engines operate in the demand mode in response to hardware FIFO flags generated by the FPGAs on the 4205.

Moving data from the SDRAM to the Fibre Channel device requires a different strategy. In this case, the DMA controller inside the QLogic Fibre Channel interface offers the highest efficiency. Once a 32 MB data buffer is available for delivery, this DMA controller fetches the data from the SDRAM and writes it out to one of the four disks in the JBOD system.

The PowerPC is responsible for managing the PLX and QLogic Fibre Channel DMA engines and for setting up the overall length of the recording. In addition to controlling recording start and stop, the processor keeps track of the channel-to-disk assignment to make sure the Fibre Channel packets are appropriately formed and targeted. The processor also controls the functions of the 6236 A/D mezzanines.

The processor acts in a supervisory role directing traffic on the board. It also supports read back operations from the JBOD, so that data stored in real-time during the recording event can be retrieved and transferred across the Ethernet port to a workstation for archiving and analysis.

An obvious enhancement of this system would be to tap the power of the four Xilinx FPGAs to perform signal processing functions. The FPGAs are ideally situated directly in the data stream and are supported with a wealth of development tools including Pentek's GateFlow® FPGA Resources.

This wideband real-time recording system is available from Pentek preconfigured and pretested as System RTS 2501. For more information on the RTS 2501 visit: www.pentek.com/go/pipe2501art. ❑

Product Focus

Model 6821

Pentek Introduces the Industry's First VME Board with 12-bit 210 MHz A/D and Dual Virtex-II Pro FPGAs

Model 6821 features one of the fastest A/Ds in the market with sampling rates to 210 MHz!

GateFlow

Features

- Digitizes and processes signals with 100 MHz bandwidth in real-time
- Multiboard synchronization and FPDP or FPDP-II ports
- Large local memory for real-time recording and digital delay applications
- Compatible with Pentek GateFlow® IP Cores and FPGA Design Tools
- Designed for radar, SIGINT and high-speed data acquisition applications

The new single-channel 6U VMEbus board features one of the fastest 12-bit A/Ds on the market with sampling rates to 210 MHz. Targeting extremely high-performance DSP tasks, the Model 6821 couples this high-speed A/D with two Xilinx Virtex-II Pro FPGAs. The board excels in data acquisition, demodulation, filtering, convolution and analysis operations that are critical in many real-time high-speed applications.

Input Stage and A/D Converter

The Model 6821 accepts one front panel analog input through a 50-ohm transformer with flat frequency response from 400 kHz to 700 MHz. Input level is software-selectable at +8 dBm or +2 dBm full-scale. The transformer offers a low-distortion path to the differential inputs of the AD9430 A/D converter and minimizes system noise and ground loops.

Clocking Gating and Triggering

The sampling clock can be sourced from an internal crystal oscillator or from an external sinusoidal clock with maximum frequency of 210 MHz. An external LVDS bus supports synchronous data acquisition across multiple