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VXS: Switched Serial Gigabit Fabric for VMEbus

The VMEbus, well into a third decade of widespread deployment, continues as the dominant bus structure for high-performance embedded systems. In an industry characterized by a steady succession of new device offerings with speed and density increases every few months, VMEbus has retained this leadership position not simply because it was based on a sound electrical and mechanical architecture. Indeed, the major reason for its longevity has been a series of performance and feature enhancements promoted and nurtured by a broad base of VMEbus vendors. Before we discuss VXS, the latest enhancement, we will first review some basics of switched fabrics.

Switched Fabrics

A switched fabric is a system for connecting devices together to support multiple simultaneous data transfers usually implemented with a crossbar switch, as shown in Figure 1. Data is sent in packets with information contained in the packet header for identification, routing and error detection and correction. To ensure adequate performance for any given system, the interconnecting fabric can be as simple as a point-to-point connection between two devices, or a more complicated architecture that may include switches, routers, hubs, and repeaters.

Because of recent advances in serial data technology, the new generation of switched fabrics uses serial links. With bit data rates now in the gigahertz range, these new serial interfaces can easily rival their parallel counterparts. In many cases the transition from parallel to serial occurs only at the lowest levels of the OSI layer model. In this way, existing protocols are maintained so legacy products with parallel interfaces can be supported with hardware adapters that convert the physical layer interface to the new serial link.

This strategy has been extremely successful in allowing the new serial technology to be inserted seamlessly. One excellent example is the migration of parallel flat cable SCSI to serial Fibre Channel as the interface of choice for the latest generation of high-performance hard disks and disk arrays.

One of the major benefits of these new serial interfaces is the reduced number of signal lines and smaller connectors and cable. This results in enhanced system density, simpler system integration, lower installation costs, and easier maintenance. Another benefit is the ability to use copper cable for low cost local connections or optical cable for fast, long haul transmission of data. Again, the physical layer can be made completely transparent to the protocol layer.

Yet another benefit of serial links is the ability to gang together multiple serial links to boost data throughput. Since the signal in each single bit link contains embedded clock and timing information, each link can propagate on its own across the channel and transceivers at each end can handle the multiplexing and demultiplexing for 1x, 4x, 8x or 16x ganging at a relatively low hardware layer.

Once the benefits of switched serial fabrics became apparent, embedded systems vendors sought ways to take advantage of this technology for a wide range of interconnection needs: boards to peripherals, boards to boards, chassis to chassis, and facility to facility. Not only are switched serial fabrics attractive alternatives for front panel interconnections, they are also extremely appropriate for backplane data traffic to augment or replace the conventional parallel backplane bus.

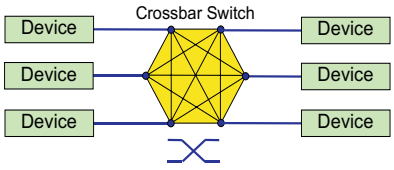

Figure 1. Switched Fabric Concept

Popular Switched Serial Fabrics

Embedded system vendors are now faced with many contending switched serial fabrics:

Infiniband is primarily aimed at server and storage system connectivity for box-to-box links.

StarFabric provides transparent serial links between PCI devices.

PCI Express is Intel's initiative for connecting processors and boards in personal computers and workstations.

Hyper Transport is AMD's solution for chip-to-chip and board-to-board connections in personal computers.

RapidIO is targeted for chip-to-chip and board-to-board connections for real-time COTS embedded systems and has strong support from Motorola.

These five fabrics are all vying for position. Aside from some valid technical pros and cons for each fabric, the key issues for switched fabrics tend to be business issues. For example: which major vendors are backing each standard? How easily can these new fabrics be integrated into existing software operating system environments? What components are available for bridging to existing hardware and processors? What kind of switches are available? And finally, can the fabric achieve a high production volume to make the parts inexpensive and easily connected?

Serial RapidIO

One of the switched fabrics, Serial RapidIO, is especially well suited for ➤

VXS: Switched Serial Gigabit Fabric for VMEbus

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real-time embedded systems. RapidIO is promoted by the RapidIO Trade Association whose founding members include Motorola, Lucent, Mercury, IBM, Texas Instruments, et al.

Objectives of this high-performance, packet-switched, interconnect standard include fast interprocessor communication, networking of DSPs, high-speed backplane interconnect, and efficient chip-to-chip and board-to-board transfers. These speed goals are addressed with scalable serial bit rates of up to 10 GHz. Performance and efficiency are achieved through a combination of a low-overhead protocol plus hardware error detection and correction. By offloading these tasks from the processor, Serial RapidIO is well suited for real-time applications, where shared coherent memory, channel predictability and low-latency are essential.

At the physical layer, Serial RapidIO uses the same differential current mode signaling as other standards including Fibre Channel, Infiniband and 802.3 XAUI.

VXS

During the last few years, the VITA 41 committee of the VMEbus Standards Organization has been defining a switched serial backplane fabric for VMEbus called VXS. The specification defines a VXS Payload Card, a VXS Switch Card and a connector scheme for a backplane family to support VXS.

Because of the "fabric wars", the VXS specification was defined to be fabric agnostic: there are five sub-specifications, one for each of the five fabrics described previously. The switched fabric architecture chosen to connect the boards across the backplane is a ganged 4x, full-duplex serial channel, so that each interconnect supports data flow in both directions simultaneously.

Serial bit rates are defined for frequencies up to maximum of 10 gigabits/sec, although lower frequencies are supported for the first systems. With the 4x ganging and a nominal bit frequency of 2.5 GHz, the input path and output path are both capable of moving data at 1 Gbyte/sec.

VXS Payload Card

The VXS Payload cards are processor, CPU, memory, and data converter 6U VMEbus cards with the VXS interface added. They have standard P1 and P2 connectors that implement the standard VME64x backplane interface. A new P0 backplane connector mounted between P1 and P2 handles two 4x, full duplex switched serial ports. Figure 2 shows a simplified view of the Payload card and the new VXS P0 connector.

At a 2.5 GHz clock frequency, each VXS Payload card can move data in and out at an aggregate rate of 4 GBytes/sec, two orders of magnitude above the original VMEbus backplane specification!

VXS Switch Card

Unlike the Payload card, the VXS Switch card has a 6U VME board form factor but no P1 and P2 connectors. Instead, it has up to eighteen 4x full-duplex serial connectors and a power connector. The VXS Switch card implements the crossbar switching to connect Payload Cards together. Figure 3 shows a view of the VXS Switch card.

VXS Switch cards can have any number of crossbar switches and any number of serial ports. They may also include other interfaces to networks for communication and storage devices, as well as front panel serial ports to other VXS Switch cards in the same chassis or in adjacent racks. Optical serial ports could be used for remote high-speed data transfers.

VXS Backplane

The VXS backplane can take on many different layouts to accommodate specialized system needs, but will normally handle two to twenty Payload cards and one or more Switch cards. The standard board-to-board pitch of 0.8 inches is maintained

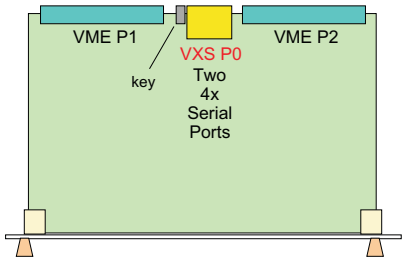

Figure 2. VXS Payload Card

throughout, and other VMEbus card cage mechanical hardware (card guides, frames, etc.) is compatible. The objective is to connect the two 4x serial links of each Payload card to links on the Switch card(s) to support the necessary board-to-board connectivity. Some smaller systems may require only a few Payload slots and a very simple Switch card, while others may need to use a full width backplane and multiple Switch cards to handle the required traffic.

Figure 4 shows one example of a 20-slot VXS backplane that holds 18 Payload cards divided equally in each half, and two Switch cards occupying the two center positions. One serial link from each Payload card is wired to one of the Switch cards while the second is wired to the other Switch card.

Since there are a maximum of 18 serial link connections on each Switch card, all 18 Payload cards can be connected to each other through two redundant paths, namely through both of the two Switch cards. This dual redundancy is attractive for ➤

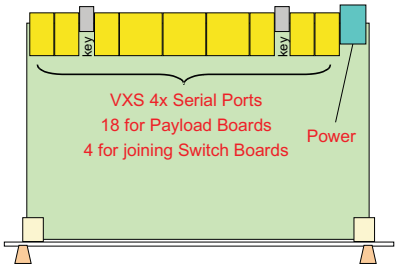

Figure 3. The VXS Switch Card

16-Channel Multiband Digital Receiver PCI Board

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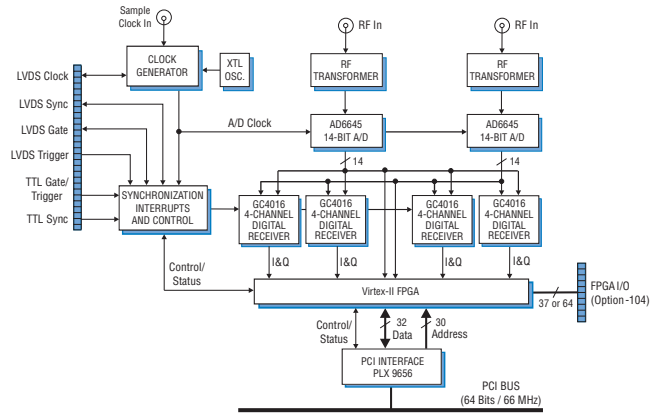
(optionally, XC2V3000), which is configured to perform various modes of data packing, formatting and channel selection.

The A/D outputs are also connected directly to the FPGA so that wideband A/D data can be delivered directly to the baseboard bypassing the digital receivers. An A/D decimation mode allows one of every N samples to be written into the FPGA memory, where N is an even integer between 2 and 4096.

Optionally available GateFlow™ FPGA Design Kits, allow the FPGA to be user-configured for implementing functions such as convolution, framing, pattern recognition or decompression.

Output Bandwidth

With a 100 MHz sample clock, the usable output bandwidth of each of the 16 receiver channels is 2.5 MHz. However, since the Model 7631 delivers parallel digital outputs from the GC4016 into the FPGA, users can take advantage of the GC4016 channel combining mode to join two or four receiver channels into a single channel with a resulting bandwidth of 5 or 10 MHz, respectively. This supports many of the new wideband wireless standards.



Model 7631 Block Diagram

Since both A/Ds connect directly to the FPGA, signals with even wider bandwidths can be accommodated.

PCI Interface

The FPGA output is connected to a 66 MHz, 64 bit PCI interface capable of up to 528 MB/sec peak data rate.

An industry standard PLX9656 PCI interface chip ensures full conformance to all PCI bus timing specifications.

For more information on the 7631 call us at 201-818-5900 or visit our website at: **www.pentek.com/go/piped7631.** ❑

many applications requiring fault tolerance and high availability. VXS Switch cards also have additional serial links that join Switch cards together, providing yet another path for routing.

Summary

VXS promises to solve even the most challenging data transfer requirements of real-time embedded systems. It will assure the continuing popularity of VMEbus by allowing legacy boards to coexist with the new VXS versions. ❑

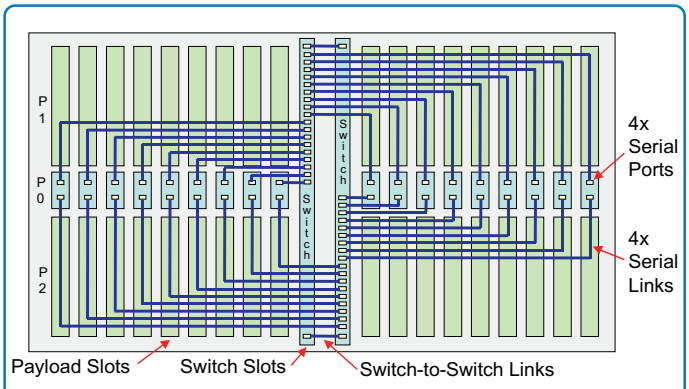


Figure 4. Example of a 20-slot VXS Backplane

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You'll be pleasantly surprised when you visit our website and find a whole new look. With the help of customer feedback, we have added some dynamite features to the site. Some of them include arranging our product offerings by application area, pulldown menus, easier log-in and YourPentek customization facilities, the ability to search by model number, and much more... Take advantage of the new features now and visit www.pentek.com. ❑

Product Focus

Model 7631

16-Channel Multiband Digital Receiver PCI Board

Model 7631 Features a Virtex-II FPGA and two 100 MHz 14-bit A/Ds

Features

- 250 MHz input bandwidth
- 5 kHz to 10 MHz output bandwidth when sampling at 100 MHz
- User-configurable Xilinx Virtex-II FPGA
- Two 80 or 100 MHz 14-bit A/Ds

Model 7631 is a 16-channel multiband digital receiver PCI board designed for computers with PCI bus slots. The 7631 includes two 14-bit A/Ds and a Virtex-II FPGA for signal processing.

Model 7631 accepts two transformer-coupled RF inputs at +4 dBm full scale into 50 ohms on front panel SMA connectors. The inputs operate at a maximum sampling frequency of 80 MHz or, optionally, up to 100 MHz.

The sampling clock can be driven from an internal crystal oscillator, or from an external clock.

Digital Receivers

The 7631 includes four Graychip GC4016 quad multiband digital receiver chips. The maximum input sampling rate for the GC4016 is 100 MHz. Each device includes four independently tunable receiver channels capable of center frequency tuning from DC to $f_s/2$ where f_s is the sample clock frequency.

Each GC4016 accepts two 14-bit parallel inputs from the two A/D converters. A crossbar switch inside the GC4016 allows all 16 receiver channels on the board to select either of the two A/D inputs for flexible switching.

Synchronization

The front panel clock and sync bus allow one 7631 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling. Sync lines on the bus allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and data collection on multiple 7631's.

FPGA

The 16 receiver outputs are delivered to a Xilinx Virtex-II XC2V1000 FPGA