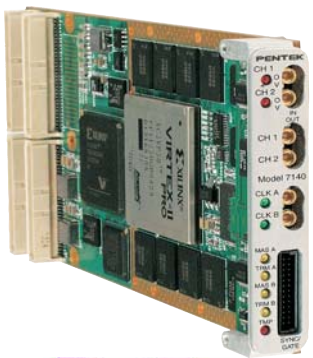
New!

Model 7140-420 Installed Core

GateFlow Transceiver with Dual Wideband DDC and Interpolation Filter - PMC/XMC



ReadyFlow Board Support Libraries
GateFlow

Features

- Complete software radio transceiver solution
- Dual GateFlow Core 420, high-performance wideband DDCs and interpolation filter factory-installed
- Improved dynamic range
- Extended DDC decimation range of 8 to 1,048,576
- Extended DDC bandwidth range of 10 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 16,384
- Extended DUC bandwidth range of 40 MHz to 4.88 kHz
- ***Conduction-cooled version available with Model 7141-703***
- ***Core 420 is also available for Models 7240, 7340 and 7640: see page 3.***

General Information

Model 7140-420, Dual Digital Transceiver with Wideband DDC and Interpolation Filter cores, is a complete software radio system in PMC/XMC format. It includes two A/D and two D/A converters for connecting to HF or IF ports of a communications or radar system.

The 7140 receiver section features two AD6645 105 MHz 14-bit A/D converters and one TI GC4016 quad multiband digital downconverter. The digital outputs of the A/Ds are delivered to the Virtex-II Pro FPGAs and to other module resources including the GC4016 which supports a decimation range from 32 to 16,384. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each of the four channels ranges from 2.5 MHz down to 5 kHz. By combining two or four channels, decimations of 16 or 8 can be achieved for an output bandwidth of up to 5 or 10 MHz, respectively.

For applications that require even wider bandwidths, Pentek offers the GateFlow IP Core 420 High-Performance Wideband DDC similar in functionality to the GC1012, but with enhanced performance and an interpolation filter that extends the range of the DAC5686 D/A converter.

Core 420 Wideband Downconverter

Like the GC4016, the Core 420 downconverter translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter then removes any out of band frequency components. An output decimator and formatter deliver output data in either real or complex representation.

An input gain block scales both I and Q data streams by a 16-bit gain term. The NCO provides over 118 dB spurious-free dynamic range (SFDR).

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable using RAM structures within the FPGA.

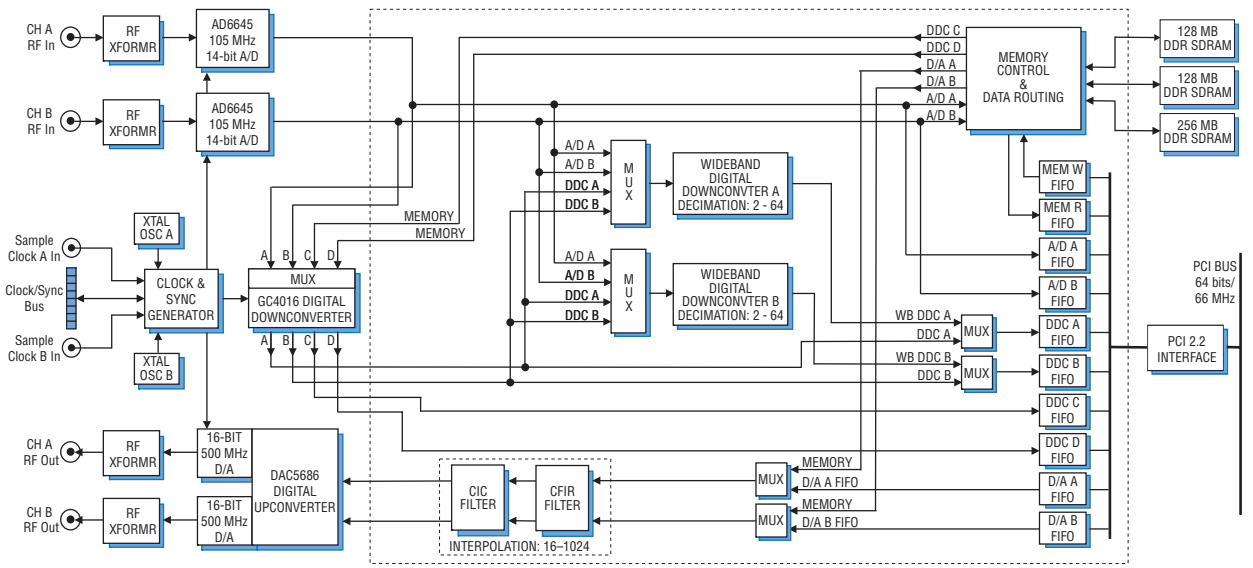
Two identical Core 420 DDCs are factory installed in the 7140 FPGA. The decimation range from 2 to 64 in six binary steps provides output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling rate of 100 MHz. It also delivers better stopband rejection than the GC4016 in combined channel modes.

A multiplexer in front of the Core 420 DDCs allows data to be sourced from either the A/D converters or from the output of the GC4016, extending the maximum cascaded decimation factor to 1,048,576.

Core 420 Interpolation Filter

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 16,384 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 16,384 which matches the maximum decimation of the GC4016 narrowband DDC.

In addition to the Core 420, all the standard features of the 7140 are retained including D/A waveform generator mode, all data routing and formatting, and delay and transient capture memory. ➤



XILINX XC2VP50 FPGA WITH GATEFLOW FACTORY INSTALLED CORE 420

New!

Model 7140-420 Installed Core

GateFlow Transceiver with Dual Wideband DDC and Interpolation Filter - PMC/XMC

XMC Interface

The Model 7140 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard provides, among others, for a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board. With two 4X links, the Model 7140 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and supports switched fabric protocols such as Serial RapidIO and PCI Express.

Ruggedization

Model 7141-70x is available in ruggedization levels from L0 forced-air commercial to L3 conduction-cooled with extended shock and vibration resistance.

Environmental

Option 703 (Level L3):

Operating Temp: -40° to 70° C
Storage Temp: –50° to 100° C
Sine Vibration: 10 g, 20–2,000 Hz
Random Vibration: 0.1 g^2/Hz, 20–2,000 Hz
Shock: 30 g, 11 msec
Relative Humidity: 0 to 95%, non-condensing; 0 to 100% with conformal coating

Ordering Information

Model	Description
7140	Dual Multiband Transceiver with FPGA - PMC/XMC
Options:	
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-104	FPGA I/O through P4 connector
-420	160 MHz wideband DDC and digital interpolation filter cores, factory-installed
-520	XMC interface
-70x	Ruggedized & conduction-cooled versions

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for board resources. Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7140's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 modules may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

PCI Interface

The Model 7140 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Mini-Circuits ADT4-5WT
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 270 MHz

A/D Converters
- **Type:** Analog Devices AD6645-105
- **Sampling Rate:** 30 MHz to 105 MHz
- **Internal Clock:** 100 MHz crystal osc.
- **External Clock:** 30 to 105 MHz
- **Resolution:** 14 bits

Digital Downconverter
- **Type:** TI/Graychip GC4016
- **Decimation:** 32 to 16,384; with channel combining mode: 8 or 16
- **Data Source:** A/D, FPGA, or PCI interface
- **Control Source:** FPGA or PCI interface
- **Output:** Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel female MMCX connectors
- **Full Scale Output:** +4 dBm into 50 ohms
  - **Option -002:** –2 dBm into 50 ohms
- **3 dB Passband:** 60 kHz to 300 MHz
  - **Option -002:** 400 kHz to 800 MHz

Digital Upconverter
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz, max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array
- **Type:** Xilinx Virtex-II Pro
- **Option -050:** XC2VP50
- **Option -104:** Installs P4 connector with 64 lines to the XC2VP50 FPGA

Memory
- **DDR SDRAM:** 512 MB in three banks
- **FLASH:** One bank of 16 MB

PCI Interface
- **PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
- **Local Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller

Environmental (Commercial version)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

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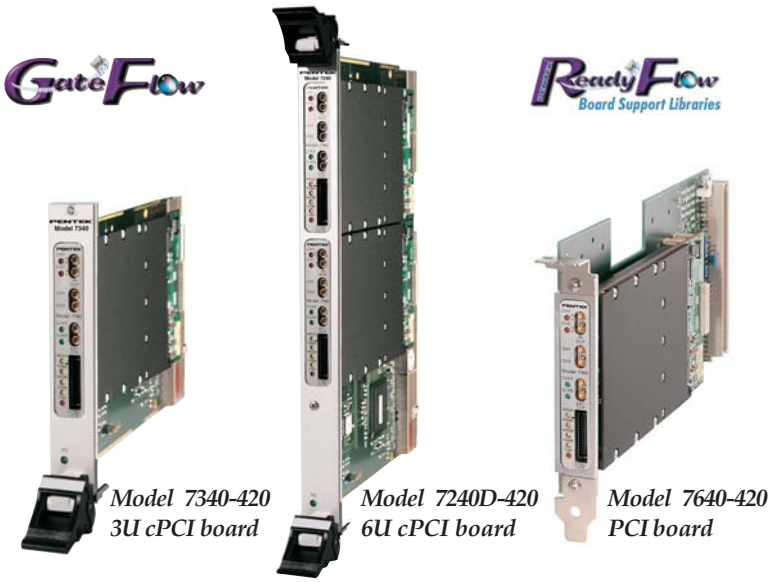
New!

Models 7240, 7240D 7340, 7640, -420

GateFlow Transceiver with Dual/Quad Wideband DDC and Interpolation Filter - PMC/XMC

Features

- Complete software radio transceiver solutions
- Two or four 105 MHz 14-bit A/Ds
- Four or eight digital down-converters (DDCs)
- One or two digital upconverters (DUC's)
- Two or four 500 MHz 16-bit D/As
- Dual GateFlow Core 420, high-performance wideband DDCs and interpolation filter, factory-installed
- Extended DDC decimation range of 8 to 1,048,576
- Extended DDC bandwidth range of 10 MHz to 76.3 Hz
- Extended DUC interpolation range of 2 to 16,384
- Extended DUC bandwidth range of 40 MHz to 4.88 kHz
- Dual timing buses for independent A/D and D/A clock rates
- LVDS clock/sync bus for multiboard synchronization
- FPGA custom I/O



General Information

Models 7240-420 and 7340-420 are cPCI software radio transceivers. They consist of one Model 7140-420 transceiver mounted on a cPCI carrier board. Model 7240-420 is a 6U cPCI board, while the Model 7340-420 is a 3U cPCI board. Model 7240D-420 is the same as the Model 7240-420, except it contains two 7140-420's rather than one.

Model 7640-420 is a half-size PCI software radio transceiver. It consists of one Model 7140-420 transceiver mounted on a PCI carrier board. Model 7640-420 attaches directly to computer boards with PCI bus slots. Front panel connectors are brought out on the computer's rear panel.

PCI/cPCI Interface

All Models include an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Option -104, FPGA I/O

Models 7240-420 and 7340-420 utilize the cPCI J3 connector.

Model 7240D-420 utilizes the J3 and also the J5 connector.

Model 7640-420 utilizes a 64-pin DIN connector for this option.

Functional Specifications

Please refer to Model 7140 for functional specifications. Individual datasheets of these units are available on our Web site at: www.pentek.com

Ordering Information

Model	Description
7240	Dual Transceiver with one FPGA - 6U cPCI
7240D	Quad Transceiver with two FPGAs - 6U cPCI
7340	Dual Transceiver with one FPGA - 3U cPCI
7640	Dual Transceiver with one FPGA - PCI
Options:	
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-104	FPGA I/O through cPCI J3 for 7240 and 7340; cPCI J3 and J5 for 7240D; 64-pin DIN connector for 7640
-420	160 MHz wideband DDC and digital interpolation filter cores, factory-installed