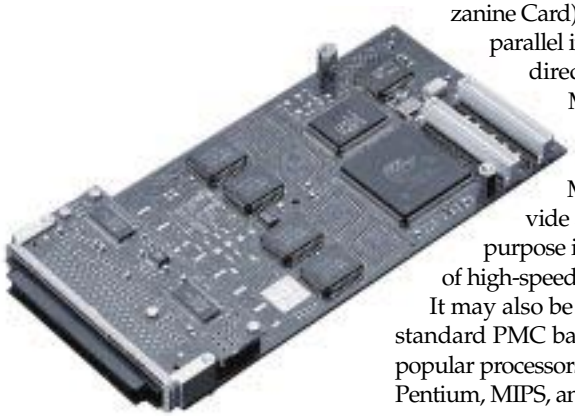
New!

Model 7101

Parallel Digital I/O PMC Module



General Information

Model 7101 is a single PMC (PCI Mezzanine Card) module for TTL or ECL parallel input or output. It can be directly attached to Pentek's Model 4285 Octal 'C40, Model 4286 Dual 'C80 and Model 6310 Multilink Adapter to provide a powerful general purpose interface for a wide range of high-speed peripheral devices.

It may also be attached to any industry-standard PMC baseboard including other popular processors such as PowerPC, Alpha, Pentium, MIPS, and i960.

Flexible I/O Options

A flexible I/O stage can be configured with a replaceable front-end 'personality module' which holds the connector and input line receivers or output drivers for each application. The standard connector is an 80-pin FPDP style KEL connector for TTL ports or a 40-pin KEL connector for 16-bit differential ECL ports.

By customizing the personality module and the FPGA, the unit can be easily configured to specific needs such as RS-422 or RS-485 differential, DR11W, etc.

Data Packing and Unpacking

The FPGA provides various types of data packing and unpacking options. It supports data I/O widths of different sizes, significantly reducing the load on the PCI bus. The packing options for the standard 32-bit input and output versions are as follows:

Input/Output Word Size	Packing Factor	Maximum Word Rate
32 bits	1:1	25 MHz
16 bits	2:1	50 MHz
10 bits	3:1	75 MHz
8 bits	4:1	75 MHz

Byte Swapping

In applications which call for exchanging data between the little endian and the big endian PCI bus, the Model 7101 may perform the necessary byte swapping thereby reducing software overhead.

DMA Controller with Linked List

The PCI interface is based on the PLX 9060/9080 device which includes a flexible DMA controller with linked-list capability. Thus it can transfer data to/from different memory locations within the PCI address map.

The DMA can be started by register accesses from a processor via PCI bus or by a direct hardware signal from the FIFO status flag outputs from the FPGA (Demand Mode).

Programmable I/O

Model 7101 features four user-programmable I/O pins. Each pin may be independently configured as inputs or outputs and may be read from or written to through control and status registers. One pin may also generate a PCI interrupt.

Interrupt to PCI

For maximum flexibility and throughput, the 7101 can be programmed to generate three types of interrupts to PCI:

- DMA transfer complete
- FIFO full, half-full, or not empty
- User input signal (PIO1 in FPDP)

Control and Status Registers

The Model 7101 features a number of Control and Status registers accessible from the PCI bus. These can be used to start and stop data acquisition functions including wait-for-SYNC (in FPDP) and start on register access.

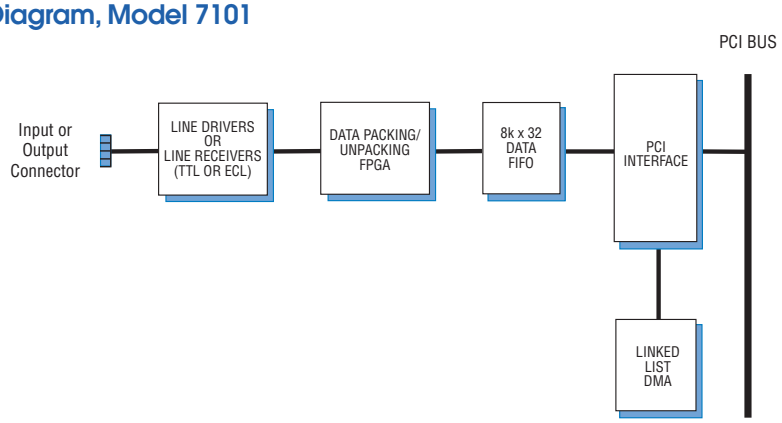
Features

- Up to 100 MB/sec rates
- Flexible input word length and data packing modes
- 8k x 32 FIFO buffer
- Byte swapping capability
- Synchronous or asynchronous ports with handshake
- Personality I/O connector stage and FPGA support custom requirements
- Compatible with the Pentek 4285 and 4286 DSP boards
- Compatible with Pentek Series 64xx A/D Converters, 6099 Memory Buffer and 65xx Digital Receivers
- Example software for host CPU boards

Ordering Information

Model	Description
7101	Digital parallel I/O PMC module
Options:	
-001	32-bit TTL FPDP input 80-pin KEL
-002	32-bit TTL FPDP output 80-pin KEL
-003	16-bit diff. ECL input 40-pin KEL
-004	16-bit diff. ECL output 40-pin KEL

Block Diagram, Model 7101



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