Model 6228

4-Channel D/A and Digital Upconverter with FPGA - VIM-2

ReadyFlow Board Support Package

GateFlow

Features

- Four 16-bit 500 MHz D/A converters with 500 MHz sample rate
- Two digital upconverters with 320 MHz sample rate
- 2x to 16x input signal interpolation filters
- Baseband D/A, quadrature modulation, and single-sideband upconversion modes
- Built-in clocking and synchronization across multiple modules
- Xilinx Virtex-II FPGA for custom DSP and signal formatting functions
- GateFlow FPGA Design Kit supports custom FPGA development

Ordering Information

Model	Description
6228	4-Channel D/A and Digital Upconverter with FPGA VIM-2
Options:	
-102	Front panel FPGA I/O (additional slot)
-112	Front panel LVDS FPGA I/O (additional slot)
-300	Xilinx XC2V3000 FPGA

General Information

Model 6228 is a VIM-2 module which attaches directly to VIM-compatible processor boards, including Pentek Models 4205, and 4290 through 4295. The Model 6228 contains four complete channels of 16-bit wideband D/A conversion. Additionally, channels can be combined for two-channel quadrature and single-sideband upconversion modes. A Xilinx Virtex-II FPGA provides additional signal processing capabilities.

Applications include generation of communication and radar test signals, electronic countermeasures, and implementation of transmit functions for advanced software radio communications systems.

Digital Upconverters

The Xilinx Virtex-II FPGA connects directly to both VIM interfaces of this VIM-2 module and provides control, status, timing and data formatting functions. It also delivers four channels of 16-bit data samples into two Texas Instruments DAC5686 Digital Upconverters and D/A converters. The D/A ouputs are sent to RF transformers that deliver wideband HF or IF signals to four female front panel SMA connectors.

The Model 6228 supports a maximum sample rate of 500 MHz in D/A mode and 320 MHz in upconversion modes.

Timing and Synchronization

The sample clock can be derived from an internal oscillator or from an external clock supplied via a front panel SMA connector. Dividers and PLL multipliers inside the DAC provide additional sampling clock options.

A LVDS (low voltage differential signal) timing bus connector on the front panel allows synchronization of multiple 6228s with the same clock, sync and triggering signals. Each module can be configured as a master or slave for the LVDS bus.

GateFlow FPGA Design Kit

The Model 6228 is available with either the XC2V1000 or XC2V3000 FPGA devices with 1 or 3 million gates, respectively. Standard functions within the FPGA include data packing and unpacking modes.

Available separately, the Model 4953 GateFlow FPGA Design Kit provides designers with all VHDL source code and device configuration for the basic factory installed functions to facilitate the addition of custom algorithms.

Front panel FPGA I/O is optionally available through a multipin connector located in a 2nd VMEbus slot. Option -102 provides 32 TTL level signals to the front panel. Option-112 provides 16 LVDS pairs and two high-speed clocks.