Model 4954-430 GateFlow IP Core

GateFlow 256-Channel Narrowband DDC IP Core

For more information go to:
pentek.com/fpga

GateFlow

Features

- 256 channels of narrowband digital downconverter (DDC)
- Extremely high channel-to-FPGA resource ratio
- Programmable number of individually tunable output channels up to 256
- Supports Virtex™-II, Virtex-II Pro, and Virtex-4 FPGAs
- 16-bit input data
- 16-bit complex output data
- Input data sample rates to 185 MHz
- 256 fully-programmable NCOs with 32-bit frequency tuning resolution
- Programmable decimation settings from 1024 to 9984 in steps of 256
- User-programmable 18-bit DDC FIR filter coefficients
- Default FIR coefficients provided for all possible decimations
- 75 dB stopband attenuation and 0.4 dB passband ripple with default filter coefficients

General Information

The Pentek Model 4954 GateFlow Library IP Core 430 is a 256-channel narrowband digital downconverter (DDC) bank designed for Xilinx Virtex-II, Virtex-II Pro and Virtex-4 FPGAs.

Utilizing a unique architecture, this core achieves a very high channel count-to-FPGA resource ratio, providing up to 256 narrowband channels in one mid-sized FPGA. Unlike classic channelizer methods, the Pentek 430 core allows for completely independent programmable tuning of each individual channel with 32-bit resolution. Filter characteristics are comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 9984 in steps of 256 and 18-bit user-programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Channelization Stage

This stage implements coarse tuning that provides 1024 fixed adjacent frequency channel outputs at the coarse tuning frequencies. Proprietary signal processing assures alias-free performance of greater than 75 dB across the passpand of each of the 1024 channelizer ouputs.

Channel Switch Matrix

Based on the desired tuning frequency setting, the Channel Switch Matrix automatically selects the most appropriate channelizer output for each of the 256 fine tuning DDC channels.

Compensation Filters

Before entering the DDCs, data passes though a FIR compensation filter. This further improves the passband flatness of each of the channelizer outputs selected by the Channel Switch Matrix.

Downconversion Stage

This stage of Core 430 features 256 sets of NCO local oscillators, mixers and decimating FIR filters.

Each NCO generates complex sine and cosine sample data streams using a digital phase accumulator and lookup table.

All 256 NCOs are independently tunable with 32-bit resolution. They deliver 18-bit ouput samples with a SFDR of 110 dB.

These complex NCO ouputs are mixed with the complex outputs of the compensation filters in 256 mixers, each consisting of a pair of digital multipliers. As a result, any desired signal of interest in each channel can be independently translated down to 0 Hz.

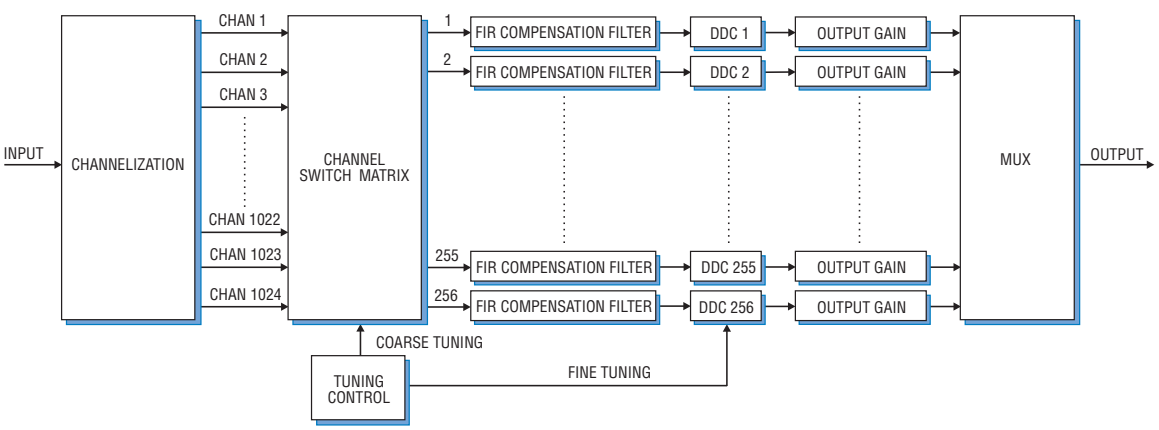
Complex outputs of the 256 mixers are passed to a bank of 256 decimating FIR low-pass filters. All 256 filters may be set to a decimation of any integer value from 4 through 32, allowing for overall decimations of 1024 to 9984 in steps of 256.

The single decimation setting is global for all channels.

Output Gain

Before the final output data is rounded back to a 16-bit result, it passes through a programmable gain stage.

This stage is used to both compensate for decimation-dependent bit growth in the filter and to allow for amplification of the result. Each channel has an independently programmable 16-bit gain control. ➤



PENTEK
Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

GateFlow 256-Channel Narrowband DDC IP Core

➤ In the event that excessive gain is applied, overflow logic can detect and flag saturation. The output is saturated and rounded to a 16-bit result. The final 256 output channels are multiplexed onto a single output data stream.

Performance

The performance specifications of the Pentek Core 430 are as follows:

Parameter	Value
Input Data Resolution	16-bit
Output Data Resolution	16-bit complex
Tuning Resolution	Clock freq. / 2^{32}
Decimation	1024 – 9984 in steps of 256
Passband Ripple	≤0.4 dB with default filter coefficients
Usable Bandwidth	80% with default filter coefficients
Stopband Attenuation	≥75 dB (limited by stage 1)
NCO SFDR	≥110 dB

Notes:
(1) With I/O registers packed into IOB Flip-Flops.
(2) With all I/O brought out to pins.
(3) To maximize clock rate, use DCMs.

Speed Performance

Input and output sampling rates are proportional to the clock frequency. The maximum clock frequency for each device is determined by its speed grade.

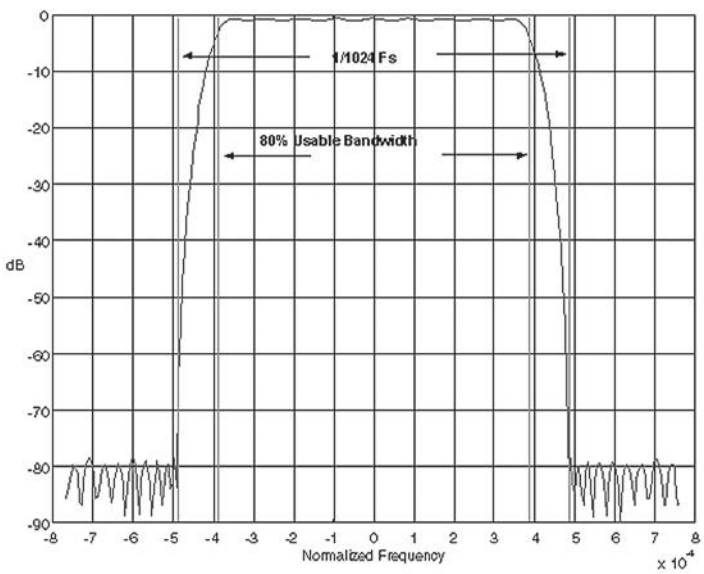
Xilinx Speed Grade	Max Clock Rate	Max Input Sample Rate
Virtex-II, Virtex-II Pro Series		
-7	173 MHz	173 MHz
-6	154 MHz	154 MHz
-5	140 MHz	140 MHz
Virtex-4, XC4FX60		
-12	185 MHz	185 MHz
-11	161 MHz	161 MHz
-10	138 MHz	138 MHz

FPGA Resource Utilization

The Pentek Core 430 will fit into the Xilinx Virtex-II Pro XC2VP50 or larger devices. The chart below shows the utilization of FPGA resources:

Resources	Virtex-II Pro	Virtex-4
Slices	15,397	18,070 (1)
IOB	161 (2)	161 (2)
Block RAM	132	132
Block Multipliers	123	123
Global Clocks	2	2
DCM/DLL	Optional (3)	Optional (3)
PPC	0	0

Decimate by 1024 Normalized Frequency Response



This figure illustrates a typical normalized output frequency response for a decimation of 1024 using the default filter coefficients. Note that all out-of-band frequencies are attenuated by 75 dB or greater while maintaining 80% usable bandwidth.

Ordering Information

Model	Description
4954-430	256-Channel Narrowband DDC IP Core

PENTEK
Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com