Model 4954-421 GateFlow IP Core

GateFlow Wideband Digital Downconverter (DDC) IP Core

For more information go to:
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Features

- High-performance wideband digital downconverter (DDC)
- Supports Virtex-II™ and Virtex-II Pro™ FPGAs
- Fits in Virtex-II XC2V1000 or larger
- Similar to GC1012B with enhanced features
- Input data 16-bit real or 16-bit complex (I and Q)
- Maximum input data rate of 160 MHz
- Maximum input bandwidth of 80 MHz (real input) or 160 MHz (complex input)
- Fully programmable NCO with 32-bit frequency and phase offset control
- SFDR >110 dB
- 2, 4, 8, 16, 32, and 64 decimation for complex output
- 1, 2, 4, 8, 16, and 32 decimation for real output
- Decimating FIR filter features up to 1792 taps
- User-programmable 18-bit FIR filter coefficients
- Default FIR filter coefficients for 80% and 90% filters
- Output formatter delivers real, complex, offset, inverted data in 16 or 24 bits

General Information

The Pentek GateFlow Model 4954 Library IP Core 421 is a high-speed wideband digital downconverter (DDC) designed specifically for Xilinx Virtex-II and Virtex-II Pro FPGAs.

The core offers similar functionality to the Texas Instruments GC1012B, but with enhanced speed, performance and programmability. The core consists of three major DSP sections: the mixer, the local oscillator and the FIR filter.

Input Stage and NCO

Core 421 accepts 16-bit real or complex input samples at up to 160 million samples per second. Inputs can be scaled by a 16-bit gain multiplier and overflow logic detects overflows.

The NCO (numerically controlled oscillator) local oscillator generates the cosine and sine sequences which are applied to the complex mixer to translate the input signal to zero frequency. This NCO provides over 118 dB spurious-free dynamic range (SFDR). Additional logic provides more flexible frequency and phase control as well as independent accumulator reset.

Mixer and FIR Filter

The mixer utilizes four 18 x 18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. For real input data, the Q input path is simply set to zero.

A mixer bypass path allows input data to be sent directly to the FIR filter with no frequency translation.

The FIR low-pass filter operates on the mixer output to remove energy from adjacent channels. It uses a highly-efficient proprietary polyphase decimating filter architecture with decimation factors of 2, 4, 8, 16, 32, and 64.

Four sets of user programmable coefficients are supported. Two factory default coefficient sets for 80% and 90% passband filters deliver 100 dB and 75 dB stopband rejection, respectively.

Output Stage

The output formatter allows the user to invert the output spectrum; offset the spectrum by one-half the output rate; convert the complex output stream to a real stream at twice the rate; and round the output to 16 or 24 bits.

Speed Performance

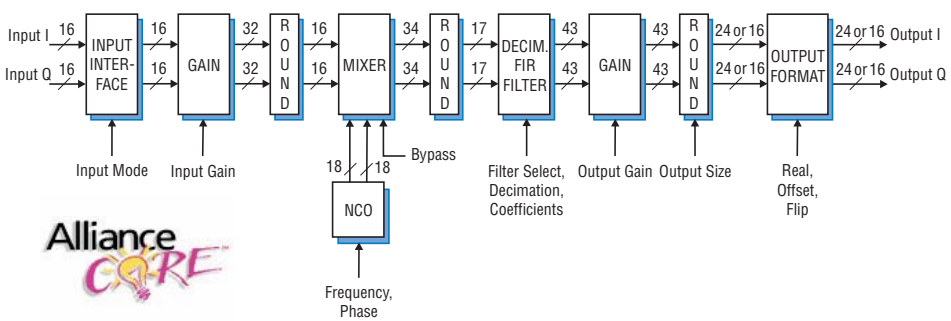
Input and output sampling rates are proportional to the clock frequency. The maximum clock frequency for each device is determined by its speed grade.

FPGA Resource Utilization

Xilinx Speed Grade	Max Clock Rate	Max Input Sample Rate
-7	160 MHz	160 MHz
-6	140 MHz	140 MHz
-5	126 MHz	126 MHz
-4	110 MHz	110 MHz

The Core 421 will fit into the Xilinx Virtex-II XC2V1000 or larger devices. The chart below shows the utilization of FPGA resources:

Resources	Core 421
Slice LUTs	5,628
Slice Flip-Flops	7,043
Block RAM	37
Block Multipliers	36
Global Clocks	2



Ordering Information

Model	Description
4954-421	Wideband DDC IP Core

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com