Model 4274

14/12-bit 10/20 MHz A/D Converter MIX Module

Features

- 14-bit A/D converter with integral sample-and-hold
- 10 MHz maximum conversion rate
- 12-bit 10 or 20 MHz versions optionally available
- TMS320C40 DSP communications port output
- 512 ksample, high-speed data buffer memory
- Internal or external sampling clock

Ordering Information

Model	Description
4274	14-bit 10 MHz A/D MIX module
Option:	
-001	12-bit 10 MHz A/D
-010	12-bit 20 MHz A/D

General Information

This high-performance A/D converter MIX module with extremely deep on-board memory serves as ideal front end for wideband data acquisition and signal analysis systems. The dual output capability, using either the 32-bit MIX bus or the 8-bit TMS320C40 front panel comm port, supports many different signal processing requirements and architectures.

A/D Conversion

The heart of the unit is an integrated sample-and-hold amplifier and A/D converter delivering 14-bit resolution at a 10 MHz sampling rate. An input overload condition is detected and latched so that the processor may be warned of a data block of compromised integrity. 12-bit 10 MHz or 20 MHz versions are optionally available.

Flexible Buffer Memory and Outputs

Two 256k x 16-bit data buffers have been arranged in a "swinging buffer" configuration. One buffer is connected to accept data from the A/D converter at a 10 MHz maximum data rate. The second buffer is available to provide sequential samples to the MIX interface, or the front panel 'C40 comm port and behaves like a FIFO (first-in-first-out) memory.

When both buffers have completed their operation cycles, the buffers may be configured to automatically swap for the next cycle. This arrangement supports two completely independent data rates for the A/D converter and the output interface.

Sample Clock Oscillator

A crystal-controlled DIP oscillator is provided for use as the sample rate clock source. Sampling frequencies to 10 MHz are provided with programmable dividers. Alternately, a front panel BNC connector accepts an external TTL clock.

Specifications

Input: single-ended, ±2.0 V full scale, front panel BNC, 50 ohms input impedance

A/D converter: 14-bits up to 10 MHz with integral sample-and-hold (Edge Technology ET2471); 12-bit 10 or 20 MHz versions optionally available

Trigger/Gate control TTL-compatible input, or MIX bus control bit; positive or negative edge starts conversion; logic '0' or '1' enables conversion; generates MIX bus interrupt N samples after trigger, where N = 1 to 256

Data memory buffer: two each, 256k x 16 (256k samples) max. size; binary-step control from 1k to 256k, software configurable; swinging buffer scheme, provides up to 512k contiguous sample storage; output buffer appears as a FIFO mapped to a single memory location

MIX interface: memory-mapped status/control register; bits include pack mode enable, clear buffer, buffer size select, hold buffer, output buffer full and empty, input overload; memory-mapped data buffer output; interrupt sources are output buffer not empty and input overload

'C40 comm port interface: two 8-bit bytes per sample, high byte first; 16 Mbytes/s maximum output rate

Power: 3.0 A at +5 V; 0.5 A at +12 V, 0.5 A at –12 V from the MIX bus

Block Diagram, Model 4274