Model 4285

Octal TMS320C40 Processor VME Board

General Information

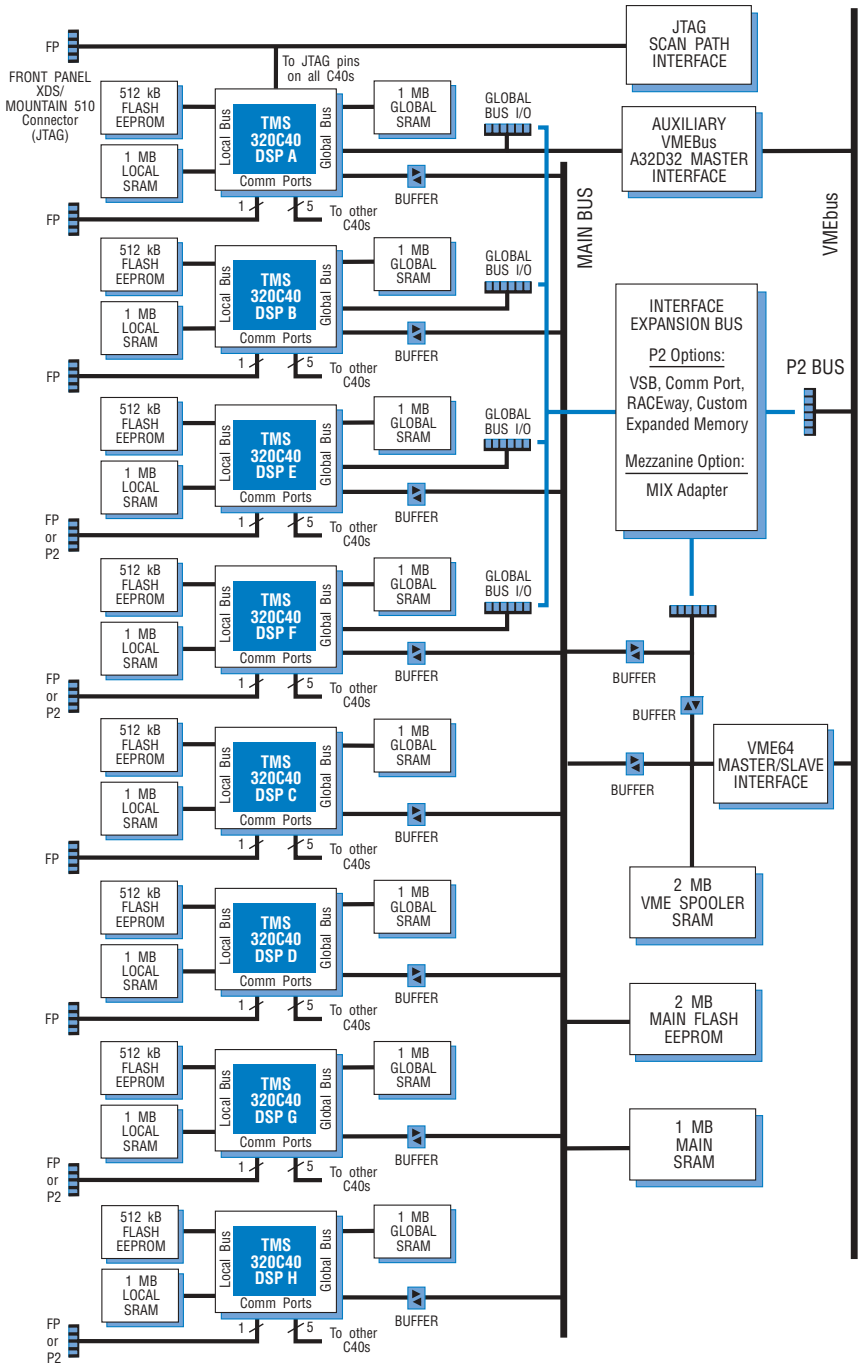
The Model 4285 Octal C40 board offers a high-density processing solution with flexible I/O capability in a single VMEbus slot. Eight C40s equipped with fast static RAM resources provide 480 MFLOPS of DSP horsepower.

Designed for power and flexibility, Model 4285 offers a wealth of I/O options, including a 3-module MIX interface and eight 20 Mbyte/sec comm ports for high-speed connections to other C40 boards and comm port peripherals. The unit may be easily configured with fewer processors or less memory to reduce cost in high-volume applications.

Local SRAM Memory

Each processor may be outfitted with 1 Mbyte Local SRAM. These SRAMs are ideal for storing program code, while the global bus processes the data.

Block Diagram, Model 4285



Features

- Scalable architecture with up to eight C40 processors
- 480 MFLOPS processing power
- One MB global and local SRAM per processor
- Up to 9 MB main global SRAM shared by all processors
- 512 kB boot flash EEPROM per processor
- Up to 2 MB user flash EEPROM
- 50 or 60 MHz clock
- MIX expansion bus
- VME master, VME64 master/slave and VSB interfaces
- High-speed global bus I/O
- RACEway interface option

PENTEK

Pentek, Inc., One Park Way ◆ Upper Saddle River, NJ 07458 ◆ Tel 201-818-5900
Fax 201-818-5904 ◆ Email: info@pentek.com

www.pentek.com

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Global SRAM Memory

One Mbyte Global SRAM for each C40 maximizes the use of its dual bus architecture and its ability to conduct data and program cycles in parallel on the two busses. This resource minimizes data moves and improves real-time performance.

Zero-wait access is provided between each C40 and its own global SRAM, and all eight C40s can be executing from their own global SRAMs simultaneously. Both local and global C40 busses can operate at full speed with zero-wait performance.

Shared Main SRAM Memory

One Mbyte of Shared Main SRAM (optionally expandable to 9 Mbyte) is accessible by all eight processors and the VMEbus simply by addressing the space allocated for the desired SRAM. When a C40 addresses the main global SRAM, a single wait state is generated.

Spooler SRAM

Up to 2 Mbyte Spooler SRAM buffers the data between the VMEbus and any of the C40s to decouple them from VMEbus traffic.

Main Flash EEPROM Memory

Data or application programs can be permanently stored in up to 2 Mbyte nonvolatile, Main Flash EEPROM, thereby providing true standalone embedded processor operation.

Communications Ports

These links support popular multiprocessing structures by providing private 20 Mbyte/sec data paths among processors. Eight comm ports are brought out to front panel connectors, while up to four may be brought out to the P2 interface.

VME Interface

The VME64 VMEbus interface allows any of the C40s to act as a VMEbus master for data transfers to or from any VMEbus device. It also provides VMEbus slave access to the Main Flash EEPROM, the Main SRAM, and the modules on any of the mezzanine expansion busses. The P2 interface provides capabilities for VSBbus, comm port, RACEway and custom interface options.

Mezzanine Bus Interface

All C40s have access to the mezzanine bus interface which supports SRAM memory expansion and up to three MIX modules.

Each C40 can read or write to these modules for easy access to Pentek's extensive family of I/O peripherals.

Specifications

Processors
Scalable, one to eight TMS320C40s, 50 or 60 MHz clock

Local SRAM
Size: 1 MB per processor
Access: C40 local bus only
Access time: zero wait state

Global SRAM
Size: 1 MB per processor
Access: C40 global bus only
Access time: zero wait state

Boot Flash EEPROM
Size: 512 kB per processor
Access: C40 local bus only
Access time: three wait states

Main SRAM
Size: 0 MB, 1 MB (std), 9 MB
Access: all C40s and VMEbus
Access time: one wait state

VME Spooler SRAM
Size: 512 kB (std), 2 MB
Access: all C40s and VMEbus
Access time: one wait state for 0.5 MB; two wait states for 2 MB

Main Flash EEPROM
Size: 0 (std), 512 kB, 2 MB
Access: all C40s and VMEbus
Access time: three wait states

VME64 VMEbus Master Interface
Access: All C40s and mezzanine bus, slot 1 controller
VME compliance: D64 A32, IH (1-7)

VME64 VMEbus Slave Interface
Access: VME Spooler SRAM, Main SRAM, and mezzanine bus
VME compliance: D64 A32, I (1-7),

Auxiliary VMEbus Master Interface
Access: Global Bus of Processor A
VME compliance: D32 A32, I (1-7), no support for D8 or D16

Power: 4.5 A at +5 V dc

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Support Software

Pentek **SwiftNet** supports a network of distributed VMEbus systems and allows the developer to run development tools on the host, while maintaining remote access to the VMEbus target systems.

Among others, third party software products include the Texas Instruments **Code Composer** integrated development environment.

SwiftNet

TI Third Party Network Member DSP TEXAS INSTRUMENTS

Ordering Information

Model	Description
4285	Octal TMS320C40 Processor for VMEbus, 50 MHz clock
Options:	
-001	2 MB Spooler SRAM
-005	1 MB Global and 1 MB Local SRAM (required option)
-010	0.5 MB Flash EEPROM
-011	2 MB Flash EEPROM
-031	MIX mezzanine adapter
-032	VSB master interface
-034	RACEway interface (requires at least four processors)
-035	8 MB SRAM expansion
-060	60 MHz clock

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