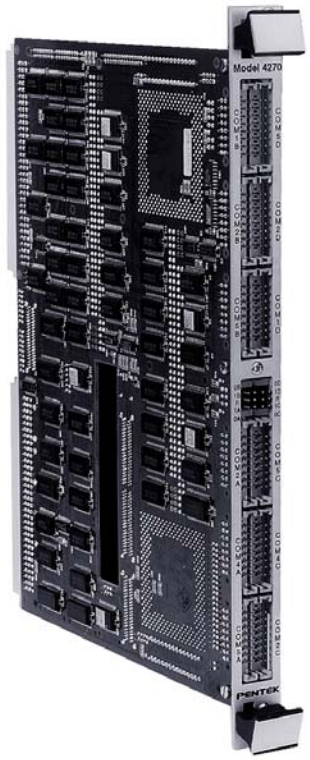
Model 4270

Quad TMS320C40 Processor VME Board/MIX Module



General Information

Model 4270 is a Quad TMS320C40 VMEbus Board/MIX Module with enough horsepower to tackle demanding processing applications. It combines the proven performance of four TMS320C40 DSPs with a board architecture built for extensive interconnectivity of processors, buses and memory resources.

Model 4270 was designed to relieve the bottlenecks associated with the movement of data which often erode the real-time performance of DSP designs.

With 4 Mbytes of local SRAM and 4 Mbytes of shared global SRAM, Model 4270 presents an incredibly powerful and yet elegantly simple programming model, to speed development time and boost real-time operation.

Powerful Standalone Processor

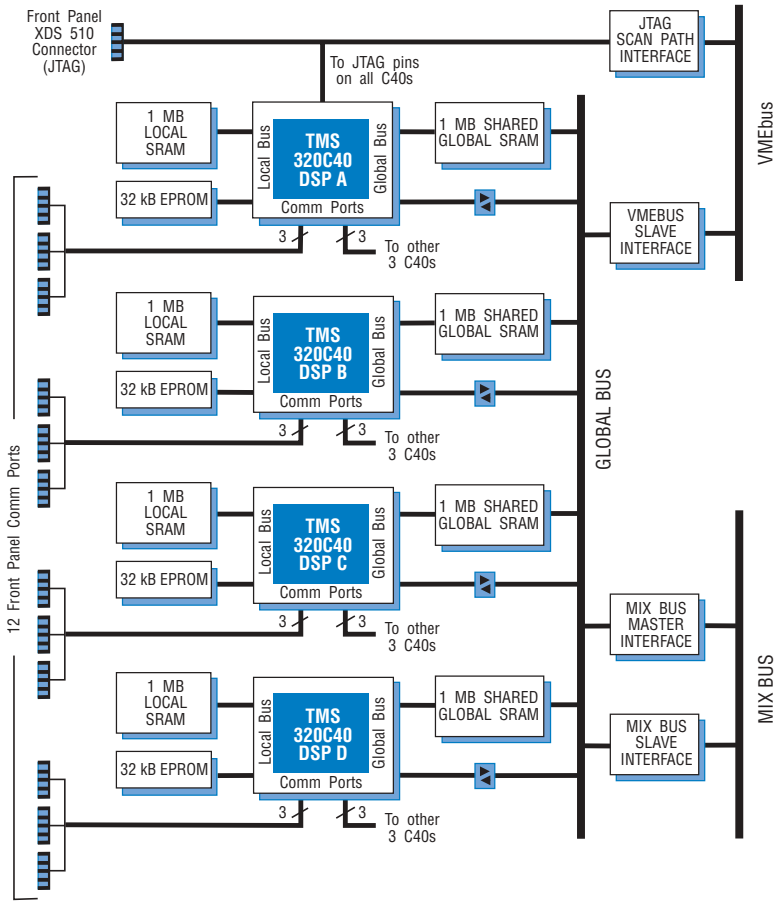
The Pentek 4270 is a full-depth single-slot VMEbus board with a complete VMEbus slave interface. All four sections of the shared global SRAM are addressable in A24 or A32 address space.

Shared Global SRAM Memory

A total of 4 Mbytes of Shared Global SRAM is accessible by all four C40s, the MIX bus, and the VMEbus simply by addressing the space allocated for the desired SRAM. This resource simplifies all applications by minimizing the data moves required by less powerful architectures.

Zero-wait access is provided between each C40 and its own global SRAM, and all four C40s can be executing from their own global SRAMs simultaneously. Both local and global C40 busses can operate at full speed with zero-wait performance. When a C40 addresses one of the other three global SRAMs, a single wait state is generated.

Block Diagram, Model 4270



Features

- Standalone VMEbus processor with VME slave interface
- Full-depth MIX module with MIX master interface
- 200 MFLOPS peak processing power
- Up to 4 MB global SRAM shared by all processors
- One MB local SRAM per processor
- 32k x 8 boot EPROM per processor
- Flexible communication port interconnections
- Compatible with all Pentek MIX baseboards & modules
- Occupies single card cage slot

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Local SRAM Memory

A private 1 Mbyte Local SRAM for each C40 maximizes the use of its dual bus architecture and its ability to conduct data and program cycles in parallel on the two busses. These zero-wait state SRAMs are ideal for storing program code, while the global bus processes the data.

Local EPROM Memory

In order to support nonvolatile storage of program or data, each C40 is equipped with a user-programmable 32 kB EPROM memory on its local bus. Ideal for embedded standalone systems which self-boot from power up, these memories can also be used for system firmware.

JTAG Emulator Support

A JTAG interface is mapped into the VMEbus slave address space to allow access from any VMEbus master. In addition, a JTAG interface to support the Model 8535 XDS emulator is also included.

Comm Port Support

Three of the six 20 Mbyte/sec communication ports for each C40 are connected to the other three C40s. The other three comm ports are brought out to convenient front panel connectors. These ports are compatible with Pentek's family of single and dual C40 coprocessor MIX modules and Pentek's other C40 comm port compatible products.

It's not a MIX Baseboard

Model 4270 is not a MIX baseboard. However, it can be used either as a standalone VME board or as a MIX module. As a full-depth MIX module, it can be attached to any MIX baseboard such as the Model 4200, along with data acquisition MIX modules, to create powerful signal processing systems.

Support Software

Pentek **SwiftNet** supports a network of distributed VMEbus systems and allows the developer to run development tools on the host, while maintaining remote access to the VMEbus target systems.

Among others, third party software products include the Texas Instruments **Code Composer** integrated development environment.

Specifications

Processors
Four TMS320C40s, 40 or 50 MHz clock

Local SRAM
Size: 1 MB (256k x 32) per processor
Access: C40 local bus only
Access time: zero wait state

Global SRAM
Size: 1 MB (256k x 32) per processor
Access: all four sections of global SRAM are accessible from all four C40s, MIX bus, and VMEbus
Access time: zero wait state from the global bus of the associated C40; one wait state from the global bus of the other three neighboring C40s

EPROM
Size: 32 kB (32k x 8) per processor
Access: C40 local bus only
Access time: three wait states

VMEbus Interface
VME compliance: slave device, A32 D32 I(1-7)
Memory model: A16 for control registers A24/A32 for global SRAM
A16 base address: set by jumpers, on any 64 byte boundary
A24/A32 base address: set by A16 registers, on any 4 MB boundary
Interrupts: levels 1 to 7

MIX Interface
MIX compliance: master and slave
Memory model: control register and global RAM are memory-mapped into MIX address space
Interrupts: generates interrupts to MIX baseboard; handles interrupts from MIX baseboard

Power: 9.0 A at +5 V dc

Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

Applications

- arrays for 3-D image processing
- bidirectional rings for neural networks
- pipelined linear arrays
- tree structures for complex searches
- hexagonal grids for numerical analysis
- 4-D hypercube structures
- hierarchical processing

Data Acquisition and Signal Analysis System

16-channel data acquisition and signal analysis system fits in just three VMEbus slots. System consists of a 4270, a 4255 SCSI Interface MIX module, a 4252 16-channel 16-bit A/D and D/A Converter MIX module, all stacked on a 4200A MIX Baseboard.

SwiftNet

TI Third Party Network Member DSP™ TEXAS INSTRUMENTS

Ordering Information

Model	Description
4270	Quad TMS320C40 Processor Board/MIX Module for VMEbus, 40 MHz clock
Option:	
-015	50 MHz clock

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