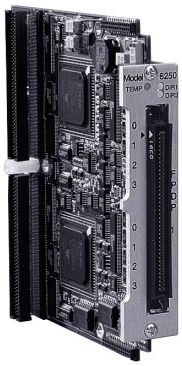
Model 6250

Configurable Logic FPGA with FPDP I/O VIM-2 Module



ReadyFlow Board Support Libraries

GateFlow FPGA Design Kit

Features

- Supports high-performance custom signal processing
- One or two FPDP (Front Panel Data Port) interfaces
- Xilinx Virtex-II Series FPGAs
- Two gate densities available: 1000K & 3000K
- GateFlow FPGA configuration package
- On-board auxiliary SRAM

Ordering Information

Model	Description
6250	Configurable Logic FPGA VIM-2 module with FPDP I/O

Options:

-002	Dual FPDP, plug and cable
-004	Dual FPDP, two slots
-102	Front panel FPGA I/O (additional slot)
-300	Xilinx XC2V3000 FPGAs
-401	1k FFT in FPGA
-404	4k FFT in FPGA

Accessories:

4953-250	GateFlow FPGA Design Kit for 6250

General Information

Model 6250 is a Configurable Logic FPGA VIM-2 module with FPDP I/O. It features up to two FPDP (Front Panel Data Port) interfaces, and two Xilinx Virtex II FPGAs (field programmable gate arrays).

The Model 6250 supports custom, high-performance signal processing and computing functions for any VIM-compatible processor board.

As a VIM-2 module, Model 6250 connects to two of the four processor nodes, leaving the other two available for a second VIM-2 module to provide other functions.

FPGA Devices

The Model 6250 may be equipped with one of two FPGA devices in the Xilinx Virtex-II family: Model XC2V1000 (standard), or XC2V3000 (Option -300).

Each FPGA interfaces directly to all three sections of the associated VIM interface: both serial ports, the 32-bit BI-FIFO parallel port and the control/status port. The BI-FIFO buffers on the processor board allow the processors to move blocks of data efficiently to and from each FPGA.

The two FPGAs are interconnected with up to 68 (XC2V3000) programmable user I/O lines to support data and control passing between the two devices. An optional connector is available for FPGA front panel I/O (Option -102).

SRAM

Each FPGA is equipped with two 256k x 16 SRAMs. Each SRAM is connected to the FPGA with separate address and data buses so they can be used independently. The SRAMS can be used for storing data without consuming internal FPGA logic cells to implement RAM.

FPDP Interfaces

One FPDP interface is provided as standard with an additional interface available in two different optional configurations: single-slot, with the second connector accessible through a front panel ribbon cable (Option -002), or two slots with the second connector in an adjacent slot (Option -004).

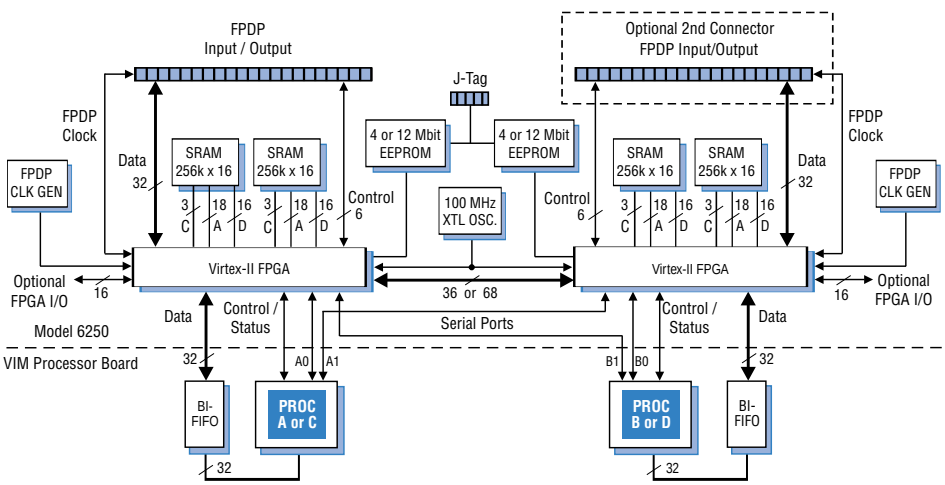
FPGA Programming

An optional FPGA design kit to be used in conjunction with the Xilinx Foundation development tool suite is provided. It includes VHDL source files for the VIM interface and control registers for the clock functions. Templates for implementing custom signal processing blocks are included with detailed instructions. FPGA code may be downloaded from the processor node or permanently stored in non-volatile memory.

Numerous third-party sources for IP signal processing core libraries compatible with the Virtex-II support a wide range of popular algorithms and functions. These include FFTs, FIR filters, compression and decompression algorithms, software radio blocks, decryption, telemetry functions, decoders, encoders, and convolution.

In addition, a GateFlow FPGA Design Kit is optionally available from Pentek.

Block Diagram, Model 6250



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