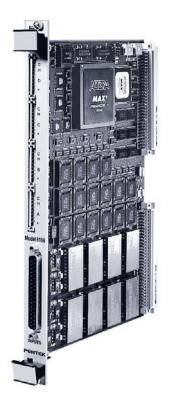
# Model 6106 Model 6109

# 8-Channel 14-bit 2 MHz A/D Converter VME Board 8-Channel 12-bit 20 MHz A/D Converter VME Board



# **General Information**

Models 6106 and 6109 are high-performance 8-channel A/D converters for VMEbus data acquisition, control, and DSP applications. Model 6106 offers 14-bit resolution, 2 MHz maximum sampling rate, and optional differential inputs. Model 6109 offers 12-bit resolution, 20 MHz maximum sampling rate and single-ended inputs only. Otherwise, Models 6106 and 6109 are identical.

Digitized data is stored in eight independent 1-ksample FIFOs; 16-ksample FIFO depth is optionally available.

## Interfaces

Output data can be delivered to the VMEbus, or to four front panel C40-compatible comm ports. Each comm port delivers data for two A/D channels. Alternately, the comm port associated with channels 1 and 2 can be programmed to deliver data for all channels.

The VMEbus interface provides full memory-mapped access to all FIFOs, interrupt controls, sample rate generators, status registers, and control registers. The FIFOs can be configured under software control to interrupt the VMEbus on full, half-full, and not empty conditions.

# **Sampling Rate Control**

The sampling clock can be supplied from one of four internal sample rate generators, or an external TTL sampling clock. The internal generators include programmable dividers to support four different sampling rates, one for each pair of A/D's. Sampling rates up to 2MHz (Model 6106) or 20 MHz (Model 6109) are supported.

# **Trigger Input**

A front panel TTL trigger input allows data collection to be initiated by positiveor negative-edge transitions, or gated by logic levels. A programmable sample counter interrupts the VMEbus after 2 to 256 samples have been collected.

# **Applications**

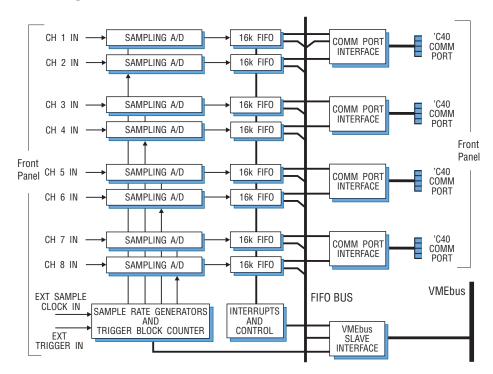
These models are ideal for real-time process control applications where latency and loop delay must be minimized.

As each sample is converted, it is immediately available to the selected interface because of the near-zero fall through time of the FIFOs. A minimum delay between conversion and processing is thus made possible. >

# Block Diagram, Models 6106, 6109

#### **Features**

- 8 channels with 14-bit or 12-bit resolution
- Internal or external sampling clocks to 2 MHz or 20 MHz
- VME and C40 comm port interfaces
- FIFO buffering for each converter output
- 8-Channel anti-aliasing lowpass filter, Model 6606
- Optional differential inputs (Model 6106 only)





# 8-Channel 14-bit 2 MHz A/D Converter VME Board 8-Channel 12-bit 20 MHz A/D Converter VME Board

## Anti-aliasing Filter (Contact Factory)

The Model 6606 is an 8-channel passive LC anti-aliasing filter VMEbus board. It provides a cutoff frequency of 800 kHz or, optionally, 8 MHz and is pin-for-pin compatible with the Models 6106 and 6109.

# **Specifications**

## Input Channels

Number: eight, any channel may be enabled or disabled Input, Model 6106 Single-ended: ±5.0 V full scale, 10 kohm input impedance Differential (option -005): ±10.0 V full scale, 10 kohm input impedance, ±9.0 V max. input with respect to

ground; 300 kHz small signal bandwidth

# Input, Model 6109

Single-ended: ±1.0 V full scale, ACcoupled with 10 kHz high-pass cutoff, 50 ohm input impedance

### A/D Converters

**Type:** ADS927 Model 6106; AD9042 Model 6109

Sampling rate: DC to 2 MHz, Model 6106; 5 to 20 MHz, Model 6109

Model Model

	6106	6109	
ion	: 14	12	h

Resolution:	14	12	bits
THD:	-84	-60	dB re FS
SNR:	76	50	dB
SFDR:	75	60	dB
11 01 1			

Sampling Clocks

**Frequency dividers:** four, one for each A/D pair; each divides internal or external reference by N, where N = 1 to 65536

**Internal reference:** 20 MHz (±100 ppm) **External reference:** 20 MHz max. optically-isolated TTL-compatible front panel input

#### Trigger/Gate Control

**Input:** optically-isolated TTL-compatible front panel input, or VMEbus control bit

**Trigger mode:** positive or negative edge starts conversion

Gate mode: logic '0' or '1' enables conversion

Sample counter: generates VMEbus interrupt N samples after trigger, where N = 2 to 256

#### **Output FIFO:**

**Model 6106:** 1 ksample per channel, optionally expandable to 16 ksamples **Model 6109:** 16 ksamples per channel

### **Comm Port Interface**

**Number:** four C40-compatible comm ports, one per pair of A/Ds **Data and control lines:** eight data plus

four control lines each

**Data format:** data is always transferred as four eight-bit bytes forming a 32-bit C40 long word

#### **Combined Port Mode**

Transfers: one comm port delivers data for up to eight channels Non-packed: one 14-bit sample leftjustified in 32-bit word, with 3 LSBs indicating channel ID Packed: two 14-bit samples left justified in both 16-bit fields of 32-bit long word, with two LSBs indicating channel pair ID

#### Independent Port Mode

Transfers: each comm port delivers data for one or two channels Non-packed: one 14-bit sample leftjustified in 32-bit long word, only one channel enabled per pair Packed: two 14-bit samples left-justified in both 16-bit fields of 32-bit word

#### **VMEbus** Interface

**Type:** slave A32 D32 I(1-7) **Transfers:** BLT (block level transfers), 16 k range per FIFO

**Control registers:** sample clock divisors, trigger/gate control, interrupt mask, channel enables, clock source, comm port modes, FIFO resets,

A24/A32 base address, interrupt vector register

**Status registers:** interrupt status, FIFO flags

**Memory map:** all FIFOs, control and status registers are mapped into A16 space; FIFOs are also mapped into A24/ A32 space

Maskable interrupts: FIFO status (full, half-full or not-empty conditions) and sample counter

Power: 3.0 A at +5 V; 0.5 A at ±12 V Size: standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 0.8 in. wide

## **Ordering Information**

		0	
	Model	Description	
	6106	8-Channel 14-bit 2 MHz A/D Converter VME board	
	6109	8-Channel 12-bit 20 MHz A/D Converter VME board	
Options:			
	-001	16 ksample FIFO (Model 6106 only)	
	-005	Differential inputs, Model	



PENTEK

6106 only