Model 78610

**General Information**

Model 78610 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 78610 includes a general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 78610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface completely the factory-installed functions and enable the 78610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

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### Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCIe Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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### Ordering Information

**Model Description**

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<th>Model</th>
<th>Description</th>
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<td>LVDS Digital I/O with Virtex-6 FPGA - PCIe</td>
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**Options:**

- `-062` XC6VLX240T
- `-064` XC6VSX315T
- `-104` LVDS FPGA I/O through 68-pin ribbon cable connector
- `-105` Gigabit serial FPGA I/O through two 4X top edge connectors
- `-155*` Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- `-165` Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

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**PCI Express Interface**

The Model 78610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.