General Information

Model 7650 is a half-length PCI Quad 200 MHz A/D. It consists of one Model 7150 Quad A/D mounted on a PCI carrier board. The Model 7650 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other module resources.

Virtex-5 FPGAs

The architecture includes two Virtex-5 FPGAs. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition to the built-in functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP with the factory-shipped functions.

The processing FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVDS I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 7650 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

A second Virtex-5 FPGA provides board interfaces including PCI-X or PCI Express. Implementing the PCI interfaces in this second FPGA, keeps the processing FPGA resources free for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but additional processing resources up to an additional 640 DSP48E Slices.

Option -104 installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs of LVDS connections to the interface FPGA for custom I/O.

Clocking and Synchronization

The architecture includes a flexible timing and synchronization circuit that allows the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus. ➤

Features

- Complete software radio interface solution
- Four or 200 MHz, 16-bit A/Ds
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
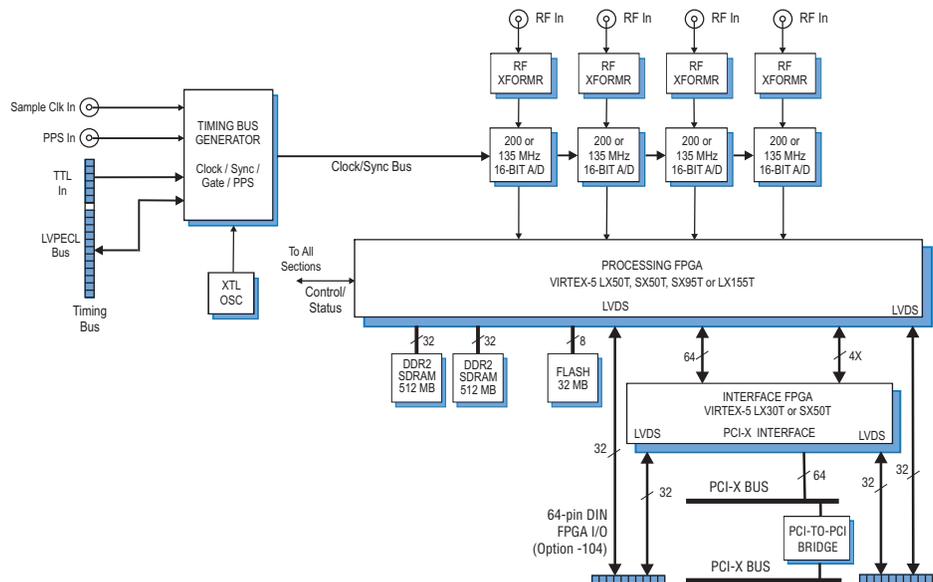
➤ Clocking and Synchronization

The timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 7650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. Each memory bank can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

PCI-X Interface

The Model 7650 includes an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes four separate DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33, 66 and 100 MHz are supported.

Optional PCI Express Interface

For systems that require a PCI Express board interface, the Model 7650 can be optionally factory-configured with x4 PCI Express in the interface FPGA. Other serial protocols as well as different bus widths can be accommodated with custom IP cores.

Specifications

Front Panel Analog Signal Inputs
  Input Type: Transformer-coupled, front panel female SMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

A/D Converters
  Type: Texas Instruments ADS5485
  Sampling Rate: 10 MHz to 200 MHz
  Internal Clock: 200 MHz crystal osc.
  External Clock: 10 to 200 MHz
  Resolution: 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock
  Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
  Sync/Gate Bus: 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array
  Processing FPGA: One Xilinx Virtex-5 XC5VSX50T; optional FPGAs include: XC5VLX50T, XC5VSX95T, XC5VLX155T and XC5VFX100T
  Interface FPGA: One Xilinx Virtex-5 XC5VLX30T; optional FPGA: XC5VSX50T

Custom I/O
  Available only with SX95T, LX155T and FX100T FPGAs
  Option -104: Installs a 64-pin DIN connector with 16 pairs of LVDS connections to the processing FPGA and 16 pairs to the interface FPGA for custom I/O

Memory
  DDR2 SDRAM: Up to 1 GB in two banks

PCI Interface
  PCI-X Bus: 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
  DMA: 4 channel demand-mode and chaining controller

Environmental
  Operating Temp: 0° to 50° C
  Storage Temp: –20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI card

Ordering Information

Model	Description
7650	Quad 200 MHz, 16-bit A/D with two Virtex-5 FPGAs - PCI

Options:

-104	FPGA I/O through a 64-pin DIN connector

Contact Pentek for additional available options.

PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com

www.pentek.com

A/D Performance

Spurious-Free Dynamic Range
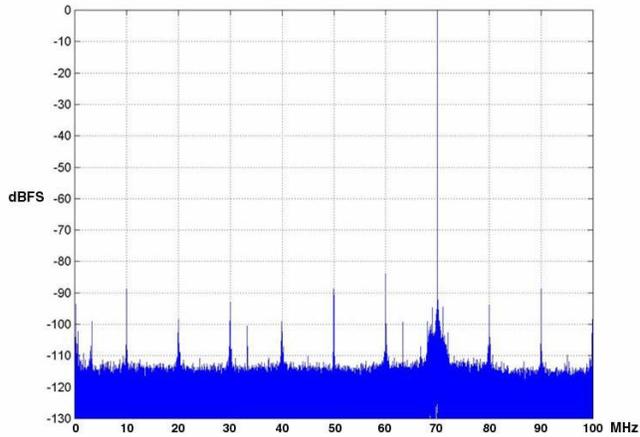
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup
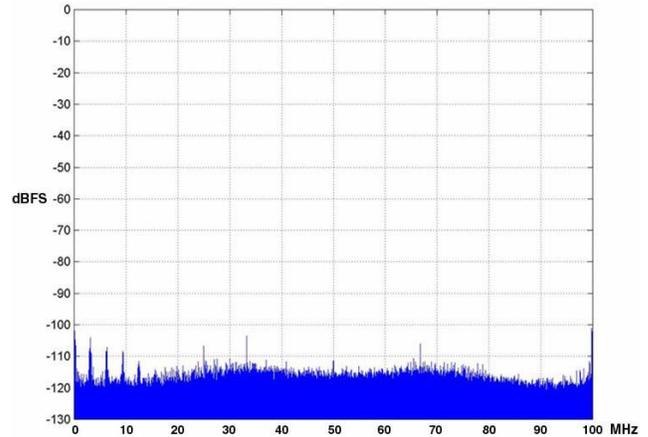
f_s= 200 MHz, Internal Clock

Input Frequency Response
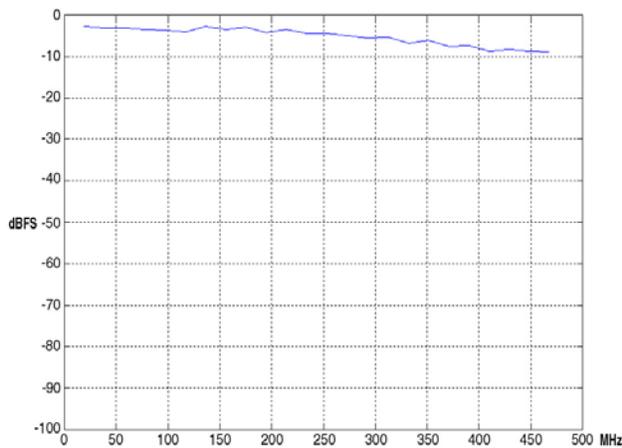
f_s= 200 MHz, Int. Clock

Two-Tone SFDR
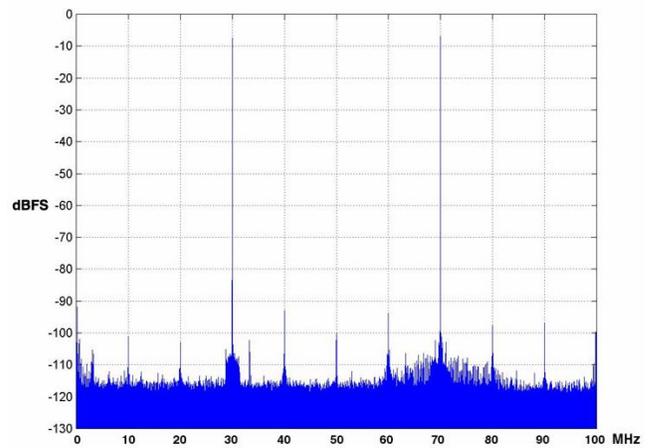
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk
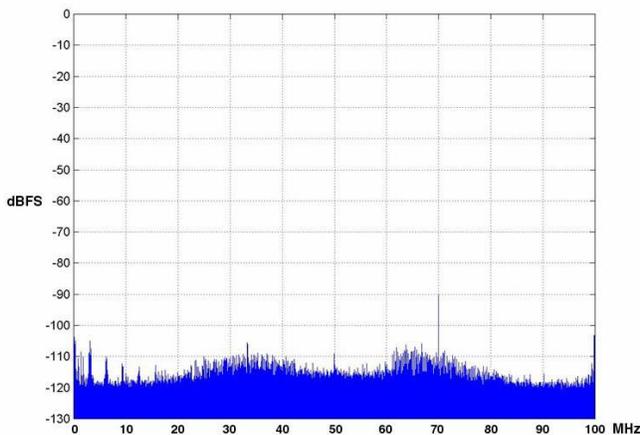
f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz

f_s= 200 MHz, Int. Clock