Model 7641

Dual Multiband Transceiver with FPGA - PCI

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio transceiver solution
- Two 125 MHz 14-bit A/Ds
- Input signal bandwidth up to 50 MHz
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O through a 64-pin DIN connector
- Optional factory-installed IP cores available

General Information

Model 7641 is a half-length PCI multiband transceiver. It consists of one Model 7141 transceiver mounted on a PCI carrier board. The Model 7641 attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on PCI slot panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter and D/A converters.

Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

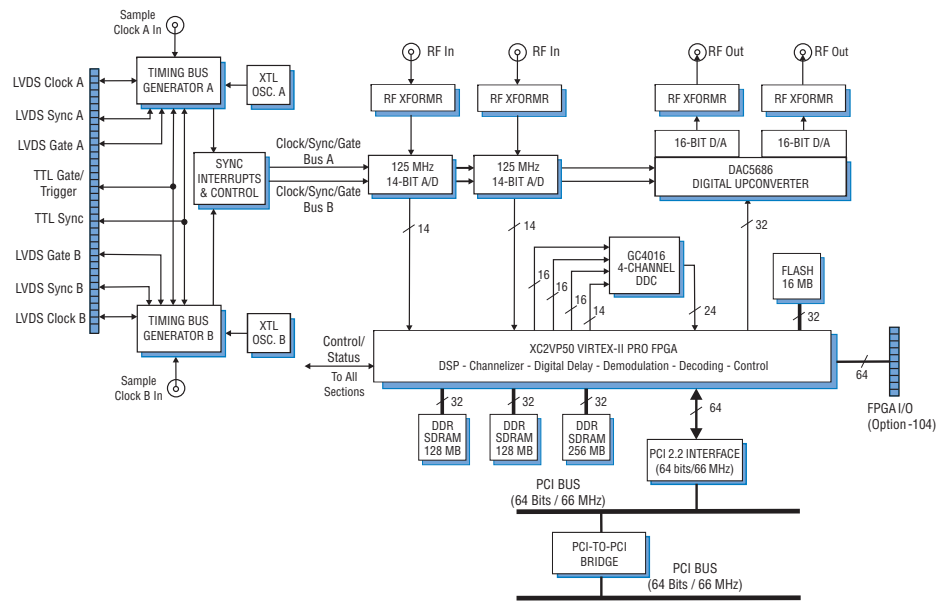
Option -104 adds a 64-pin DIN connector with 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as ➤



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➤ the timing source for the A/Ds, the downconverter, the upconverter and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7641's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

PCI Interface

The Model 7641 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal oscillator A or B
External Clock: 1 to 125 MHz
Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
Option -002: –2 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz
Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clocks

Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro
Option -050: XC2VP50
Option -104: Installs 64-pin DIN connector with 64 lines to the XC2VP50 FPGA

Memory

DDR SDRAM: 512 MB in three banks
FLASH: One bank of 16 MB

PCI Interface

PCI Bus: 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
Local Bus: 64-bit, 66 MHz
DMA: 9 channel demand-mode and chaining controller

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard PCI half-length board

Ordering Information

Model	Description
7641	Dual Multiband Transceiver with FPGA - PCI
Options:	
-002	Full-Scale Output: –2 dBm into 50 ohms; 3 dB Passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillator
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O through 64-pin DIN connector
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	GateFlow Installed core: Dual wideband DDC and interpolation filter
-430	GateFlow Installed core: 256-channel narrowband DDC

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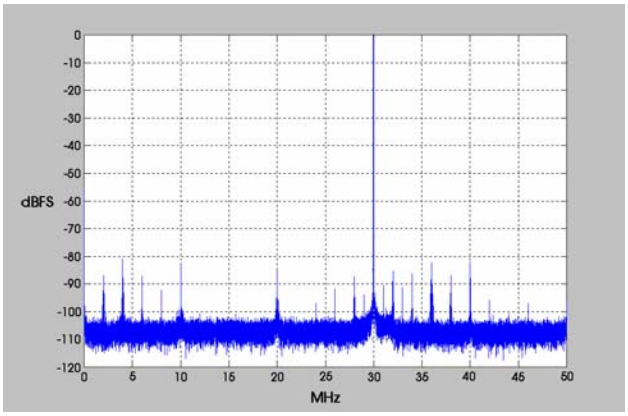
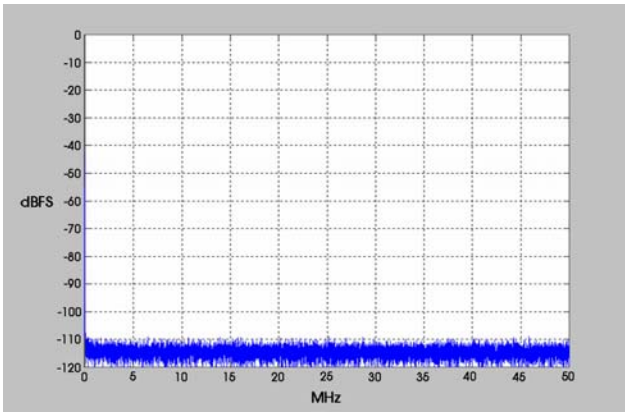
A/D Performance

Spurious Free Dynamic Range



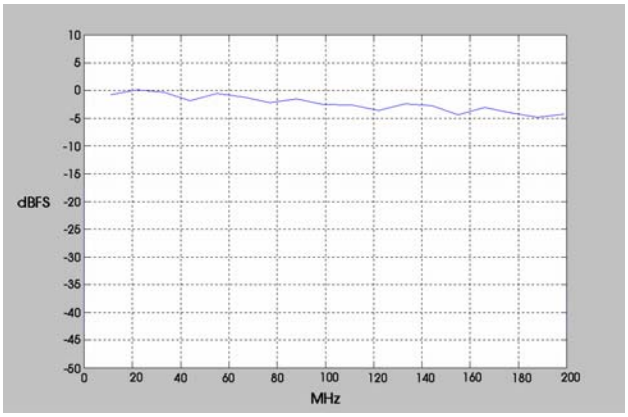
f_{in} = 70 MHz, f_s = 100 MHz

Spurious Pick-up



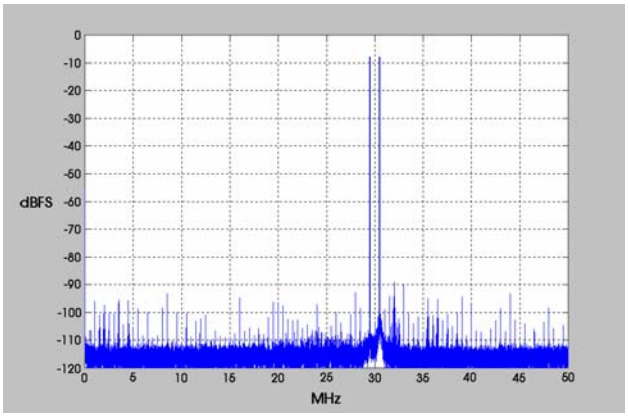
f_s = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



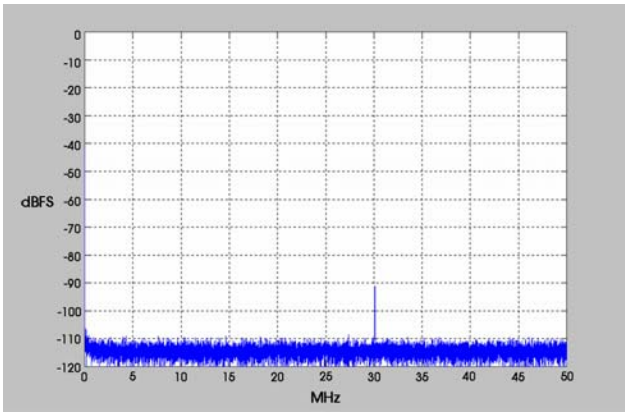
f_s = 100 MHz

Two Tone SFDR



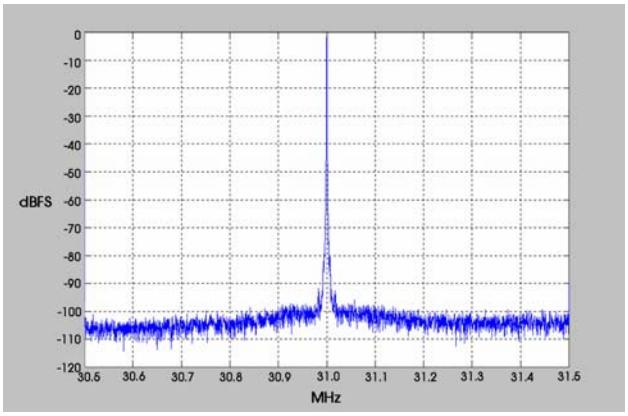
f_1 = 29.5 MHz, f_2 = 30.5 MHz, f_s = 100 MHz

Crosstalk



$f_{in\ Ch2}$ = 69 MHz, f_s = 100 MHz, Ch 1 shown

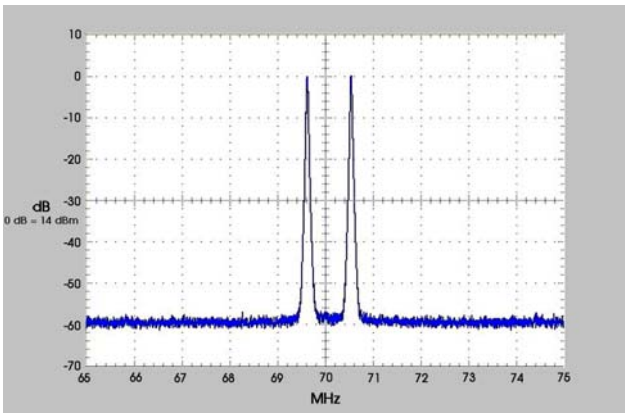
Phase Noise



f_{in} = 69 MHz, f_s = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz

D/A Performance

Two Tone Intermodulation Distortion



f_1 = 69.5 MHz, f_2 = 70.5 MHz, f_s = 100 MHz