New!

Models 72841, 73841 and 74841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

Model 74841 *Model 73841*

JADE

NAVIGATOR Design Suite

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex Ultra-Scale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization\
- Optional LVDS connections to the FPGA for custom I/O

General Information

Models 72841, 73841and 74841 are members of the Jade™ family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a cPCI carrier board. Model 72841 is a 6U cPCI board while the Model 73841 is a 3U cPCI board; both are equipped with one Model 71841 XMC. Model 74841 is a 6U cPCI board with two XMC modules rather than one.

They include one or two A/Ds, programmable DDCs, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

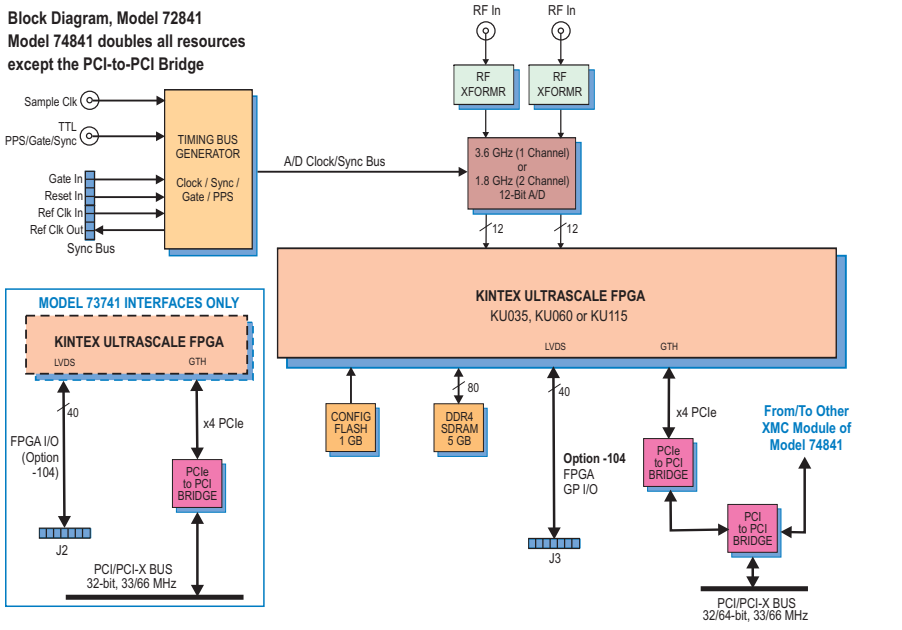
Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. ➤



PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Models 72841, 73841 and 74841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation .

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 (or J2 connector, Model 73841) for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

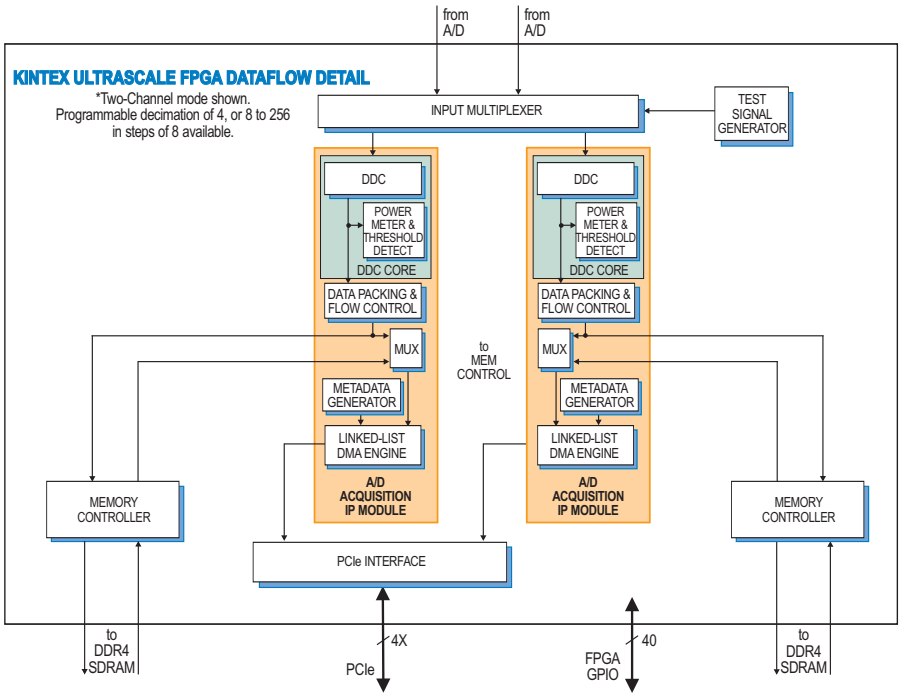
The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high- speed sync boards to drive the sync bus. ➤



PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

Ordering Information

Model	Description
72841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI
73841	1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 3U cPCI
74841	2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI
Options:	
- 084	XCKU060-2 FPGA
- 087	XCKU115-2 FPGA
-104	LVDS I/O between the FPGA and J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841
-702	Air cooled, Level L2

➤ Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek- supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73841: 32 bits only.

Specifications

Model 72841 or Model 73841: One A/D
Model 74841: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841

Memory Banks (1 or 2)
Type: DDR4 SDRAM
Size: One or two banks, 5 GB each
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73741: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Standard 6U or 3U cPCI board

PENTEK
Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com