

New!

Models 7290, 7290D and 7390

Multifrequency Clock Synthesizers - 3U/6U cPCI



Model 7390 Model 7290D

Features

- Simultaneous synthesis of up to five different clocks
- Eight or 16 SMC clock outputs
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Quad VCXOs allow selection from different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface



Ordering Information

Model	Description
7290	Multifrequency Clock Synthesizer - 6U cPCI
7290D	Dual Multifrequency Clock Synthesizer - 6U cPCI
7390	Multifrequency Clock Synthesizer - 3U cPCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

These Models generate up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Models 7290 and 7390 generate eight clocks while Model 7290D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a

wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input

Connector Type: SMC

Input Impedance: 50 ohms

Reference Frequency: 5 to 100 MHz

Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners

Quantity: Four or eight

Type: Texas Instruments CDC7005

Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four or eight)

Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz

Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)

Connector Type: SMC

Output Impedance: 50 ohms

Output Level: +3 dBm @ 700 MHz

Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)

Operation: control and status interface

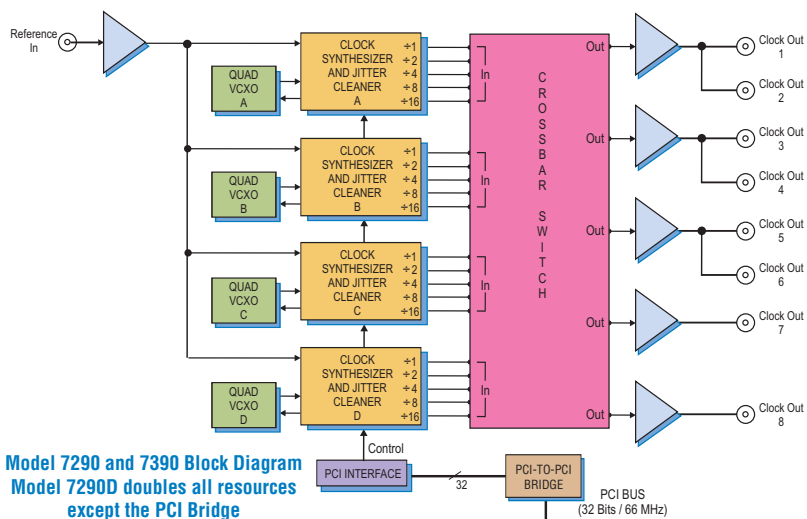
Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board



Model 7290 and 7390 Block Diagram
Model 7290D doubles all resources except the PCI Bridge