



Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable serial gigabit interfaces
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

General Information

Model 71662 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe

interface complete the factory-installed functions and enable the 71662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

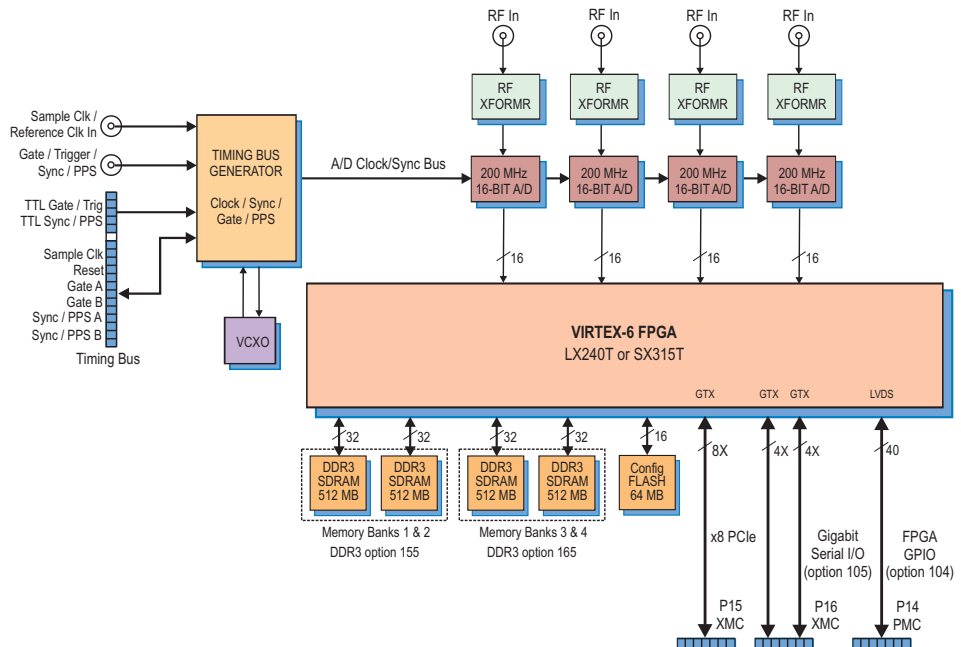
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols. ➤



A/D Acquisition IP Modules

The 71662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64

from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 * f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

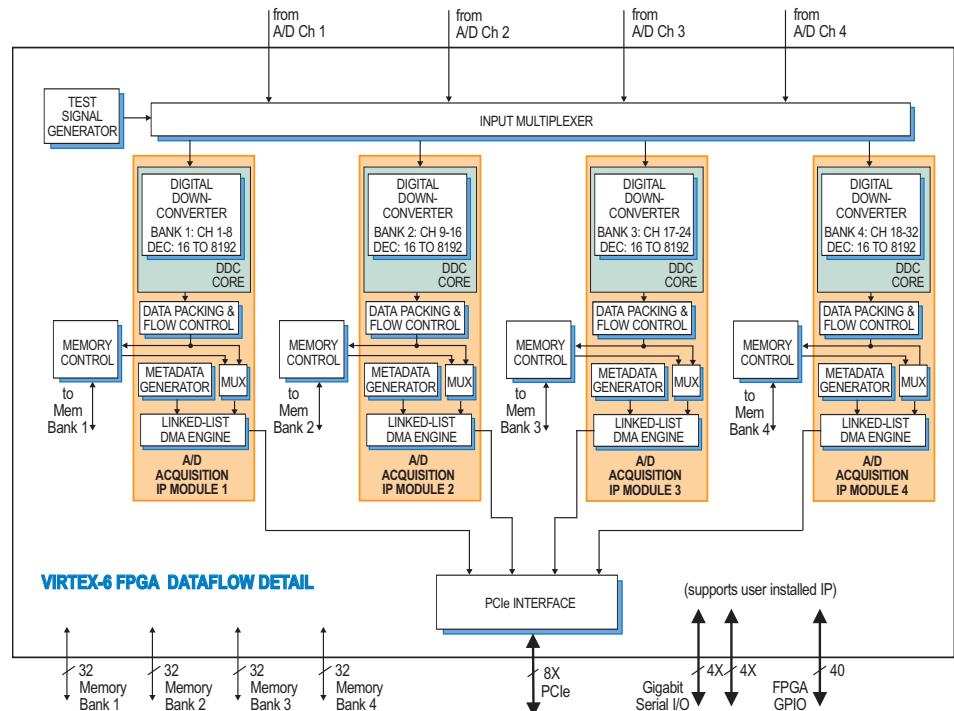
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.



► Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



Ordering Information

| Model | Description |
|-----------------|---|
| 71662 | 4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC |
| Options: | |
| -062 | XC6VLX240T |
| -064 | XC6VSX315T |
| -104 | LVDS FPGA I/O through P14 connector |
| -105 | Gigabit serial FPGA I/O through P16 connector |
| -155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2) |
| -165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |
| -702 | Air cooled, Level L2 |
| -713 | Conduction cooled, Level L3 |

Contact Pentek for availability of rugged and conduction-cooled versions

| Model | Description |
|-------|--|
| 8266 | PC Development System See 8266 Datasheet for Options |

XMC Interface

The Model 71662 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71662 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Four 8-channel banks, one per acquisition module

Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
LO Tuning Freq. Resolution: 32 bits, 0 to f_s

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8;

Gen. 2: x4

Environmental

Standard: L0 Air-Cooled

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Option -702: L2 Air-Cooled

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Sine Vibration: 2g, 20-500 Hz

Random Vibration: 0.04g²/Hz, 20-2000 Hz

Shock: 20 g, 11 ms

Option -713: L3 Conduction-Cooled

Operating Temp: -40° to 70° C

Storage Temp: -40° to 100° C

Sine Vibration: 10g, 20-2000 Hz

Random Vibration: 0.1g²/Hz, 20-2000 Hz

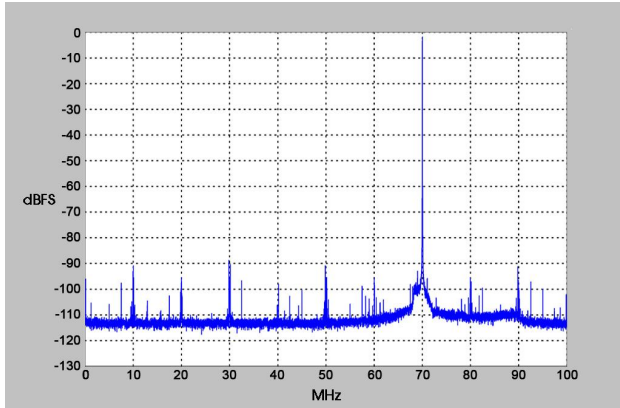
Shock: 30 g, 11 ms

Relative Humidity: 0 to 95%, non-condensing

Size: Standard XMC module, 2.91 in. x 5.87 in.

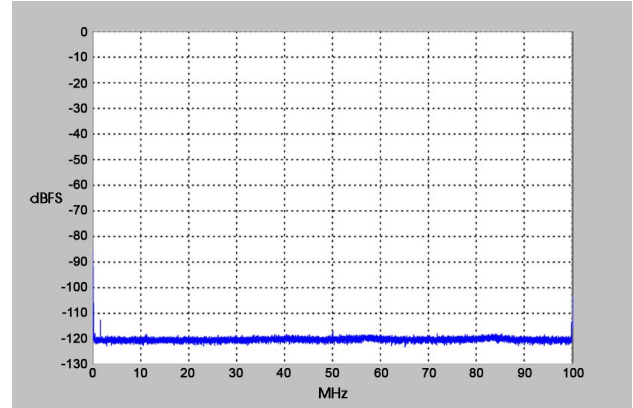
A/D Performance

Spurious Free Dynamic Range



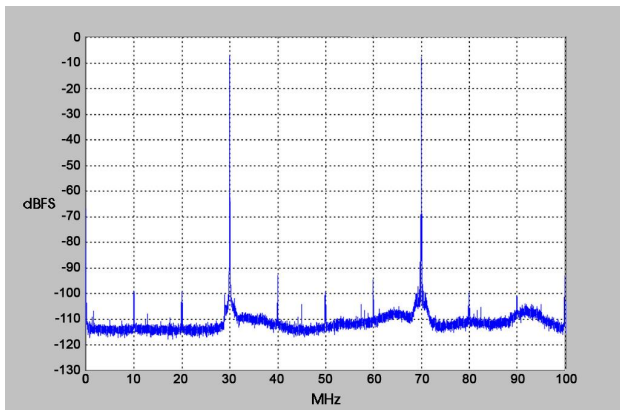
$f_{in} = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$, Internal Clock

Spurious Pick-up



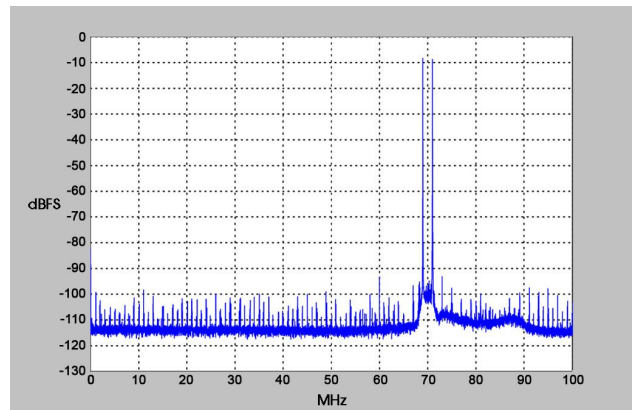
$f_s = 200 \text{ MHz}$, Internal Clock

Two-Tone SFDR



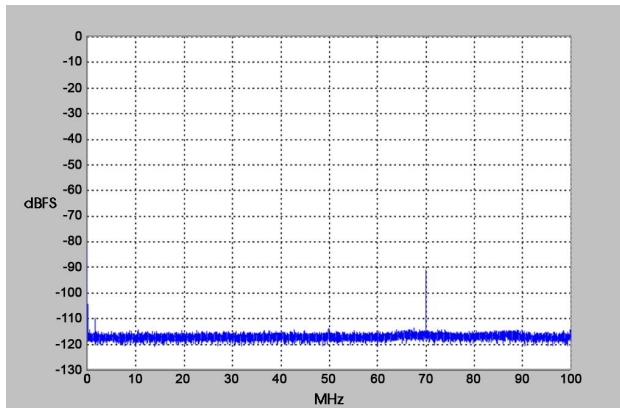
$f_1 = 30 \text{ MHz}$, $f_2 = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$

Two-Tone SFDR



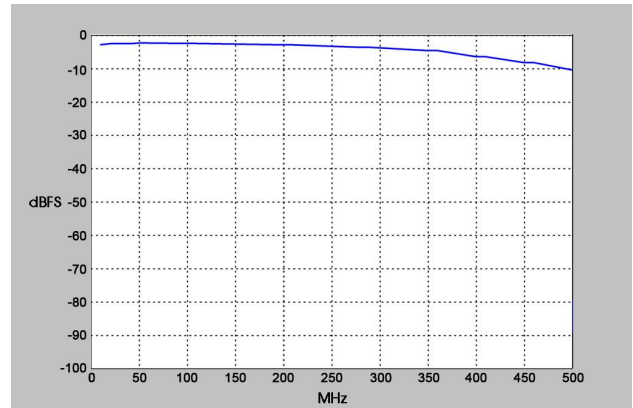
$f_1 = 69 \text{ MHz}$, $f_2 = 71 \text{ MHz}$, $f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}$, $f_s = 200 \text{ MHz}$, Ch 1 shown

Input Frequency Response



$f_s = 200 \text{ MHz}$, Internal Clock