# Model 7141-703

# Dual Multiband Transceiver with FPGA - Ruggedized PMC/XMC

GateFlow ReadyFlow Board Support Package

## Features

- Complete software radio transceiver solution
- VITA 42.0 XMC compatible
- Two 125 MHz 14-bit A/Ds
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multi-module synchronization
- 28 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O on P4
- Optional factory-installed IP Cores available

## General Information

Model 7141-703 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It includes two A/D and two D/A converters capable of bandwidths to 40 MHz and above. The Model 7141-703 uses the popular PMC format and supports the emerging VITA 42 XMC standard with optional switched fabric interfaces. The Model 7141-703 is offered as a fully conduction-cooled/ruggedized board meeting Pentek's L3 ruggedization level (option 703).

## A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

## Digital Downconverter Stage

A TI/Graychip GC4016 quad digital downconverter accepts either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/D converters, FPGA signal processing engines, SDRAM delay memory and data sources on the PCI bus.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining two or four channels, output bandwidth of up to 5 or 10 MHz can be achieved.

## Digital Upconverter Stage

A TI DAC5686 digital upconverter (DUC) and dual D/A accepts baseband real or complex data streams from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel SSMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

## Virtex-II Pro FPGA

The Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with data and programming interfaces to each of the on-board resources including the A/D converters, GC4016 digital downconverter, digital upconverter, and D/A converters.

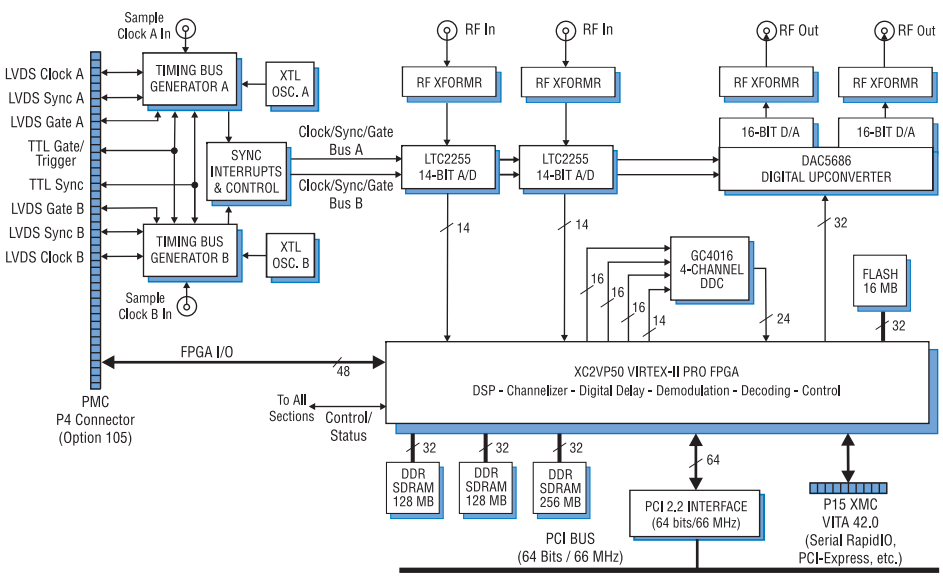
Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

Option -105 adds the P4 PMC connector with 28 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O.

The FPGA includes two PowerPC cores which can be used as local microcontrollers to create complete application engines.

## Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals. ➤





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## XMC Interface

The Model 7141-703, option 520 complies with the VITA 42.0 XMC specification for carrier boards. This emerging standard defines a 4X link with a 3.125 GHz bit clock between the XMC module and the carrier board.

With two 4X links, the 7141-703 achieves 2.5 GB/sec streaming data transfer rate independent of the PCI interface and can support switched fabric protocols such as Serial RapidIO and PCI Express.

## Software Support

The Pentek ReadyFlow Board Support Package and VxWorks, Linux and Windows device drivers for specific embedded processor boards and operating systems, speed software development tasks.

The Pentek GateFlow FPGA Design Kit facilitates user-installed FPGA functions using the Xilinx ISE Foundation tool suite. The FPGA Design Kit allows the user to configure FPGAs for implementing preprocessing functions such as convolution, framing, pattern recognition or decompression.

## Ordering Information

| Model | Description |
|---|---|
| 7141 | Multiband Transceiver with FPGA - PMC/XMC |
| **Options:** | |
| -050 | XC2VP50 Virtex-II Pro FPGA |
| -100 | 100 MHz Bus A and Bus B internal oscillators |
| -125 | 125 MHz Bus A and 100 MHz Bus B oscillators |
| -105 | FPGA I/O and sync bus through P4 connector |
| -5xx | XMC interface |
| -703 | Level L3 - Ruggedized & conduction-cooled version |

➤ Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverter, the upconverter, and the D/As. Both timing buses accept clocks from two external reference clocks or two internal oscillators.

Timing signals for both Bus A and B are available on the P4 PMC connector allowing multiple modules to be synchronized. In the slave mode, differential LVDS inputs drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple modules.

Up to seven slave 7141-703's, can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards. Up to 80 boards may be synchronized with a Model 9190 Clock and Sync Generator.

## Memory Resources

Three independent banks of SDRAM are available to the FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

## PCI Interface

The Model 7141-703 includes an industry-standard interface fully compliant with PCI 2.2 bus specifications. The interface includes nine separate DMA controllers for efficient transfers to and from the module.

Data widths of 32 or 64 bits and data rates of 33 or 66 MHz are supported.

## Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMCX connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +10 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 300 MHz

**A/D Converters**
- **Type:** Linear Technology LTC2255
- **Sampling Rate:** 1 MHz to 125 MHz
- **External Clock:** 1 to 125 MHz
- **Resolution:** 14 bits
- **Clock Source:** Timing Bus A or B

**Digital Downconverter**
- **Type:** TI/Graychip GC4016
- **Decimation:** 32 to 16,384; with channel combining mode: 8 or 16
- **Data Source:** A/D, FPGA, or PCI interface
- **Control Source:** FPGA or PCI interface
- **Output:** Parallel complex data

**Receiver Bypass Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

**Front Panel Analog Signal Outputs**
- **Output Type:** Transformer-coupled, front panel female SSMCX connectors
- **Full Scale Output:** +4 dBm into 50 ohms (other options available)
- **3 dB Passband:** 60 kHz to 300 MHz (other options available)

**Digital Upconverter**
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz, max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits
- **Clock Source:** Timing Bus A or B

**Timing Buses A & B:** Clocks selectable from onboard crystal oscillators, external or LVDS bus, gates and syncs from LVDS bus

**External Clocks:** Front panel female SSMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

**P4 Timing Bus:** Available as option 105, dual clock/sync/gate input/output LVDS buses; one sync TTL input, one gate TTL input

**Field Programmable Gate Array**
- **Type:** Xilinx Virtex-II Pro
- **Option -050:** XC2VP50
- **Option -105:** Installs P4 connector with 56 lines to the XC2VP50 FPGA

**Memory**
- **DDR SDRAM:** 512 MB in three banks
- **FLASH:** One bank of 16 MB.

**PCI Interface**
- **PCI Bus:** 64-bit, 66 MHz (also supports 32-bit and/or 33 MHz)
- **Local Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller

**Environmental (Level L3):**
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Sine Vibration:** 10 g, 20–2000 Hz
- **Random Vibration:** 0.1 $g^2$/Hz, 20–2,000 Hz
- **Shock:** 30 g, 11 msec
- **Relative Humidity:** 0 to 95%, non-condensing; 0 to 100% with conformal coating

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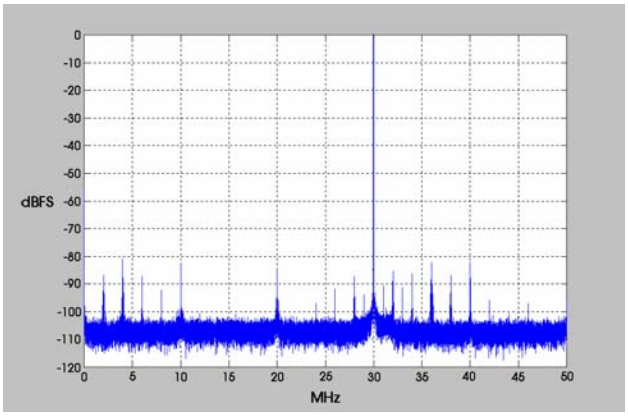
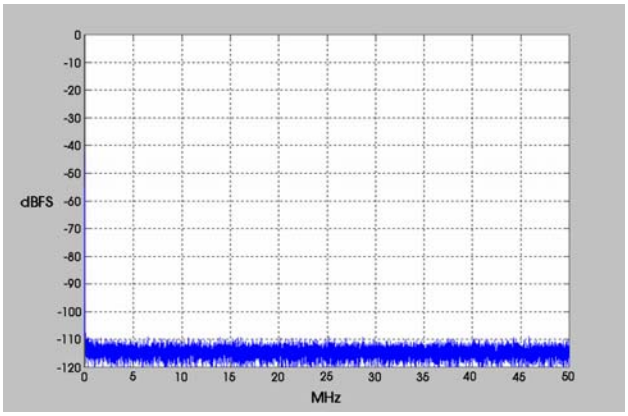
## A/D Performance

Spurious Free Dynamic Range



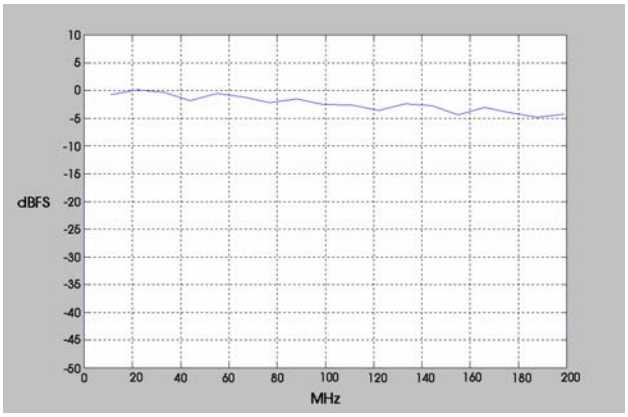

$f_{in}$ = 70 MHz, $f_s$ = 100 MHz

Spurious Pick-up



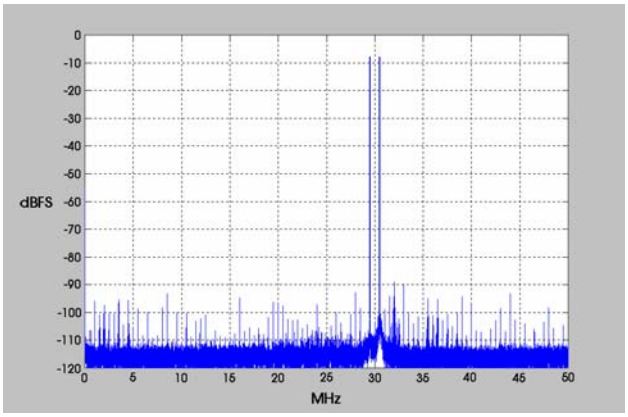

$f_s$ = 100 MHz, 32k point FFT, 8 averages

Input Frequency Response



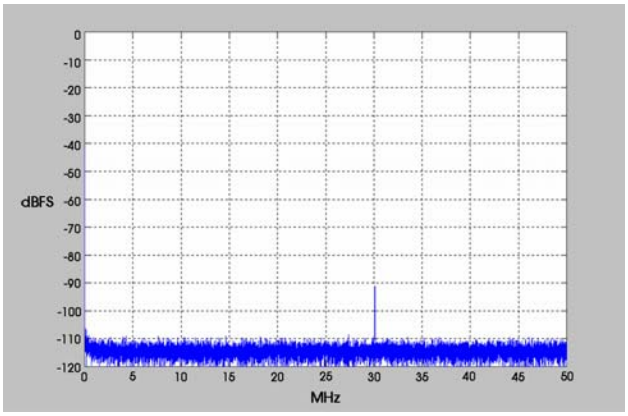

$f_s$ = 100 MHz

Two Tone SFDR



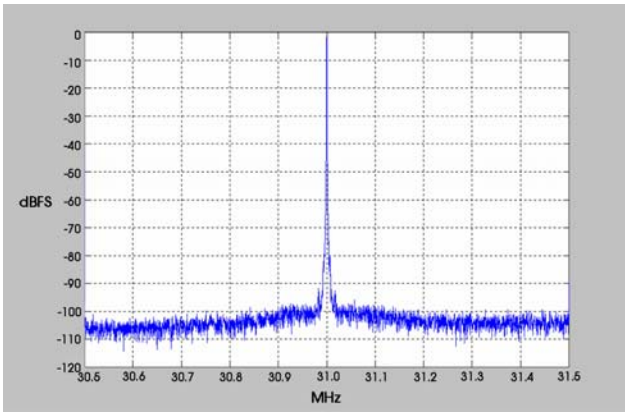

$f_1$ = 29.5 MHz, $f_2$ = 30.5 MHz, $f_s$ = 100 MHz

Crosstalk




$f_{in\ Ch2}$ = 69 MHz, $f_s$ = 100 MHz, Ch 1 shown

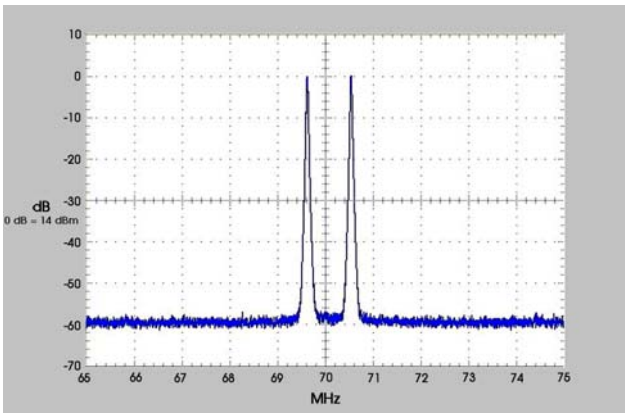
Phase Noise




$f_{in}$ = 69 MHz, $f_s$ = 100 MHz
Phase Noise @ 100 kHz = -102 - 10*log(610) = -129.8 dB/Hz

## D/A Performance

Two Tone Intermodulation Distortion




$f_1$ = 69.5 MHz, $f_2$ = 70.5 MHz, $f_s$ = 100 MHz