

New!

# FlexorSet Model 7070-324

## 4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - x8 PCIe



Model 7070-324



### Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input data rate, 2 GHz output sample rate with interpolation)
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

### General Information

Model 7070-324 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3324 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

### The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data

multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

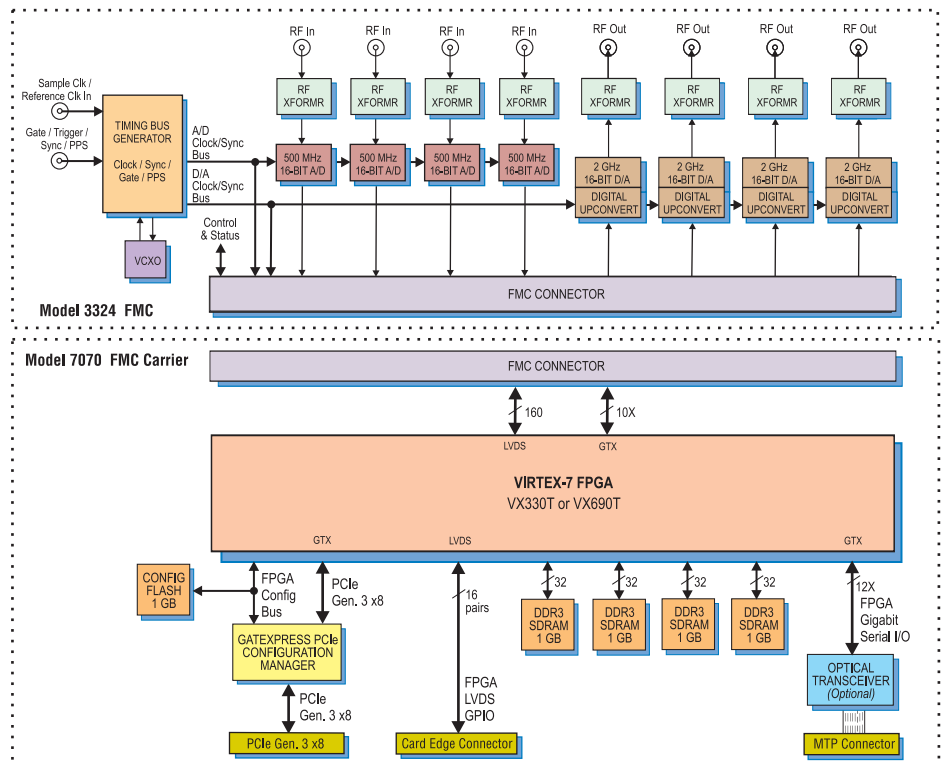
The 7070-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-324 to operate as a turnkey solution without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their custom ▶



**A/D Acquisition IP Modules**

The 7070-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Modules**

The 7070-324 factory-installed functions include four sophisticated D/A Waveform Playback IP modules. A linked-list control allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

► IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The 7070-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on the PCIe slot panel.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is

especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

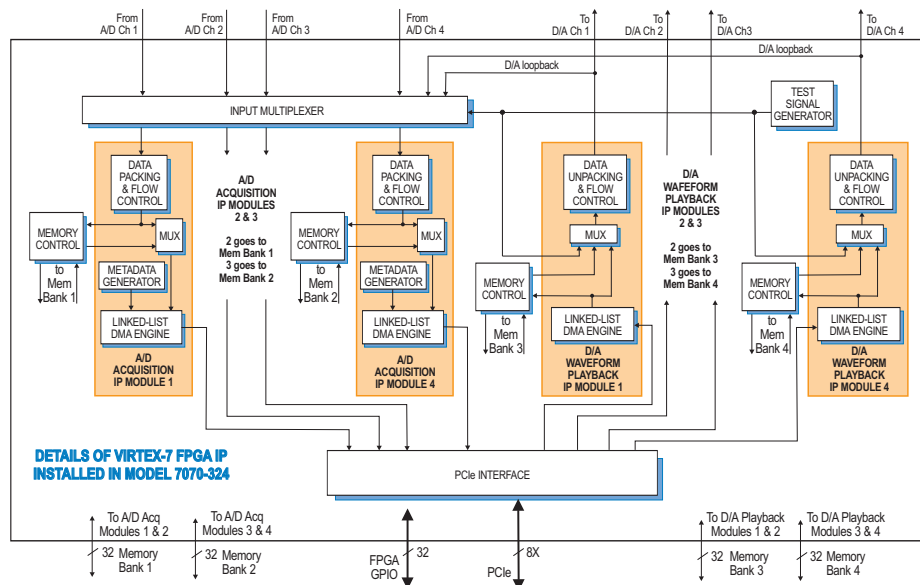
Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed.

In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space ►



### PCI Express Interface

The Model 7070-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Memory Resources

The 7070-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

### Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.



### Ordering Information

Model	Description
7070-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe

#### Options:

-076	XC7VX690T-2 FPGA
-104	LVDS FPGA I/O to card-edge connector
-110	12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model	Description
8266	PC Development System See 8266 Datasheet for Options

▶ allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

### A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into 500 MHz, 16-bit A/D converters.

### Digital Upconverter and D/A Stage

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

### Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

### Specifications

#### Front Panel Analog Signal Inputs

**Input Type:** Transformer-coupled, front panel connectors

**Transformer Type:** Coil Craft WBC1-1TLB

**Full-Scale Input:** +4 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 750 MHz

#### A/D Converters

**Type:** Texas Instruments ADS54J69

**Sampling Rate:** Up to 500 MHz

**Resolution:** 16 bits

#### Front Panel Analog Signal Outputs

**Output Type:** Transformer-coupled, front panel connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full-Scale Output:** +4 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

#### D/A Converters

**Type:** Texas Instruments DAC38J84

**Input Data Rate:** Up to 500 MHz

**Output Sample Rate:** Up to 2 GHz (with interpolation)

**Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

#### Clock Synthesizer

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

#### External Clock

**Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

#### External Trigger Input

**Type:** Front panel connector

**Function:** Programmable functions include: trigger, gate, sync and PPS

#### Field Programmable Gate Array

**Standard:** Xilinx Virtex-7 XC7VX330T-2

**Option -076:** Xilinx Virtex-7 XC7VX690T-2

#### Custom FPGA I/O

**Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O

**Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

#### Memory

**Type:** DDR3 SDRAM

**Size:** Four banks, 1 GB each

**Speed:** 800 MHz (1600 MHz DDR)

#### PCI-Express Interface

**PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

**Environmental:** Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)