Model 6821
Model 6822

215 MHz, 12-bit A/Ds with Virtex-II Pro FPGAs - VME/VXS

Model 6822 standard single slot (left) and conduction-cooled version.

ReadyFlow Board Support Package
GateFlow
VXS

Features

- One or two AD9430 12-bit, 215 MHz A/D converters
- Xilinx Virtex-II Pro FPGAs
- Dual 4X VXS links for Serial RapidIO
- I/F input up to 700 MHz
- Four FPDP or FPDP II front panel ports
- FIFO data buffering
- Multiboard synchronization
- ***Ruggedized and conduction-cooled versions available***

General Information

Models 6821 (single-channel) and 6822 (dual-channel) are complete high-frequency A/D converters in a 6U VMEbus form factor. They accept one or two front panel analog inputs and deliver digital output samples over two or four FPDP ports utilizing FPDP or FPDP II standards. These Models are ideal as high-speed data acquisition front ends for real-time recording, digital receivers, and DSP systems.

Input Stage and A/D Converters

Front panel female SMA connectors accept analog RF inputs at a full scale level of +8 dBm or +2 dBm (software selectable) into the primary of RF transformers that present 50 ohm input impedance. The transformers offer low-distortion paths to the differential inputs of the Analog Devices AD9430 A/Ds, with flat frequency response from 400 kHz to 700 MHz (standard).

Clocking, Gating and Triggering

The A/D converter sample clock can be sourced from an internal 210 MHz crystal oscillator or from an externally supplied sinusoidal clock of 215 MHz, maximum. This clock is accepted through a front panel SMA connector terminated in 50 ohms.

An external LVDS bus supports synchronous data acquisition across multiple boards. This is ideal for applications such as multichannel radar systems.

Virtex-II Pro FPGAs

Both Models utilize two Xilinx Virtex-II Pro Series FPGAs. Each FPGA is optionally equipped with 128 MB of SDRAM and 16 MB of FLASH memory.

Each FPGA accepts 12-bit signals at the sampling frequency from the A/D converter. Several data packing modes are selectable across the multiple FPDP ports. The FPGAs also act as controllers for other board functions including gating and triggering.

Optional LVDS I/O is available through either the VMEbus P2 connector or a second-slot front panel mezzanine.

FIFOs and FPDP Outputs

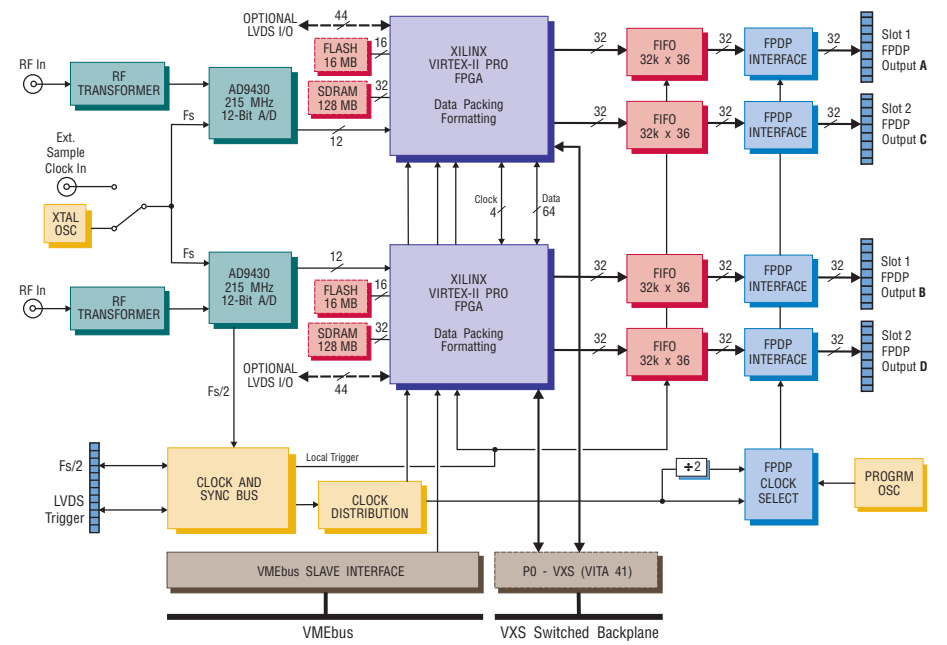
Following each FPGA are two 32-bit wide FIFO buffers with standard depth of 32k words. These FIFOs are useful as elastic memory to support hard disk latencies in recording applications.

A total of four FPDP output ports are available, two per FPGA, to support data transfers of 320 MB/sec each or greater. One port per FPGA is attached to the board's front panel, with the second attached to an optional second-slot front panel.

A data demultiplexing mode splits the data stream between each pair of FPDP ports, reducing the output data rate by a factor of up to four (depending on the data packing mode and number of FPDP ports) to support slower FPDP devices.

Optional VXS Interface

Both Models provide optional full duplex VITA-41 VXS links to the VME P0 connector for both FPGAs. These links support 4X Serial RapidIO, or other switched fabrics such as PCI Express and Xilinx Aurora. ➤



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Model 6821
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➤ Switchless VXS Card Cage

A five-slot card cage with full fabric support for three payload cards without the need for a switch card is now available for developing and testing VXS cards.

Specifications

Front Panel Analog Signal Inputs
- **Quantity:** Model 6821: 1, Model 6822: 2
- **Input Type:** Transformer-coupled, front panel female SMA connector
- **Full Scale Input:** +8 dBm (1.59 V p-p) or + 2 dBm (0.796 V p-p), software selectable, into 50 ohms
- **Input Bandwidth:** 150 MHz
- **Transformer 3 dB Passband:** 400 kHz to 700 MHz (other values optionally available)

A/D Converter
- **Quantity:** Model 6821: 1, Model 6822: 2
- **Type:** Analog Devices AD9430-210
- **Sampling Rate:** 60 MHz to 215 MHz
- **Internal Clock:** 210 MHz crystal osc. std.; 213.333 MHz crystal osc. optional
- **External Clock:** 60 to 215 MHz
- **Resolution:** 12 bits
- **Bandwidth:** 700 MHz at full power

Clock Source: Onboard crystal oscillator, front panel external clock

External Clock: Front panel female SMA connector, sine wave, 0 to +4 dBm, AC coupled, 50 ohms impedance

Sync/Gate Bus: One 26-pin connector with one clock, one FPGA sync, and four gate input/output LVDS signals; one sync and one gate input TTL signals

Field Programmable Gate Arrays
- **Quantity:** 2, both Models
- **Type:**
- **Option -050:** Virtex-II Pro XC2VP50-5
- **Option -020:** Virtex-II Pro XC2VP20-5
- **FPGA I/O:**
- **Option -222:** Adds one 68-pin connector per FPGA through a second-slot front panel; each connector provides thirty two LVDS data I/O differential pairs, two LVDS clock I/O pairs and four control I/O pairs
- **Option -121:** Provides twenty four LVDS differential data I/O pairs, two clock I/O pairs and four control pairs from FPGA2 to VMEbus P2 connector (not available with XC2VP20)

Memory

SDRAM:
- **Quantity:** 2 banks, 1 per FPGA
- **Size:** 128 MB per bank (256 MB total)
- **Bus Width:** 32 bits
- **Speed:** 133 MHz

FLASH:
- **Quantity:** 2, 1 per FPGA
- **Size:** 16 MB each (32 MB total)
- **Bus Width:** 16 bits

Front Panel Data Port (FPDP) Outputs
- **Quantity:** 2 standard; 4 with option -224 (additional ports located on second-slot front panel)
- **Output Type:** non-inverted configuration, FPDP I or FPDP II
- **Clock:** Onboard programmable oscillator (up to 50 MHz), or sample clock with one line to each FPDP port

FIFOs
- **Quantity:** 2 standard (one per FPDP port), 4 with option -224
- **Size:** 32,768 x 36
- **Speed:** Sample clock rate ÷ 2

VME Slave Interface
- **Type:** Slave A16/D16, A16/D32 (A32/D32 programmable)
- **Control:** Operating modes, gate/trigger, FIFO reset, data packing, FPDP I/II selection, FPDP framing, time sync command, status

Power
- **Default Configuration:** 19 W
- Note: User FPGA designs will increase power consumption, normally within the following ranges:
- **With XC2VP20 FPGAs:** from 28 W to 38 W maximum
- **With XC2VP50 FPGAs:** from 41 W to 62 W maximum

Environmental (Commercial version)
- **Pentek Ruggedization Level:** L0
- **Cooling Method:** Forced air
- **Operating Temp:** 0 to 50° C
- **Storage Temp:** –20 to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

Environmental - Option -703
- **Pentek Ruggedization Level:** L3
- **Cooling Method:** Conduction cooling
- **Operating Temp:** –40 to 70° C
- **Storage Temp:** –50 to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Sine Vibration:** 10 g, 20–2,000 Hz
- **Random Vibration:** 0.1 g^2/Hz, 20–2,000 Hz
- **Shock:** 30 g, 11 ms

Environmental - Option -720
- **Relative Humidity:** 0 to 100% non-condensing with conformal coating

Size: Standard 6U VMEbus board, single slot; board 160 mm (6.3 in.) x 233.5 mm (9.2 in.), panel 20.3 mm (0.8 in) wide; Option -222 or -224: 40.6 mm (1.6 in) wide

Weight: 425 grams (15 oz.); 794 grams (28 oz.) conduction-cooled version

Ordering Information

Model	Description
6821	Single 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS
6822	Dual 215 MHz, 12-bit A/D with Virtex-II Pro FPGAs - VME/VXS
Options:	
-020	XC2VP20 FPGAs
-050	XC2VP50 FPGAs
-121	LVDS I/O thru P2
-213	213.333 MHz crystal oscillator
-222	2nd Slot LVDS I/O
-224	2nd Slot FPDP I/O
-234	FPDP for conduction-cooled version
-340	128 MB SDRAM and 16 MB FLASH per FPGA
-422*	Wideband Ultra High-Speed DDC IP Core factory-installed
-5xx	VXS Interface
-70x	Ruggedized & conduction-cooled versions

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