Model 6235 Installed FFT Core

GateFlow Dual Channel Wideband FFT Receiver - VIM-2

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Features

- Dual 12-bit 105 MHz A/Ds
- Dual wideband receivers
- Built-in real-time 105 MHz 1k or 4k FFT Processor
- Radar preprocessor
- Energy detection for signal intelligence receivers
- Offloads DSP processing
- Suitable for IF signals up to 150 MHz
- Ready To Use - No FPGA programming required

General Information

The Model 6235 Dual Wideband Digital Receiver includes two complete data acquisition and receiver channels in a VIM-2 mezzanine module compatible with all VIM-compatible platforms, including the Pentek C6000 and PowerPC processor boards.

Model 6235 utilizes two AD9432 105 MHz 12-bit A/Ds and two GC1012B wideband digital receivers.

In the standard module, the Virtex-II FPGA contains factory programmed code to implement control, initialization, mode selection and data formatting functions. However, much of the FPGA remains available for custom signal processing.

Extended versions of the standard FPGA functions are now available which include GateFlow Installed IP Cores that perform real-time FFT (Fast Fourier Transform) algorithms. With either option installed, all existing operational modes of the 6235 module remain intact. Option -401 provides a 1024-point FFT and option -404 provides a 4096-point FFT. Only one of these options may be installed in a 6235 module.

FFT Operation

The block diagram below shows the signal flow paths and processing blocks for both FFT options. The switches are programmable multiplexers controlled through the VIM status/control interface. In order to take advantage of symmetrical pipelined processing, these switch mode settings must be the same for both channels.

The FFT can process output samples from the A/D or the digital receiver. At the user's option, a Hanning window may be applied to the selected FFT input source.

The FFT block utilizes a complex radix-4 algorithm with five or six butterfly stages for the 1024- or 4096-point algorithms, respectively. Several advanced noise reduction techniques employed in the algorithms deliver a spurious free dynamic range for the FFT calculation of better than 90 dB.

The FFT output points are reordered (deinterleaved) and may be delivered either as complex I & Q values or routed through a sum-of-squares power calculator.

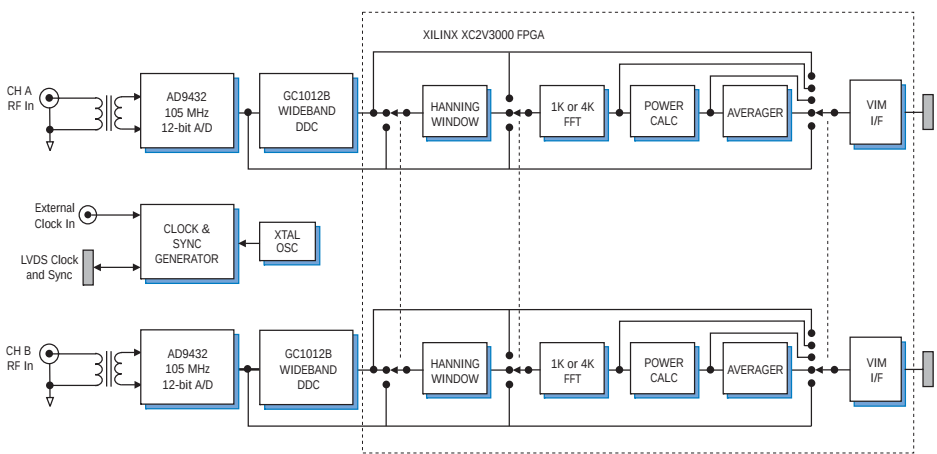
An optional averager permits averaging of up to four outputs in the single channel mode or two outputs in the dual channel mode prior to delivery through the VIM interface.

These FFT engines are derived from Pentek's Model 4954-401 and -404 GateFlow Quad FFT IP Core Libraries, also available separately for custom applications.

Calculation Times

Using the A/D input mode with a sample clock of 100 MHz, both channels of the 6235 can easily perform FFT calculations in real time with no data loss for either size FFT, with up to 50% input overlap processing. In this case, FFT calculation times for the 1024- and 4096-point FFTs are 2.56 usec and 10.24 usec, respectively. The selectable Hanning window and output power calculation do not impact speed.

Either FFT engine requires the Xilinx XC2V3000 FPGAs (ordered as Option -300).



Ordering Information

Model	Description
6235	Model 6235 Dual Channel Wideband FFT Receiver - VIM-2

Options:

-300-401 1k FFT

-300-404 4k FFT

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