



Features

- Four 65 or 80 MHz, 14-bit A/D converters
- Front panel FPGA I/O connector
- All downconverters can select any of the four inputs
- 90 MHz input bandwidth
- 3.2 kHz to 1.6 MHz output bandwidths for $f_s = 64$ MHz
- Front panel clock and sync bus to sync multiple boards

General Information

Model 6230 is a general-purpose 32-channel narrowband digital receiver VIM-4 module. It attaches directly to VIM-compatible processor boards and connects directly to all four processors.

Front End

The Model 6230 accepts four analog RF inputs on front panel SMA connectors. Input amplifier bandwidth of 90 MHz supports direct IF undersampling. Each input is amplified and, optionally, lowpass filtered to remove out-of-band signals and prevent aliasing. The filters may be bypassed for undersampling applications.

Optionally available, transformer-coupled inputs reduce distortion for input signals above 10 MHz and are recommended for IF undersampling applications.

Each of the four inputs is then digitized by a 14-bit A/D converter which is capable of operating at sample rates up to 65 MHz (Analog Devices AD6644) or, optionally, 80 MHz (AD6645). The A/D converter clock can be driven from an internal 64 MHz or 80 MHz crystal oscillator or from an external sample clock supplied through a front panel SMA connector.

Digital Downconverters

The 6230 includes eight Graychip GC4016 quad narrowband digital downconverter chips. The maximum input sampling rate for the GC4016 is 80 MHz. Each device includes four independently tuned channels capable of center frequency tuning from DC to 32 MHz, and with output bandwidths ranging from 3.2 kHz to 1.6 MHz (for 64 MHz sample clock).

Each GC4016 accepts four 14-bit parallel inputs from the four A/D converters. Inter-

nal crossbar switches allow all 32 receiver channels on the board to select any of the four A/D inputs for flexible switching.

Synchronization

The front panel clock and sync bus allow one 6230 to act as a master, driving the sample clock out to a front panel cable bus using LVDS differential signaling. Multiple slaves can then be clocked synchronously with the master. Additional sync lines allow synchronization of the local oscillator phase, frequency switching, decimating filter phase, and FIFO data collection on multiple 6230's.

FPGAs

The 32 downconverter outputs are delivered to two Xilinx Virtex-E Series XCV300E FPGAs (Field Programmable Gate Arrays) which perform various modes of data packing, formatting and channel selection. The A/D outputs are also connected directly to the FPGAs so that wideband A/D data can be delivered directly to the processor board bypassing the downconverters. Xilinx Model XCV600E FPGAs are optionally available for more extensive applications.

Optionally available GateFlow Design Kits allow the FPGAs to be configured by the user for implementation of custom preprocessing functions such as convolution, framing, pattern recognition and decompression.

VIM Processor Interface

The FPGA outputs are connected directly through the VIM mezzanine interface to the 32-bit synchronous FIFO on the VIM processor board where they are buffered for efficient block transfers into the processor. The processor can control the programmable registers on its associated GC4016's as well as control and initiate sync bus functions.



Ordering Information

Model	Description
6230	32-Channel Narrowban Receiver with A/D and FPGA - VIM-4

Options:

-080	80 MHz A/Ds and internal oscillator
-105	Transformer-coupled inputs

-600 XCV600E FPGAs

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