New!

FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

Model 5983-324

JADEFX

Flexor

NAVIGATOR Design Suite

Features

- Supports Xilinx Kintex UltraScale FPGA
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input sample rate, 2 GHz output sample rate with interpolation)
- 4 and 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- LVDS connections to the Kintex Ultrascale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-324 FlexorSet™ combines the Model 5983 and the Model 3324 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances.

The Flexor Architecture

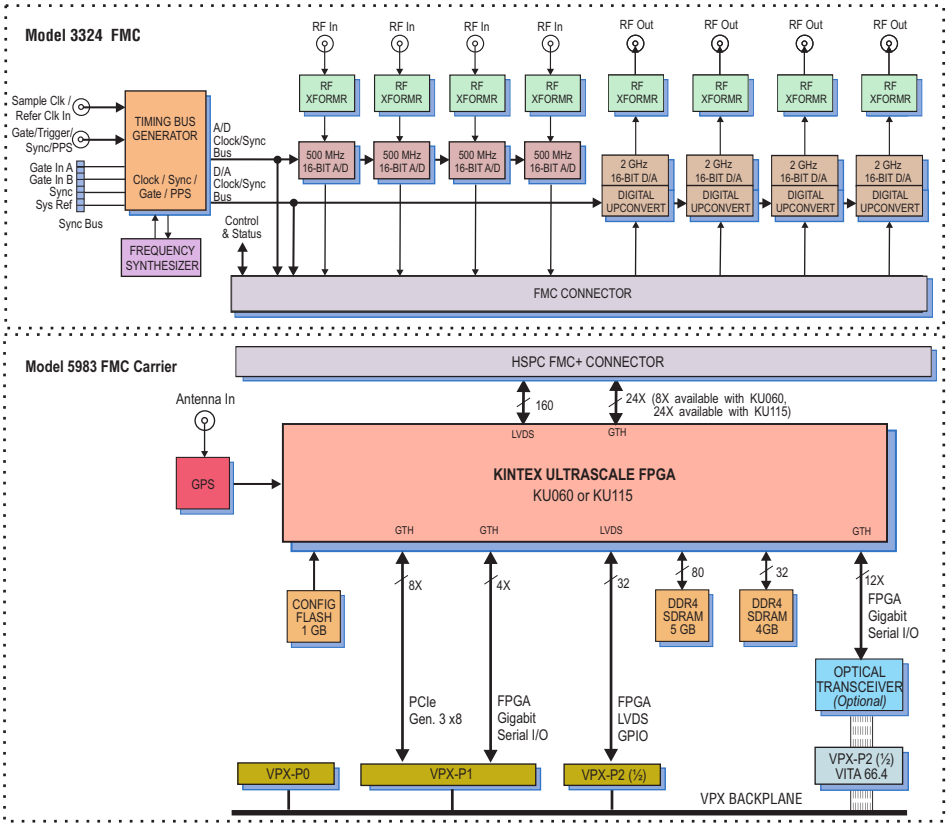
Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-324 includes factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-324 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP. ➤



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Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

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4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

A/D Acquisition IP Modules

The 5983-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Recorder IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Recorder IP Modules

The 5983-324 factory-installed functions include four sophisticated D/A Waveform Recorder IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-324 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

Memory Resources

The 5983-324 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

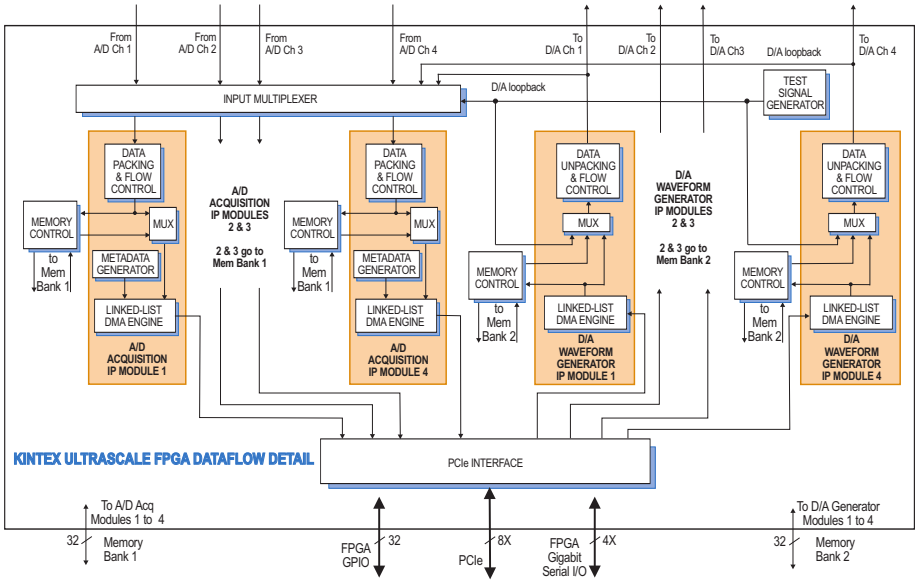
A/D Converter and Downconverter

The front end accepts four analog RF or IF inputs on front-panel connectors with transformer-coupling into Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

Digital Upconverter and D/A

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. ➤



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➤ GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel connectors

Transformer Type: Coil Craft WBC4-6TLB

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks ➤

FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

➤ **External Clock**
Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -763: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

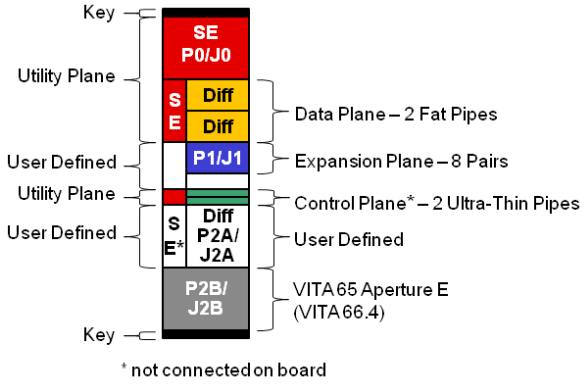
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatibile with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

Model	Description
5983-324	4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Kintex UltraScale FPGA - 3U VPX
Options:	
-087	XCKU115-2 FPGA
-110	VITA-66.4 12X optical interface
-180	GPS Support
-702	Air cooled, Level L2
-763	Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions



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