New!

Model 5950

8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX

General Information

The Model 5950 is a high-performance 3U OpenVPX board based on the Xilinx Zynq UltraScale+ RFSoC FPGA. The RFSoC integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture creating a multichannel data conversion and processing solution on a single chip. The Model 5950 brings RFSoC performance to 3U VPX with a complete system on a board.

Complementing the RFSoC's on-chip resources are the 5950's 18 GBytes of DDR4, a sophisticated clocking section for single board and multi-board synchronization, a low-noise front end for RF input and output, a PCIe interface, a gigabit serial optical interface capable of supporting dual 100GigE connections and general purpose serial and parallel signal paths to the FPGA for communication to custom IP processing.

A/D Converter Stage

The front end accepts analog IF or RF inputs on eight front panel MMCX connectors with transformer-coupling into the RF signal chain of the RFSoC. Inside the RFSoC, the analog signals are routed to eight 4GSPS, 12-bit A/D converters. Each converter has built-in digital downconverters with programmable 1x, 2x, 4x or 8x decimation and independent tuning. The A/D digital outputs are delivered into the Zynq's programmable logic and processor system for signal processing, data capture or for routing to other resources.

D/A Converter Stage

The RFSoC's eight D/A converters accept baseband real or complex data streams from the FPGA's programmable logic. Each 6.4GSPS, 14-bit D/A includes a digital upconverter with independent tuning and interpolations of 1x, 2x , 4x and 8x. Each D/A output is transformer coupled to a front panel MMCX connector.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D and D/A converters. It includes a sample clock, SysRef and gate or trigger signals. Using this internal clock requires no other clock to be supplied for operation.

In an alternate mode, the on-board sample clock can be synchronized to a 10 MHz reference clock received through a front panel connector. This mode provides a means for synchronizing multiple boards in a system through a distributed reference clock.

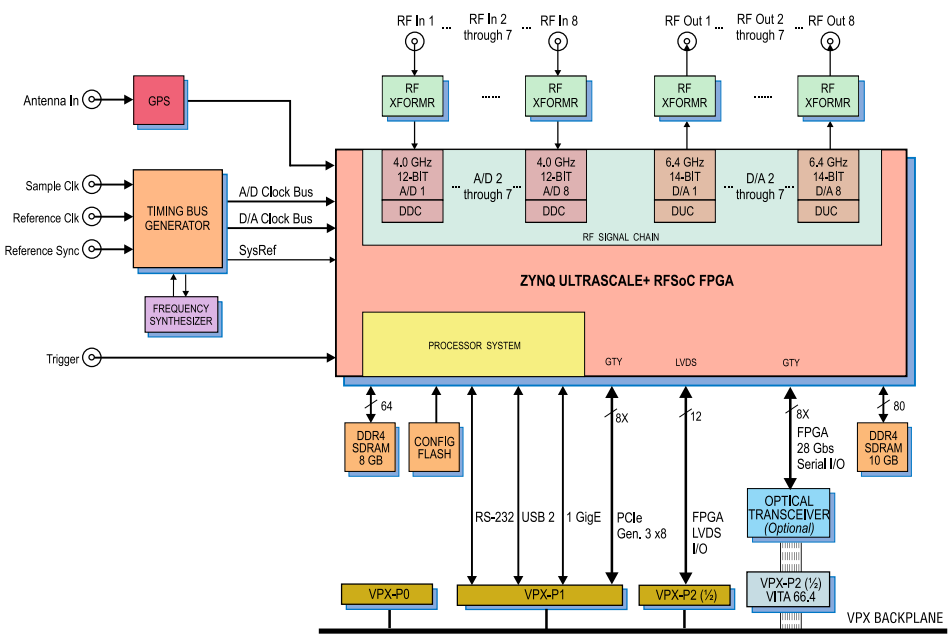
The Model 5950 also includes a front panel external clock input for applications that require the sample clock from an external source. This mode bypasses the on-board sample clock.

A front panel trigger/gate input is provided on the 5950 for external control of data acquisition and playback.

NAVIGATOR Design Suite

Features

- Supports Xilinx Zynq UltraScale+ RFSoC FPGAs
- 18 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Zynq UltraScale+ FPGA for custom I/O
- Optional optical interface for backplane gigabit serial communication
- Compatible with several VITA standards including: *VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available



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Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx, OnyxFx, JadeFX and Model 5950 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Board Architecture

As a central foundation of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

The RFSoC's on-chip data converters are supported by specialized IP including A/D acquisition and D/A waveform generation engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked- list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5950 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Expandable I/O

The Model 5950 supports the VITA-66.4 standard providing up to eight 28 Gbps duplex optical lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

Eight pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O.

Memory Resources

The 5950 architecture supports a 10 GByte bank of DDR4 SDRAM memory accessible from the programmable logic. User-installed IP along with the Pentek supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

An 8 GByte bank of DDR4 SDRAM is available to the processing system as program memory and storage.

PCI Express Interface

The Model 5950 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging. The GPS provides a 1 PPS and 10 MHz reference clock to the FPGA.

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Specifications

Field Programmable Gate Array
Xilinx Zynq UltraScale+ RFSoC XCZU27DR

RFSoC RF Signal Chain

A/D Converters:
Quantity: 8
Sampling Rate: 4.0 GHz
Resolution: 12 bits

Digital Downconverters:
Quantity: 1 per A/D
Decimation Range: 1x, 2x, 4x and 8x
LO Tuning Freq. Resolution: 48 bits, 0 to f_s
Filter: 80% pass band, 89 dB stop-band attenuation

D/A Converters:
Quantity: 8
Sampling Rate: 6.4 GHz
Resolution: 14 bits

Digital Upconverter:
Quantity: 1 per D/A
Interpolation Range: 1x, 2x, 4x and 8x
LO Tuning Freq. Resolution: 48 bits
Filter: 80% pass band, 89 dB stop-band attenuation

RFSoC RF Processing System

ARM Cortex -A53:
Quantity: 4
Speed: 1.5 GHz

ARM Cortex -R5:
Quantity: 2
Speed: 600 MHz

Custom FPGA I/O
Parallel: 8 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 8X duplex lanes @ 28 Gbps

Memory

Processing System:
Type: DDR4 SDRAM
Size: 8 GBytes
Speed: 1200 MHz (2400 MHz DDR)

Programmable Logic:
Type: DDR4 SDRAM
Size: 10 GBytes
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

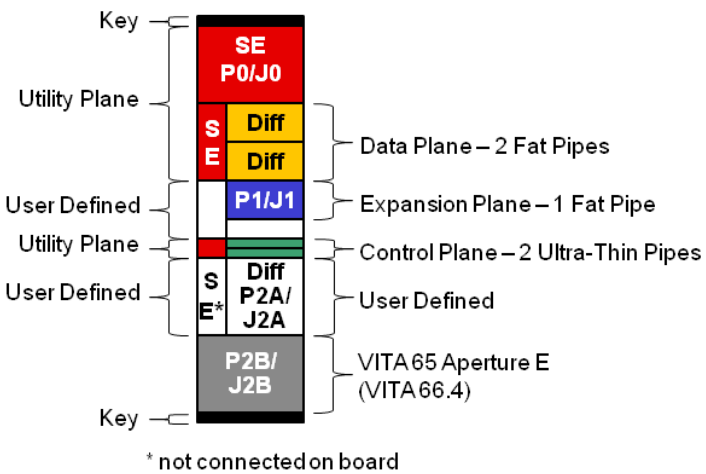
Environmental

Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
OpenVPX Compatibility: The Model 5983 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1



* not connected on board

Ordering Information

Model	Description
5950	8-Channel A/D & D/A Zynq UltraScale+ RFSoC Processor - 3U VPX
Options:	
-110	VITA-66.4 8X optical interface
-180	GPS support

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System See 8267 Datasheet for Options

Preliminary Information

Specifications subject to change

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