

New!

Models
57865 & 58865

2-/4-Ch 200 MHz 16-bit A/D Channelizer, 762/1524 Narrowband DDCs, 4/8 Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX



Model 58865



General Information

Models 57865 and 58865 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Board Support package, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71865 XMC modules mounted on a 6U VPX carrier board. Model 57865 is equipped with one 71865 while Model 58865 is equipped with two XMC modules rather than one.

They include two or four A/Ds, complete multiboard clock and sync section, eight or 16 banks of channelizer-based DDCs and resampling filters.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container

for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules for simplifying data capture and transfer.

Each acquisition IP module contains a powerful, programmable DDC IP core and a controller for all data clocking, triggering, and synchronization functions.

From each of the acquisition modules, A/D sample data flows into identical IP modules consisting of banks of wideband and narrowband DDCs. Finally, data is delivered to four or eight DMA controllers and then to the PCIe x8 interface.

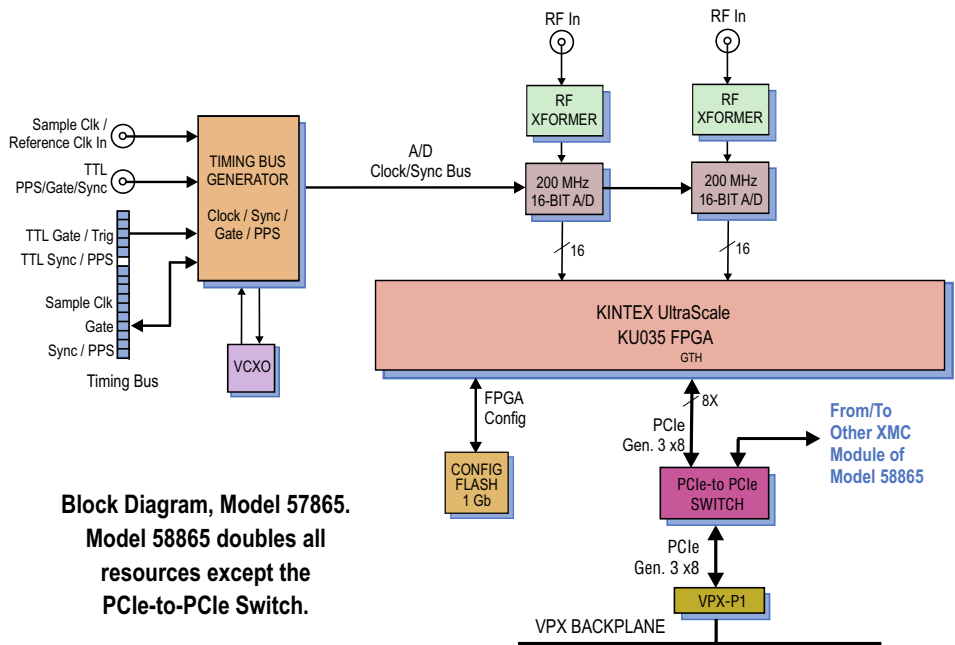
These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Xilinx Kintex UltraScale FPGA

One or two Kintex UltraScale KU035 FPGAs handle all of the control, timing, data formatting and DSP operations for the channelized DDCs and are highly optimized to maximize resource utilization and reduce power dissipation. Because of its extremely advanced FPGA design, no Navigator FDK is offered for these models so that customers cannot modify the FPGA IP. ➤

Features

- Complete software radio receiver solution for extremely high-channel-count applications
- Uses Xilinx Kintex UltraScale KU035 FPGA
- Two or four 200 MHz 16-bit A/Ds
- Four or eight wideband DDCs (digital downconverters)
- Up to 762 or 1524 narrowband DDCs
- Sample clock generation and synchronization to an external system reference
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57865.
Model 58865 doubles all resources except the PCIe-to-PCIe Switch.

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data.

Each IP module has an associated DMA engine for easily moving DDC data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC Resources

Samples from the A/D converters flow into two or four identical blocks, each containing one bank of two wideband DDCs and three or six banks of narrowband DDCs, as shown in the block diagram below.

Wideband DDCs

The wideband DDCs can be set for decimation values between 8 and 128 in steps of 4, providing usable output bandwidths from 1.25 MHz to 20 MHz for a sample rate, f_s , of 200 MHz. Because all wideband DDCs within these models feed the same DMA controller #A or C, all wideband DDCs must use the same decimation factor.

Each DDC delivers an output stream consisting of 16-bit I + 16-bit Q complex samples at a rate of f_s/N . Four samples, one from each of the wideband DDCs, are interleaved in the output stream.

All wideband DDCs can be independently tuned across the range from 0 Hz to f_s with 32 bits of resolution.

Narrowband DDCs

Each of the narrowband DDC banks can be configured to operate in three different modes, where each mode provides a different quantity of DDC channels and range of decimations.

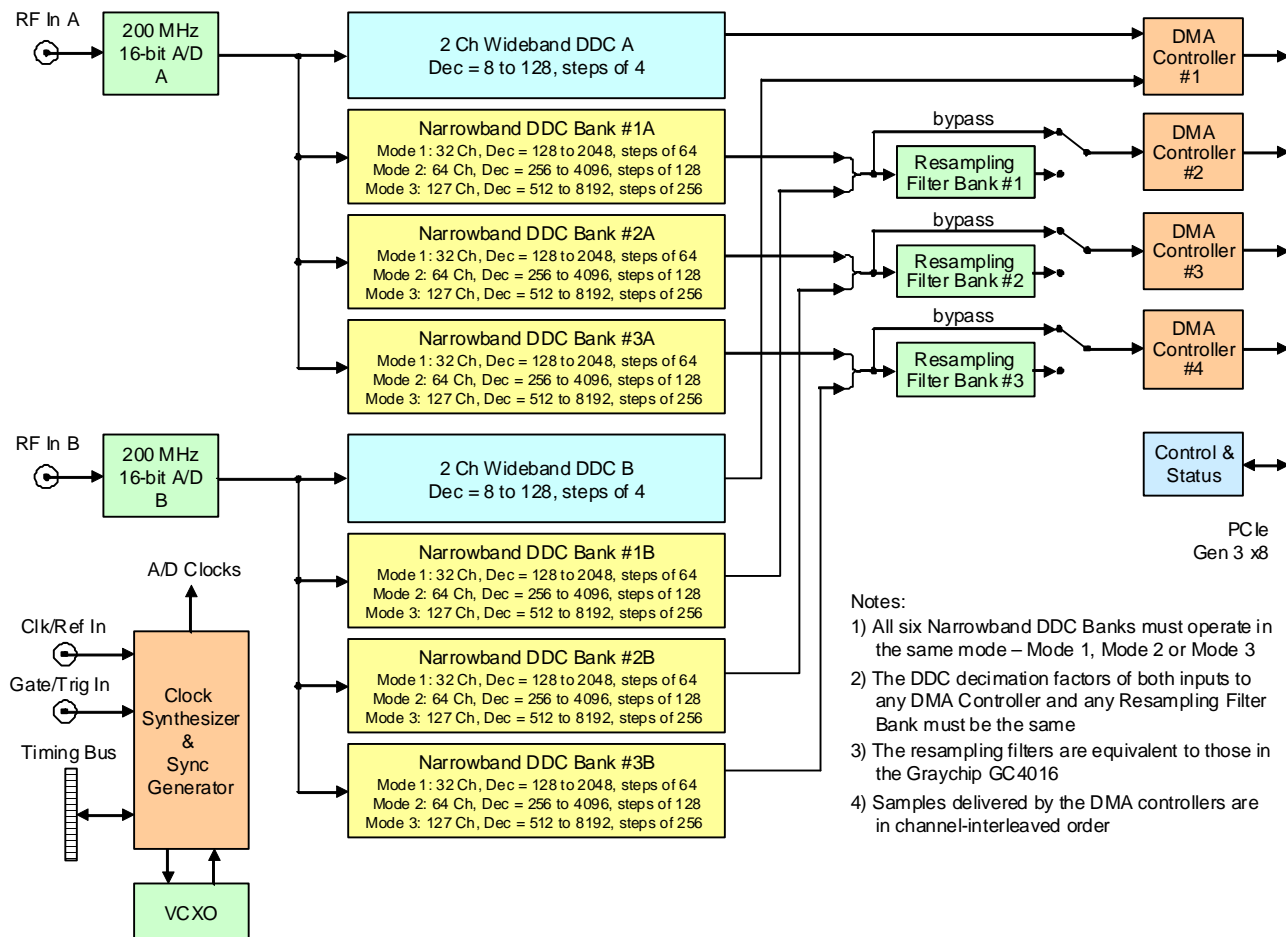
These modes are summarized in the following table:

Mode	Channels	Dec Range	Steps
1	32	128 - 2048	64
2	64	256 - 4096	128
3	127	512 - 8192	256

All narrowband DDC banks must operate in the same mode.

The 80% default filters deliver an output bandwidth of $0.8 * f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers an output stream at a rate of f_s/N , and programmable for either 16-bit I + 16-bit Q, or 24-bit I + 24-bit Q complex samples. ➤



- Notes:
- 1) All six Narrowband DDC Banks must operate in the same mode – Mode 1, Mode 2 or Mode 3
 - 2) The DDC decimation factors of both inputs to any DMA Controller and any Resampling Filter Bank must be the same
 - 3) The resampling filters are equivalent to those in the Graychip GC4016
 - 4) Samples delivered by the DMA controllers are in channel-interleaved order

Narrowband DDCs (cont.)

Because each pair of narrowband DDC banks feed a common DMA controller, the decimation setting for each DDC must be the same. Nevertheless, each pair can have a different decimation setting from the other pairs.

Resampling Filters

Three or six multiplexers allow outputs from each of the three or six narrowband DDC pairs to feed the associated DMA controller or feed the input of a resampling filter.

Each of the resampling filters is an FIR low pass filter that accepts DDC input samples at one sample rate and delivers output samples at another rate. Resampling filters are often used for better symbol recovery of signals using digital modulation schemes. The output rate is usually higher to create oversampling at a multiple of 2x, 4x, 8x, or 16x the symbol rate.

The resampling filter combines the operations of an FIR interpolation filter followed by a decimator. The overall resampling ratio is equal to the interpolation factor divided by the decimation factor, both of which are programmable parameters.

Note that each of the resampling filters can be programmed independently. Some limitations on the DDC output data rates and subsequent resampling ratios may be imposed because of maximum VPX transfer rates.

A/D Converters

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front-panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

Navigator BSP

Pentek's Navigator BSP provides a full suite of high-level C-callable libraries that support all features of these models and demonstrate all of its functional modes with examples. The software package is provided with complete source code allowing the user to modify and integrate this functionality into the end application.

Navigator BSP also includes an extremely useful Signal Viewer utility that allows developers to view digitized signals from the output samples of any DDC in time and frequency domain.

Navigator BSP is available in versions for either Windows or Linux operating systems. ►



The SPARK Development Systems are fully-integrated platforms for Pentek board-level products. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed. The system is equipped with sufficient power and cooling to ensure optimum performance.

Specifications

Model 57865: 2 A/Ds

Model 58865: 4 A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters (2 or 4)

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Wideband Digital Downconverters (4 or 8)

Decimation Range: 8 to 128 in steps of 4, common to all DDCs

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output

FIR Filter Performance: 80% band-width <0.3 dB passband ripple, >100 dB stopband attenuation

Narrowband Digital Downconverters

Quantity: Six or 12 banks

DDC Bank Modes:

Mode 1: 32 DDCs, Dec = 128 to 2048, in steps of 64

Mode 2: 64 DDCs, Dec = 256 to 4096, steps of 128

Mode 3: 127 DDCs, Dec = 512 to 8192, steps of 256

LO Tuning Freq. Resolution: 32 bits, 0 to f_s , with independent tuning for each channel

LO SFDR: >120 dB

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)

On-board clock synthesizer

Clock Synthesizer: (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock: (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)

26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input: (1 or 2)

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array: (1 or 2)

Standard: Xilinx Kintex UltraScale XCKU035-2

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Size: Board 9.187 in x 6.717 in (233.35 mm x 170.60 mm) ▶

Ordering Information

Model	Description
57865	2-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX
58865	4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

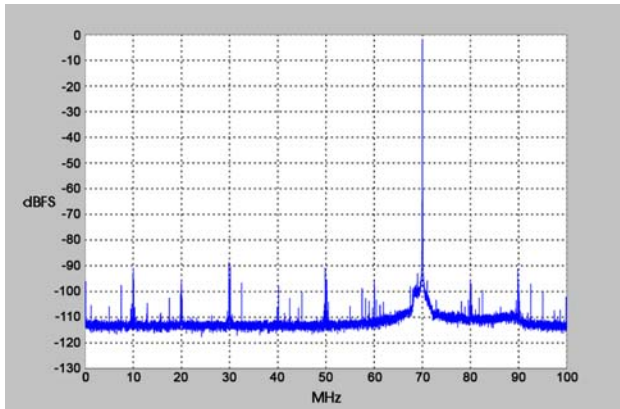
Options:

-702	Air cooled, Level L2
-713	Conduction cooled Level LR

Contact Pentek for complete specifications of rugged version

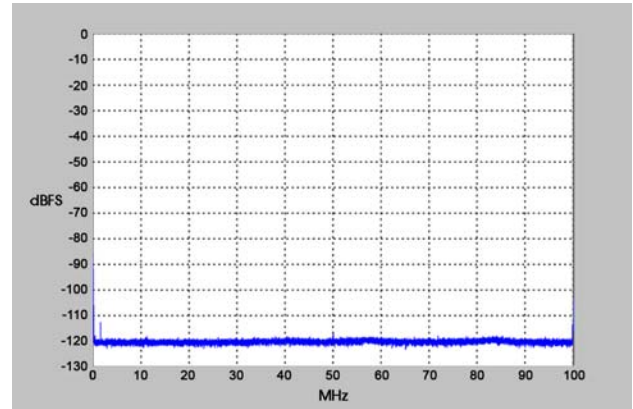
A/D Performance

Spurious Free Dynamic Range



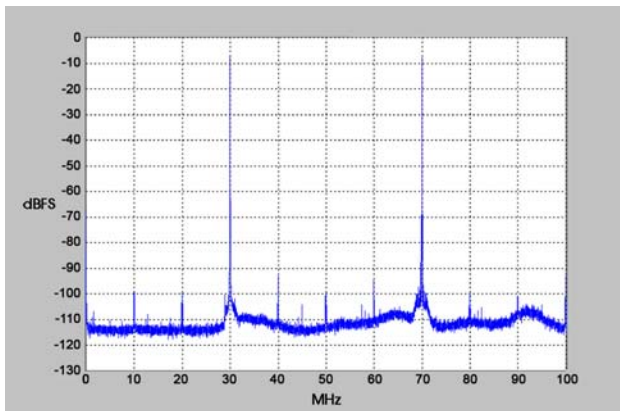
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

Spurious Pick-up



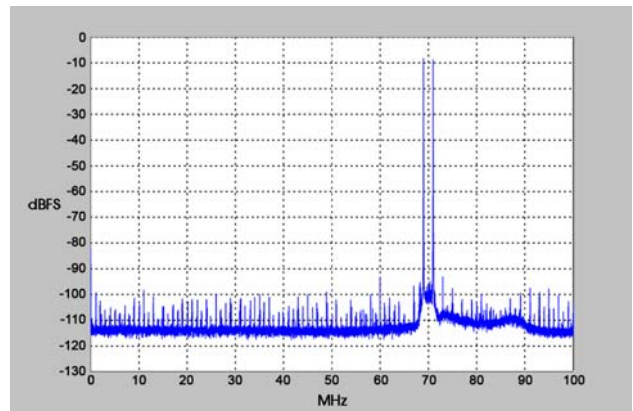
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

Two-Tone SFDR



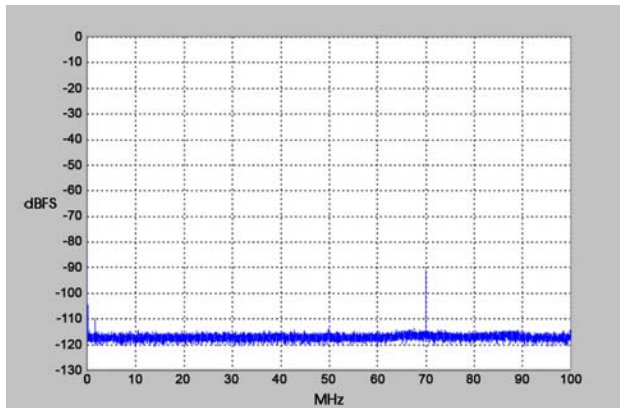
$f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

Two-Tone SFDR



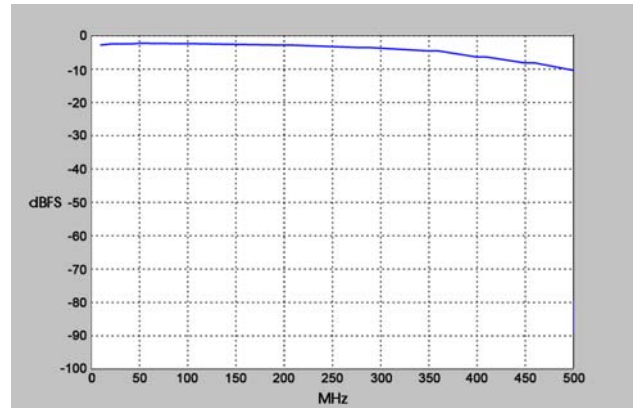
$f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

Adjacent Channel Crosstalk



$f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

Input Frequency Response



$f_s = 200 \text{ MHz}, \text{Internal Clock}$