New!

Models 57800 & 58800

Kintex UltraScale FPGA Coprocessor- 6U VPX

Model 58800

JADE NAVIGATOR Design Suite

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex Ultra-Scale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information

Models 57800 and 58800 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a VPX carrier board. Model 57800 is a 6U board with one Model 71800 module while the Model 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57800 and Model 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

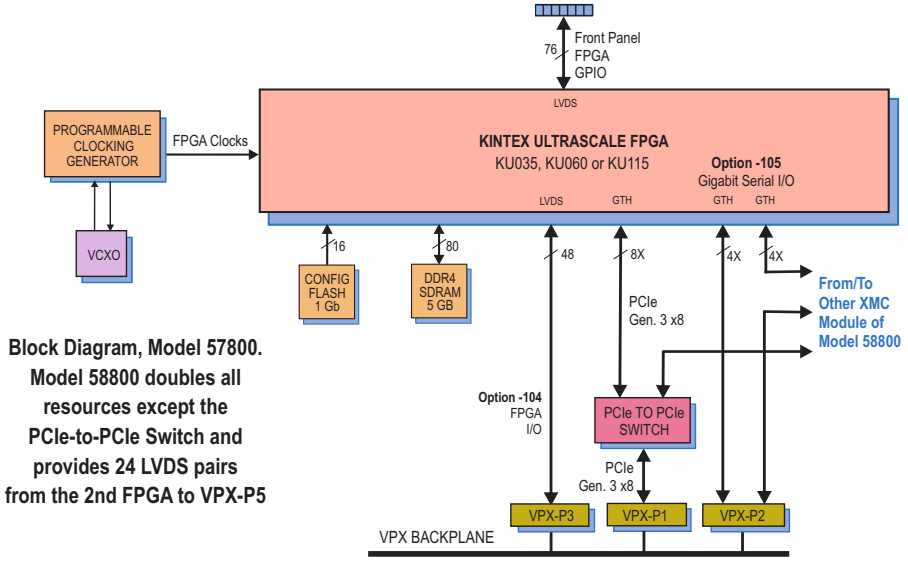
Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols. ➤



Block Diagram, Model 57800. Model 58800 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

PENTEK

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Kintex UltraScale FPGA Coprocessor- 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model	Description
57800	Kintex UltraScale FPGA Coprocessor - 6U VPX
58800	Double Kintex UltraScale FPGA Coprocessors - 6U VPX
Options:	
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O
-105	Gigabit serial FPGA I/O
-702	Air cooled, Level L2
-713	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

➤ Front-Panel Digital I/O Interface

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Specifications

Front Panel Digital I/O (1 or 2)
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 or 76 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800
- **Option -105** provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2)
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

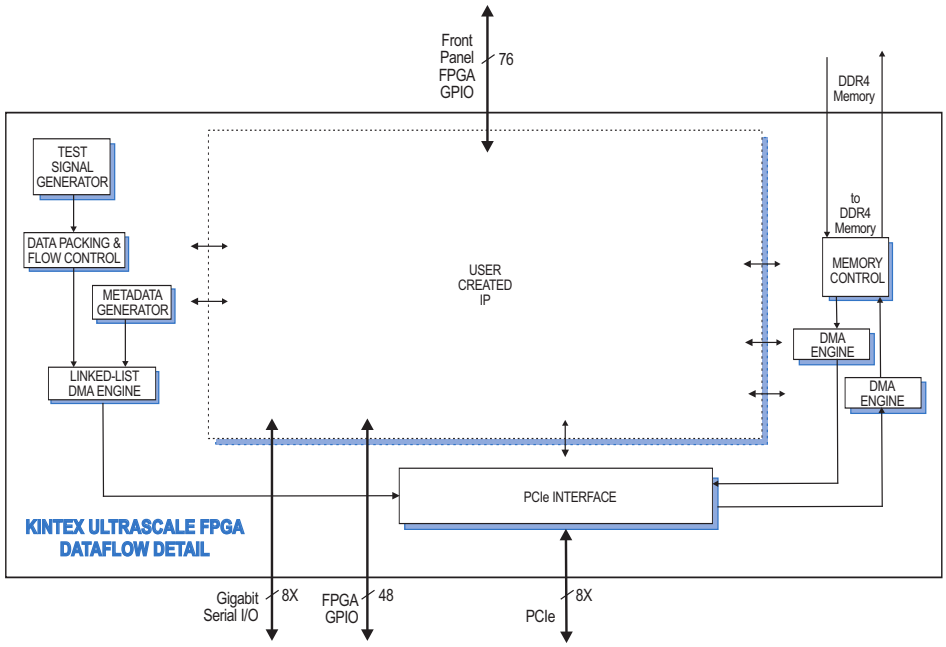
Option -702: L2 (air cooled)
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Kintex UltraScale FPGA Resources

	XCKU035	XCKU060	XCKU115
System Logic Cells	444,000	726,000	1,451,000
DSP Slices	1,700	2,760	5,520
Block RAM (Mb)	19.0	38.0	75.9



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