

New!

# Models 57720 & 58720

# 3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U Open VPX



Model 58720



### Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz 16-bit D/As
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

### General Information

Models 57720 and 58720 are members of the Onyx<sup>®</sup> family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71720 XMC modules mounted on a VPX carrier board.

Model 57720 is a 6U board with one Model 71720 module while the Model 58720 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

### The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchro-

nization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

### Extendable IP Design

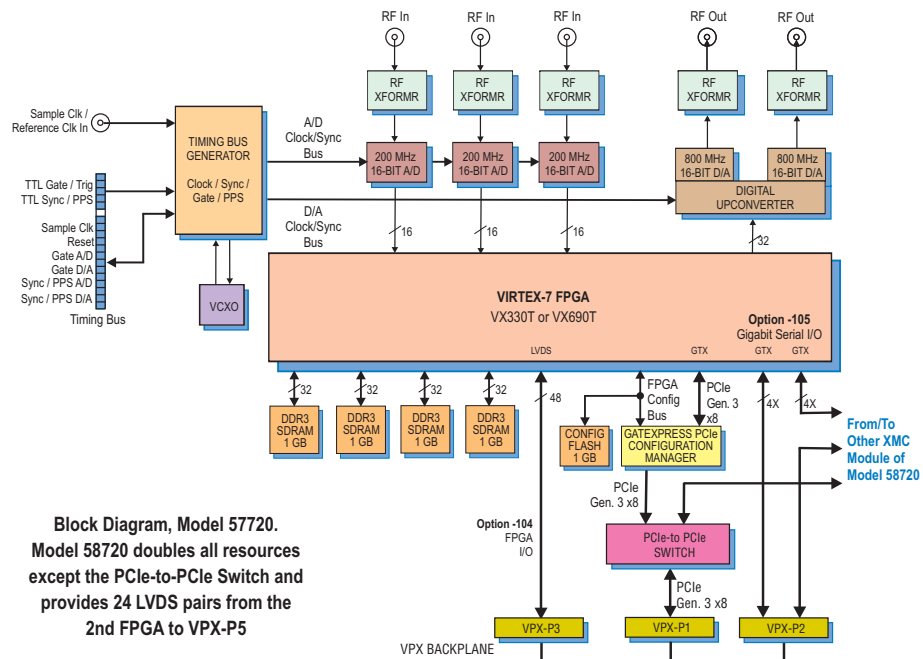
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720. ➤



**A/D Acquisition IP Modules**

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**D/A Waveform Playback IP Modules**

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**► GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of

a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

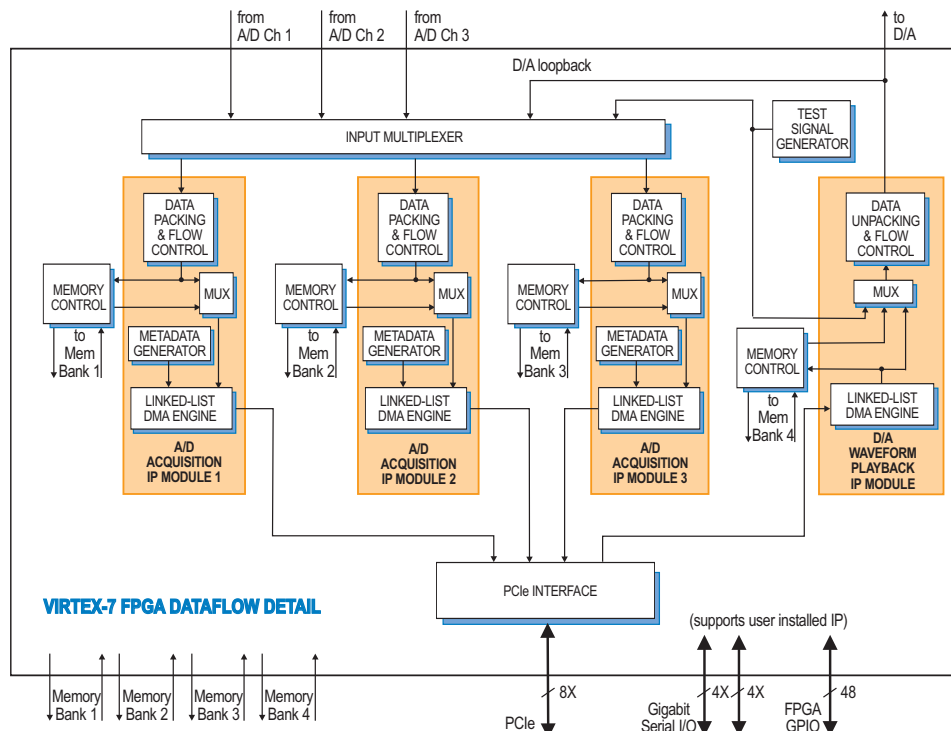
**A/D Converter Stages**

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**Digital Upconverter and D/A Stages**

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages. ►



### Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

### PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Ordering Information

Model	Description
57720	3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex7 FPGA - 6U VPX
58720	6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A with two Virtex-7 FPGAs - 6U VPX
<b>Options:</b>	
-076	XC7VX690T-2 FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57720; P3 and P5 connectors, Model 58720
-105	Gigabit link between the FPGA and P2 connector, Model 57720; gigabit links from each FPGA to P2 connector, Model 78720

*Contact Pentek for availability of rugged and conduction-cooled versions*

► When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

### Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

### Specifications

**Model 57620: 3 A/Ds, 1 DUC, 2 D/As**

**Model 58620: 6 A/Ds, 2 DUCs, 4 D/As**

#### Front Panel Analog Signal Inputs (3 or 6)

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full Scale Input:** +8 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

#### A/D Converters (3 or 6)

**Type:** Texas Instruments ADS5485

**Sampling Rate:** 10 MHz to 200 MHz

**Resolution:** 16 bits

#### D/A Converters (2 or 4)

**Type:** Texas Instruments DAC5688

**Input Data Rate:** 250 MHz max.

**Output IF:** DC to 400 MHz max.

**Output Signal:** 2-channel real or 1-channel with frequency translation

**Output Sampling Rate:** 800 MHz max. with interpolation

**Resolution:** 16 bits

#### Front Panel Analog Signal Outputs (2 or 4)

**Output Type:** Transformer-coupled, front panel female SSMC connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full Scale Output:** +4 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

#### Sample Clock Sources (2 or 4)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

#### Clock Synthesizers (1 or 2)

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

#### External Clocks (1 or 2)

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

**Timing Bus (1 or 2):** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### Field Programmable Gate Array

**Standard:** Xilinx Virtex-7 XC7VX330T-2

**Optional:** Xilinx Virtex-7 XC7VX690T-2

#### Custom I/O

**Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720

**Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720.

#### Memory Banks (4 or 8)

**Type:** DDR3 SDRAM

**Size:** 1 GB each

**Speed:** 800 MHz (1600 MHz DDR)

#### PCI-Express Interface

**PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

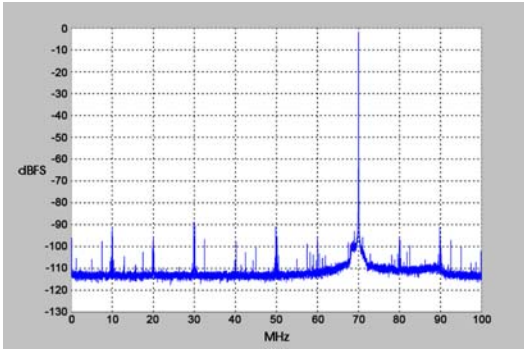
**Environmental:** Level L1 & L2 air-cooled;

Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

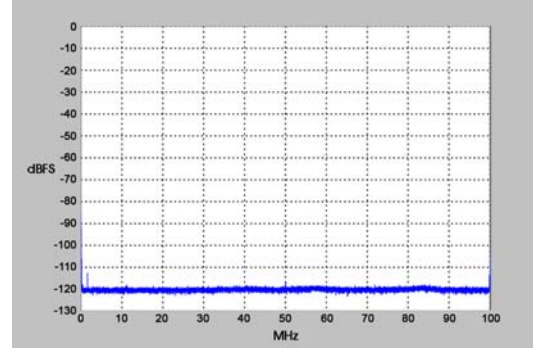
**A/D Performance**

**Spurious Free Dynamic Range**



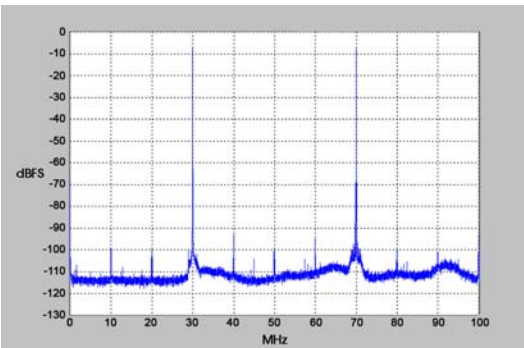
$f_{in} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

**Spurious Pick-up**



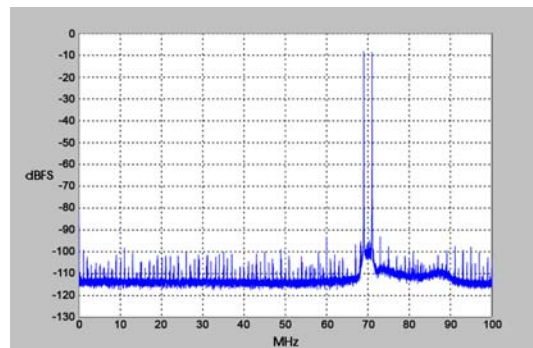
$f_s = 200 \text{ MHz}, \text{Internal Clock}$

**Two-Tone SFDR**



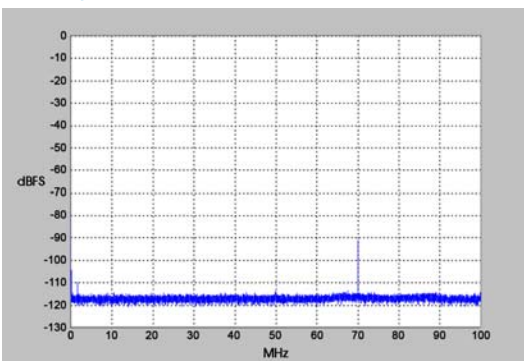
$f_1 = 30 \text{ MHz}, f_2 = 70 \text{ MHz}, f_s = 200 \text{ MHz}$

**Two-Tone SFDR**



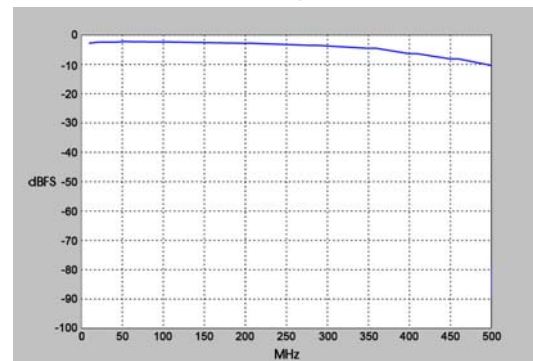
$f_1 = 69 \text{ MHz}, f_2 = 71 \text{ MHz}, f_s = 200 \text{ MHz}$

**Adjacent Channel Crosstalk**



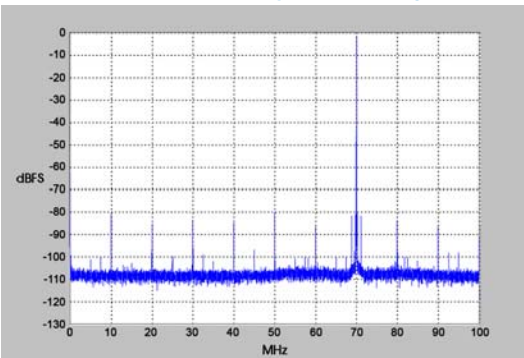
$f_{in \text{ Ch2}} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Ch 1 shown}$

**Input Frequency Response**



$f_s = 200 \text{ MHz}, \text{Internal Clock}$

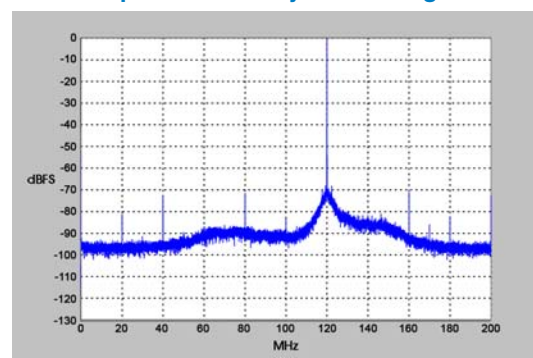
**Spurious Free Dynamic Range**



$f_{out} = 70 \text{ MHz}, f_s = 200 \text{ MHz}, \text{Internal Clock}$

**D/A Performance**

**Spurious Free Dynamic Range**



$f_{out} = 140 \text{ MHz}, f_s = 400 \text{ MHz}, \text{External Clock}$