New!

Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

Model 58662

General Information

Models 57662 and 58662 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a VPX carrier board.

Model 57662 is a 6U board with one Model 71662 module while the Model 58662 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, 32 or 64 multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, test signal generators, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

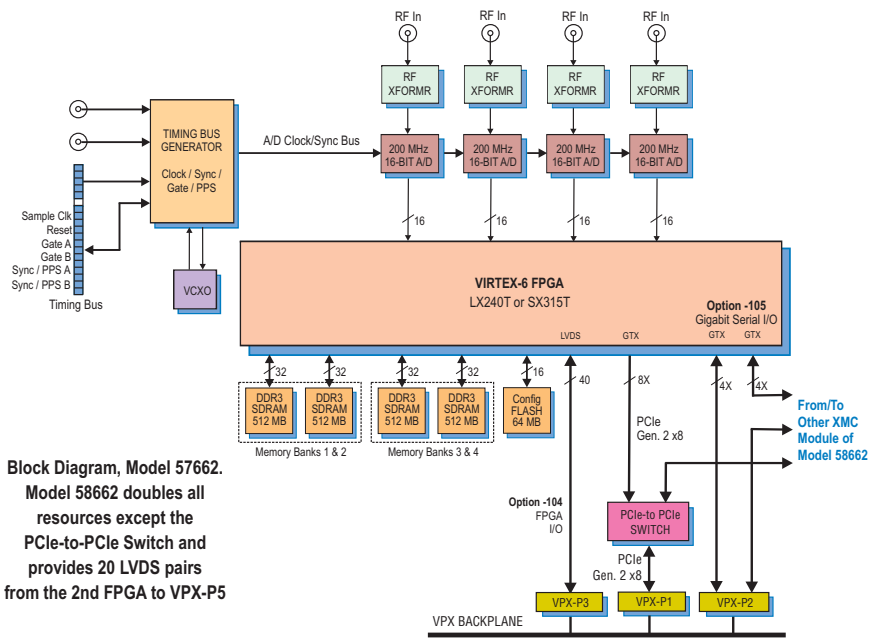
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662. ➤

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- 32 or 64 channels of multiband DDCs (digital downconverters)
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



Block Diagram, Model 57662. Model 58662 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5

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Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

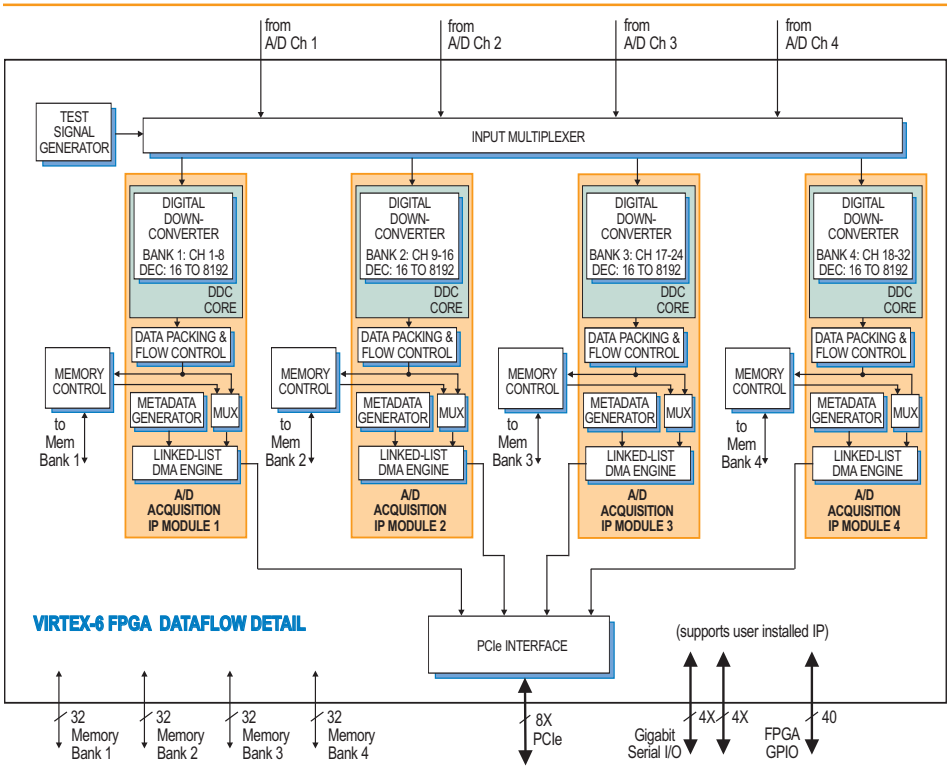
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with DDR3 SDRAM. ➤



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Models 57662 & 58662

4- or 8-Channel 200 MHz A/D with 32- or 64-Channel DDC and Virtex-6 FPGA - 6U OpenVPX

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57662: 4 A/Ds, 32 DDCs
Model 58660: 8 A/Ds, 64 DDCs

Front Panel Analog Signal Inputs (4 or 8)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (4 or 8)
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters (32 or 64)
- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
- On-board clock synthesizer

Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus (1 or 2): 26-pin connector
- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662

MemoryBanks (1 or 2)
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
57662	4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 6U VPX
58662	8-Ch 200 MHz A/D with 64-Ch DDC and two Virtex-6 FPGAs - 6U VPX
Options:	
-064	XC6VSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57662; P3 and P5 connectors, Model 58662
-105	Gigabit link between the FPGA and P2 connector, Model 57662; gigabit links from each FPGA to P2 connector, Model 58660
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

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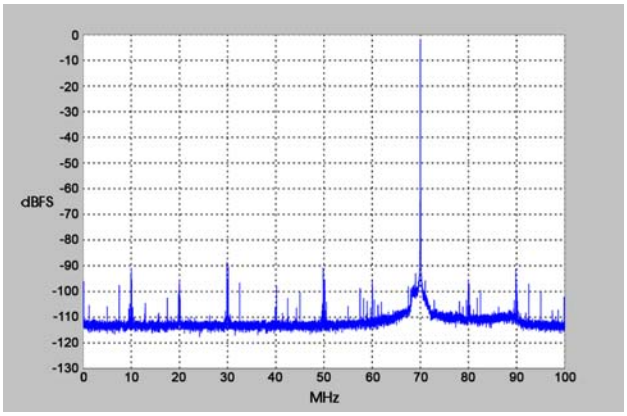
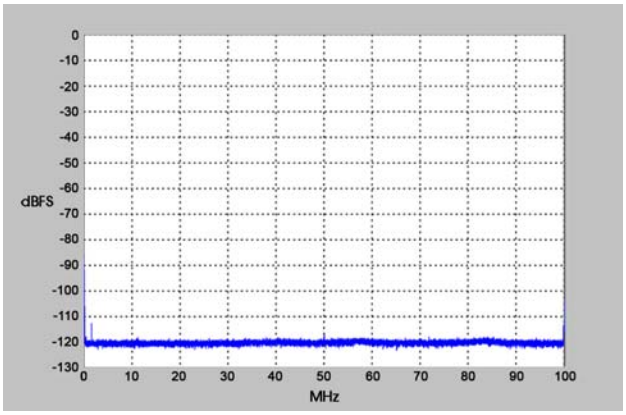
A/D Performance

Spurious Free Dynamic Range



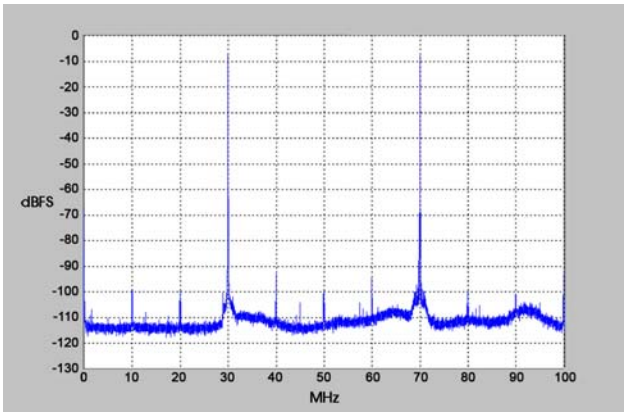
f_{in} = 70 MHz, f_s = 200 MHz, Internal Clock

Spurious Pick-up



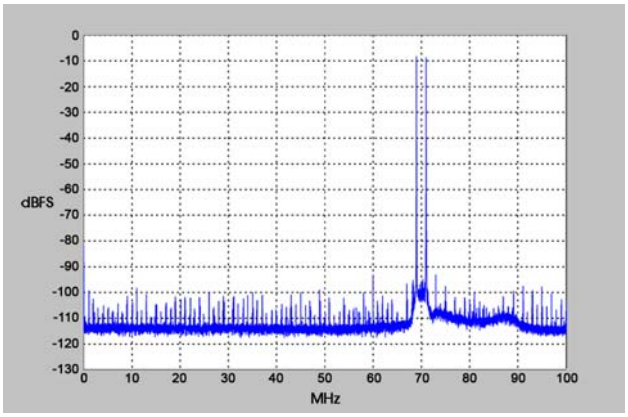
f_s = 200 MHz, Internal Clock

Two-Tone SFDR



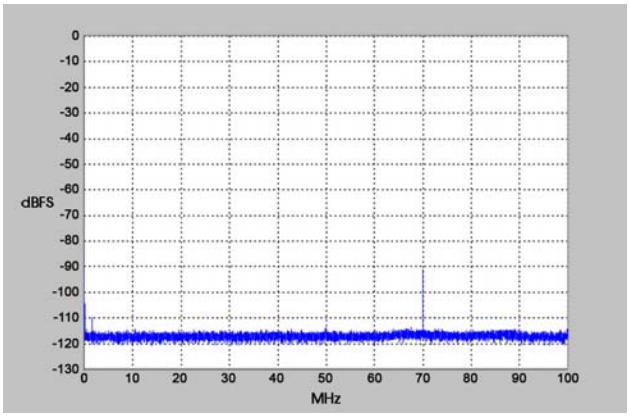
f_1 = 30 MHz, f_2 = 70 MHz, f_s = 200 MHz

Two-Tone SFDR



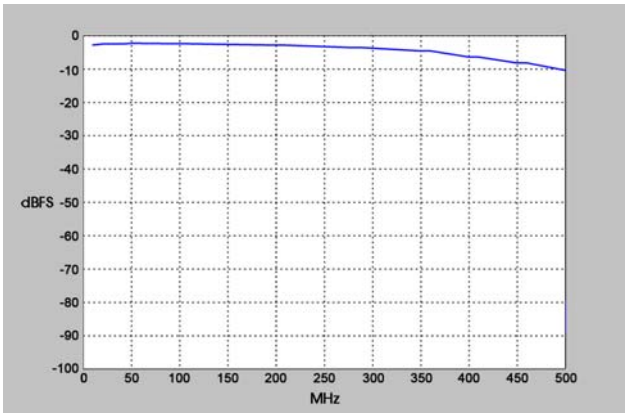
f_1 = 69 MHz, f_2 = 71 MHz, f_s = 200 MHz

Adjacent Channel Crosstalk Crosstalk



$f_{in\ Ch2}$ = 70 MHz, f_s = 200 MHz, Ch 1 shown

Input Frequency Response



f_s = 200 MHz, Internal Clock