

New!

# Models 57630 & 58630

# 1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX



Model 58630



## General Information

Models 57630 and 58630 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a VPX carrier board.

Model 57630 is a 6U board with one Model 71630 module while the Model 58630 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

## The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions

and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

## Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

## Xilinx Virtex-6 FPGA

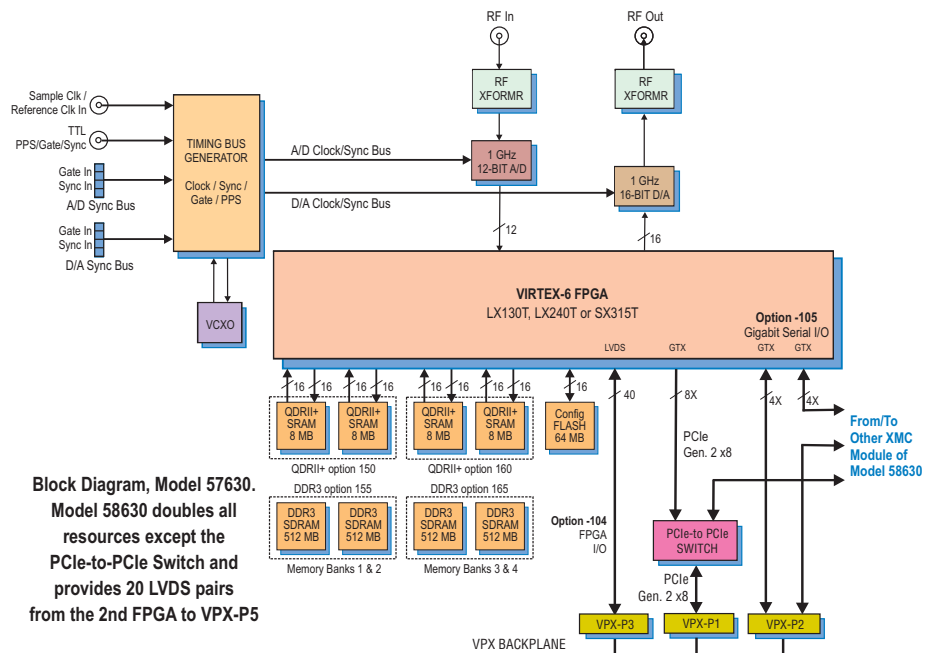
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630. ➤

## Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available



**A/D Acquisition IP Module**

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**D/A Waveform Playback IP Modules**

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**A/D Converter Stage**

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

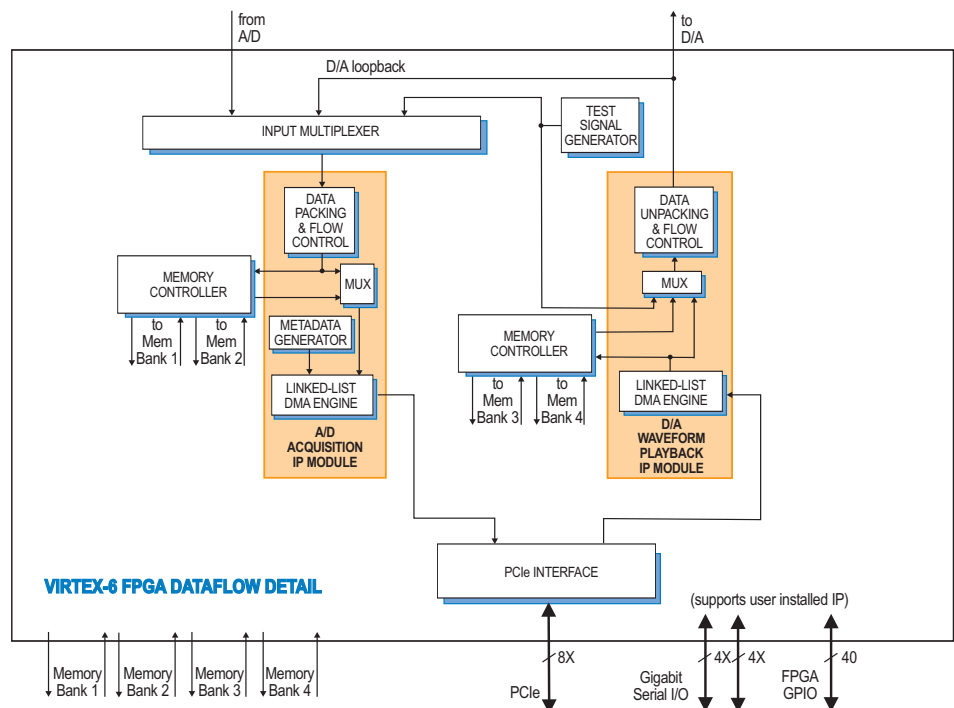
A pair of front panel μSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and gate/trigger signals.

The Pentek Model 9192 Cobalt Synchronizer can drive multiple μSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTTL external gate/trigger input is accepted on a front panel SSMC connector.

**Memory Resources**

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. ➤



► **PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Model 57630: 1 A/D, 1 D/A**

**Model 58630: 2 A/Ds, 2 D/As**

**Front Panel Analog Signal Inputs (1 or 2)**

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converters (1 or 2)**

**Type:** Texas Instruments ADS5400

**Sampling Rate:** 100 MHz to 1 GHz

**Resolution:** 12 bits

**D/A Converters (1 or 2)**

**Type:** Texas Instruments DAC5681Z

**Input Data Rate:** 1 GHz max.

**Interpolation Filter:** bypass, 2x or 4x

**Output Sampling Rate:** 1 GHz max.

**Resolution:** 16 bits

**Front Panel Analog Signal Outputs (1 or 2)**

**Output Type:** Transformer-coupled, front panel female SSMC connectors

**Sample Clock Sources (1 or 2)**

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizers (1 or 2)**

**Clock Source:** Selectable from on-board programmable VCXO or front panel external clock

**VCXO Frequency Ranges:** 10 to 945

MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

**Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clocks (1 or 2)**

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

**Timing Bus (1 or 2):** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input (1 or 2)**

**Type:** Front panel female SSMC connector, LVTTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

**Standard:** Xilinx Virtex-6 XC6VLX130T-2

**Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VVSX315T-2

**Custom I/O**

**Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630

**Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630

**Memory Banks (1 or 2)**

**Option 150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR

**Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

**PCI Express Bus:** Gen. 1 or 2: x4 or x8

**Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**Ordering Information**

Model	Description
57630	1 GHz A/D and D/A with Virtex-6 FPGA - 6U VPX
58630	Two 1 GHz A/D and D/A, with two Virtex-6 FPGAs - 6U VPX
<b>Options:</b>	
-002*	-2 FPGA speed grade
-062	XC6VLX240T FPGA
-064	XC6VVSX315T FPGA
-104	LVDS I/O between the FPGA and P3 connector, Model 57630; P3 and P5 connectors, Model 58630
-105	Gigabit link between the FPGA and P2 connector, Model 57630; gigabit links from each FPGA to P2 connector, Model 78630
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

\* This option is always required

*Contact Pentek for availability of rugged and conduction-cooled versions*