Model 56611

Quad Serial FPDP Interface with Virtex-6 FPGA - AMC

General Information

Model 56611 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 56611 serves as a flexible platform for developing and deploying custom FPGA processing IP. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56611 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 56611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

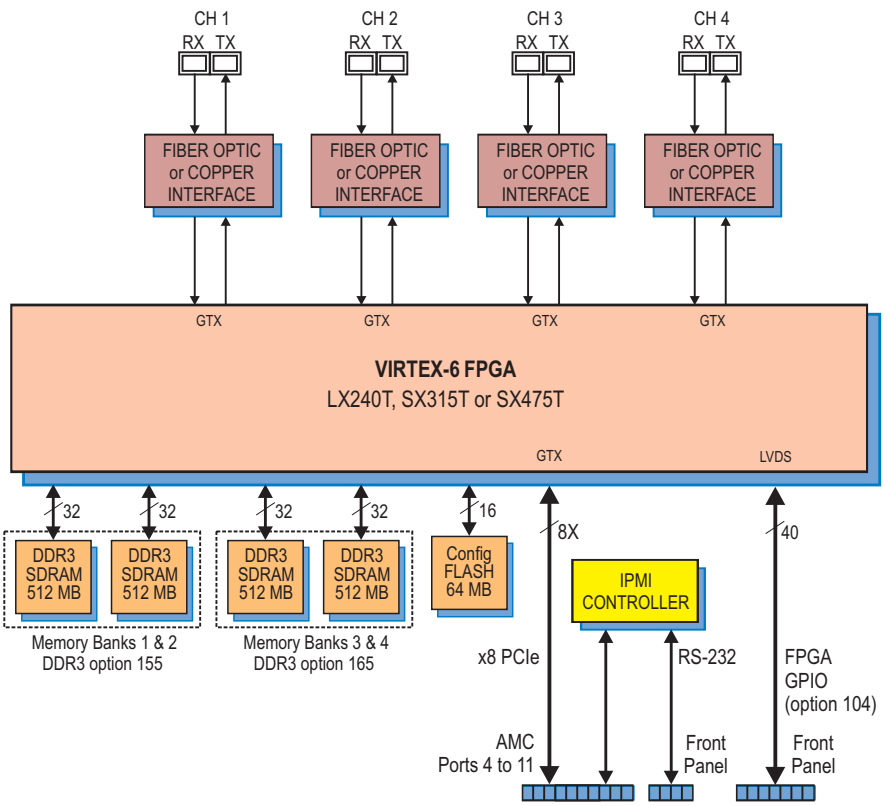
Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O. ➤

Features

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O



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AMC Interface

The Model 56611 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

➤ Serial FPDP Interface

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 56611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the module.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- **Number of Connectors:** 4
- **Fiber Optic Connector Type:** LC
  - **Laser:** 850 nm (standard, other options available)
- **Copper Connector Type:** Micro Twinax
- **Fiber Optic or Copper Link Rates:** 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable langth)
- **Fiber Optic or Copper Data Transfer Rates:** 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

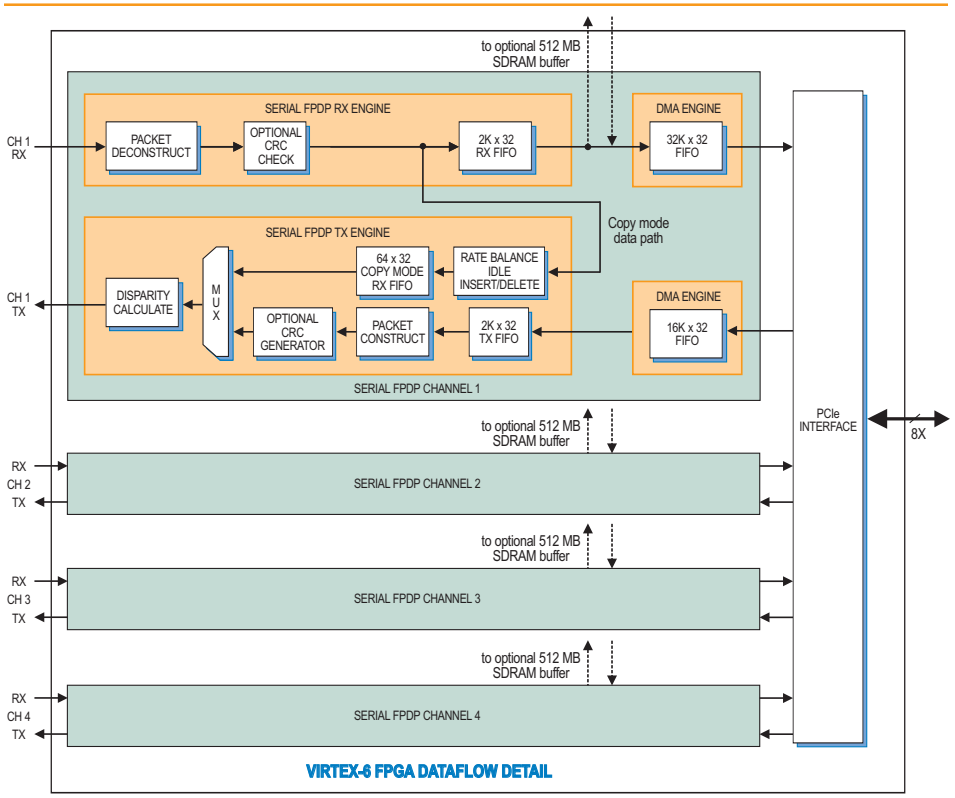
Memory
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in. ➤



Ordering Information

Model	Description
56611	Quad Serial FPDP Interface with Virtex-6 FPGA - AMC
Options:	
-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-065	XC6VSX475T FPGA
-104	LVDS FPGA I/O through front panel connector
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280	Copper serial interfaces
-281	Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

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➤ Serial FPDP VITA 17.1 Compliance

The 56611 fully complies with the VITA 17.1 specification as follows:

What Link Rate does the interface support?
■ 1.0625 Gbaud ■ 2.125 Gbaud ■ 2.5 Gbaud ■ 3.125 Gbaud ■ 4.25 Gbaud

What Serial FPDP function does the interface support?
__ Transmitter only __ Receiver only ■ Transmitter & Receiver

Does the Receiver support Flow Control (setting the STOP signal)?
__ Always active __Not supported ■ Optional (selectable)

Does the Transmitter support Flow Control (stopping data transmission on receipt of a STOP signal)?
__ Always active __ Not supported ■ Optional (selectable)

If the Transmitter supports Flow Control, after transmitting a STOP signal, how many 32-bit words can be received before a Receive FIFO overflow occurs?
■ Programmable

Does the interface support CRC?
__ Always active __ Not supported ■ Optional (selectable)

Does the Transmitter support Copy Master Mode (insertion of additional IDLE ordered sets)?
__ Always active __ Not supported ■ Optional (selectable)

Does the Receiver support Copy Mode (retransmission of data)?
■ Yes __ No

If Copy Mode is supported, what method is used for implementation (see VITA 17.1 Observation 6.1.4.4)?
__ Method 1 ■ Method 2

Does the Receiver support Copy/Loop Mode (retransmission of data and setting Flow Control)?
■ Yes __ No

What type of media is supported?
■ Short Wave Laser ■ Long Wave Laser ■ Copper

What type of media connectors are supported?
■ LC __ SC __ ST ■ Micro Twinax

Which fiber transmit data frames are supported in addition to Normal Data Fiber Frames (see VITA 17.1 Permission 7.3.3.1)?
■ Sync without Data Fiber Frames ■ Sync with Data Fiber Frames

Does the Serial FPDP Transmitter stop in response to the Serial FPDP Receiver sending NRDY True (see VITA 17.1 Observation 7.3.2.2)?
__ Always __ Never ■ Optional (selectable)

Are status bits kept up to date when there is no data to transmit by sending empty Serial FPDP Normal Data Fiber (see VITA 17.1 Rule 7.3.3.8, Recommendation 7.3.3.2 and Suggestion 7.3.3.1)?
■ Yes, empty frames transmitted __ No, status is not updated when no data is transmitted