

New!

# Model 53851

## 2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX



Model 53851 Commercial (left) and rugged version



### Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Supports VITA-49.2 VITA Radio Transport standard
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

### General Information

Model 53851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

### The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing,

channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

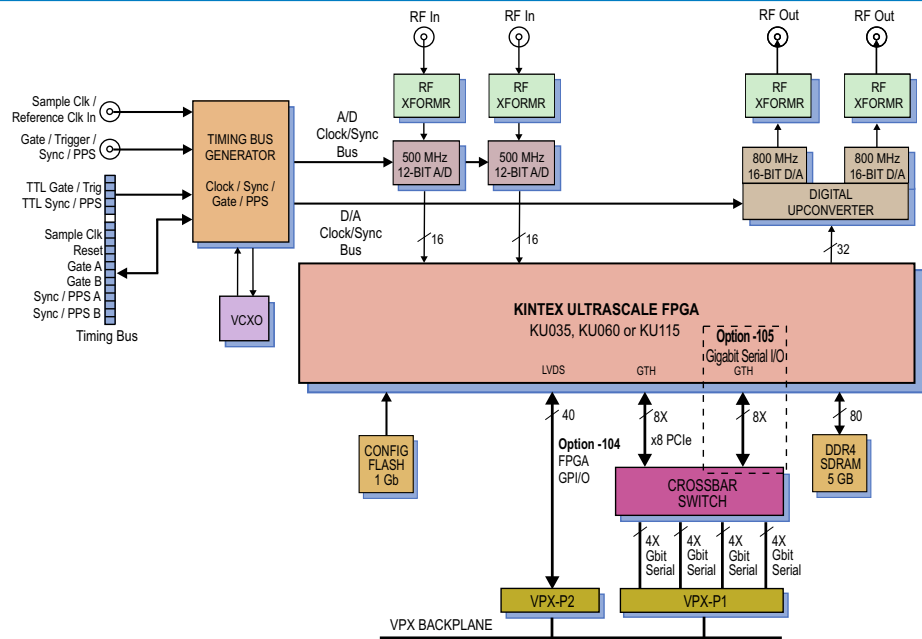
The 53851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤



**A/D Acquisition IP Modules**

The 53851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to  $f_s$ , where  $f_s$  is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output band-

widths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of  $0.8 \cdot f_s / N$ , where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of  $f_s / N$ .

**D/A Waveform Playback IP Module**

The Model 53851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

**► A/D Converter Stage**

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463. ►

**VITA 49.2 Radio Transport Standard**

VITA 49.2 is a data transport protocol for conveying digitized signal information among signal acquisition/generation and processing elements in a communication, radar or similar system.

The Model 53851 implements the VITA 49 packet format for the ADC/DDC data being transferred to the host memory via DMA.

VITA 49.2 packet elements always supported are:

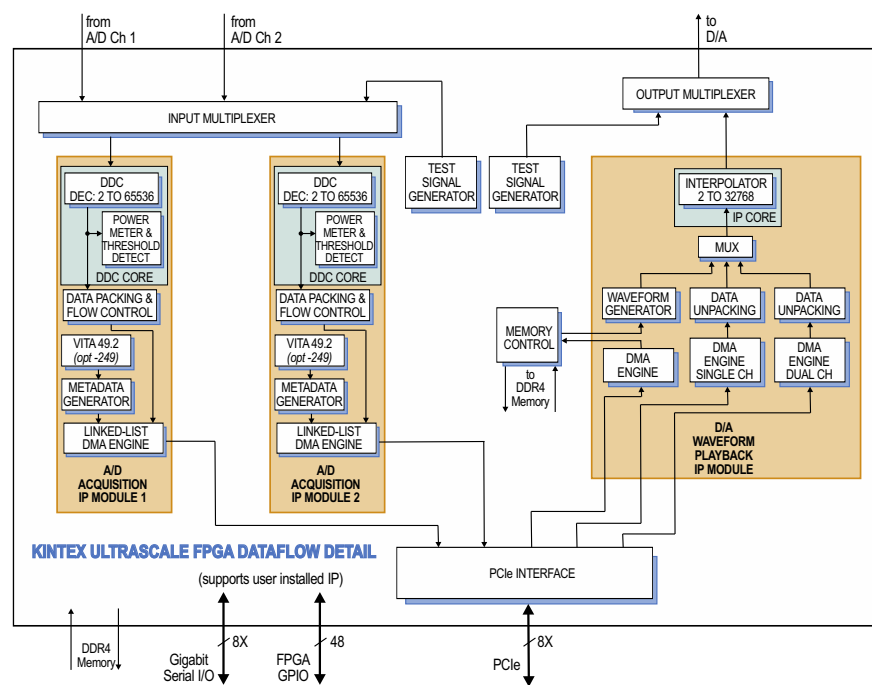
- Signal Data Packet Type
- Stream Identifier
- Integer Seconds Timestamp
- Fractions Seconds Timestamp
- Trailer

Programmable elements are:

- Packet Size
- Stream Identifier
- Trailer

The Timestamp is automatically inserted from the metadata engine. After initialization an externally applied 1 PPS pulse will increment the Integer Seconds Timestamp. A division of the sample clock will increment the fractional seconds timestamp and this count is reset by the 1 PPS pulse.

VITA 49 packets sent via DMA to the DAC/DUC for output will have the header, stream ID, timestamp and trailer removed leaving only the signal data to be transmitted.



### ► Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

### Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53851's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

### Memory Resources

The 53851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

### PCI Express Interface

The Model 53851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Fabric-Transparent Crossbar Switch

The 53851 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

### Specifications

#### Front Panel Analog Signal Inputs

**Input Type:** Transformer-coupled, front panel female SSMC connectors

**Transformer Type:** Coil Craft WBC4-6TLB

**Full Scale Input:** +5 dBm into 50 ohms

**3 dB Passband:** 300 kHz to 700 MHz

#### A/D Converters (standard)

**Type:** Texas Instruments ADS5463

**Sampling Rate:** 20 MHz to 500 MHz

**Resolution:** 12 bits

#### A/D Converters (option -014)

**Type:** Texas Instruments ADS5474

**Sampling Rate:** 20 MHz to 400 MHz

**Resolution:** 14 bits ►





The SPARK Development Systems are fully-integrated platforms for Pentek board-level products. They were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed. The system is equipped with sufficient power and cooling to ensure optimum performance.

**Ordering Information**

Model	Description
53851	2-Channel 500 MHz A/D with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 3U VPX

**Options:**

-014	400 MHz, 14-bit A/Ds
-084	XCKU060-2 FPGA
-087	XCKU115-2 FPGA
-104	LVDS FPGA I/O through VPX P2 connector
-105	Gigabit serial FPGA I/O through VPX P1 connector
-249	VITA 49-2 support
-702	Air cooled, Level L2
-763	Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions



**Digital Downconverters**

**Quantity:** Two channels  
**Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x  
**LO Tuning Freq. Resolution:** 32 bits, 0 to  $f_s$   
**LO SFDR:** >120 dB  
**Phase Offset Resolution:** 32 bits, 0 to 360 degrees  
**FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients  
**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**

**Type:** Texas Instruments DAC5688  
**Input Data Rate:** 250 MHz max.  
**Output IF:** DC to 400 MHz max.  
**Output Signal:** 2-channel real or 1-channel with frequency translation  
**Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation  
**Resolution:** 16 bits

**Digital Interpolator Core**

**Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x

**Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

**Front Panel Analog Signal Outputs**

**Output:** Transformer-coupled, front panel female SSMC connectors  
**Transformer:** Coil Craft WBC4-6TLB  
**Full Scale Output:** +4 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**

**Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**

**Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Array**

**Standard:** Xilinx Kintex UltraScale XCKU035-2  
**Option -084:** Xilinx Kintex UltraScale XCKU060-2  
**Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**

**Option -104:** provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O  
**Option -105:** Provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols

**Memory**

**Type:** DDR4 SDRAM  
**Size:** 5 GB  
**Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**

**PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**

**Standard: L0 (air cooled)**

**Operating Temp:** 0° to 50° C  
**Storage Temp:** -20° to 90° C  
**Relative Humidity:** 0 to 95%, non-condensing

**Option -702: L2 (air cooled)**

**Operating Temp:** -20° to 65° C  
**Storage Temp:** -40° to 100° C  
**Relative Humidity:** 0 to 95%, non-condensing

**Option -763: L3 (conduction cooled)**

**Operating Temp:** -40° to 70° C  
**Storage Temp:** -50° to 100° C  
**Relative Humidity:** 0 to 95%, non-condensing

**Size:** 3U VPX board 3.937 in x 6.717 in (100.00 mm x 170.61 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPX P2	20 pairs on VPX P2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No