New!

Model 53690 COTS (left) and rugged version

Cobalt
GateFlow
ReadyFlow
Board Support Package

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: *VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)*
- Ruggedized and conduction-cooled versions available

General Information

Model 53690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 53690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the

factory-installed functions and enable the 53690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ►
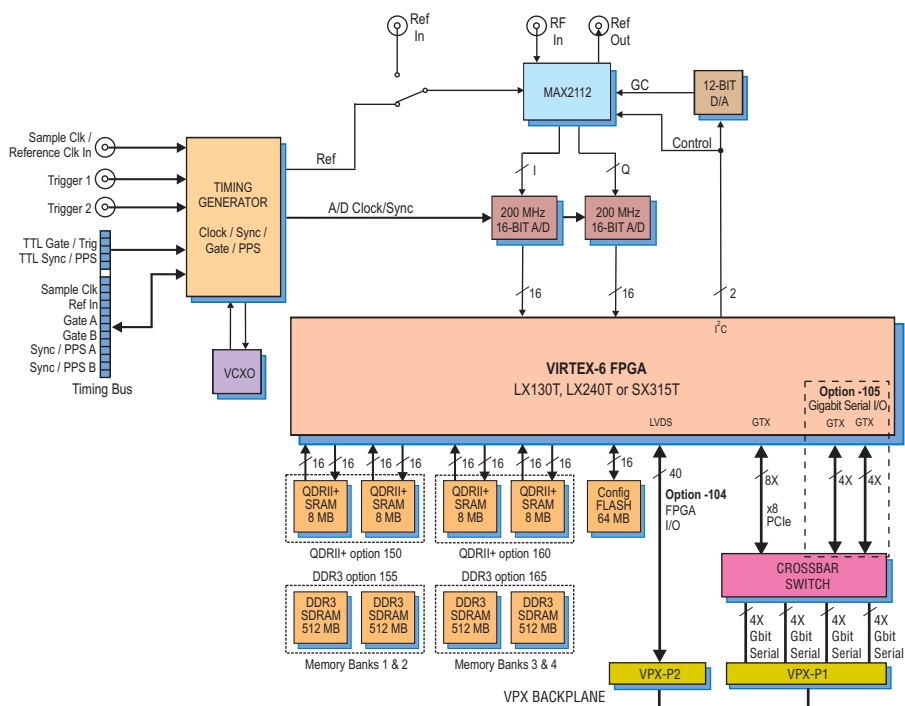
➤ RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchro-nization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board program-mable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. ➤

A/D Acquisition IP Modules

The 53690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

VIRTEX-6 FPGA DATAFLOW DETAIL
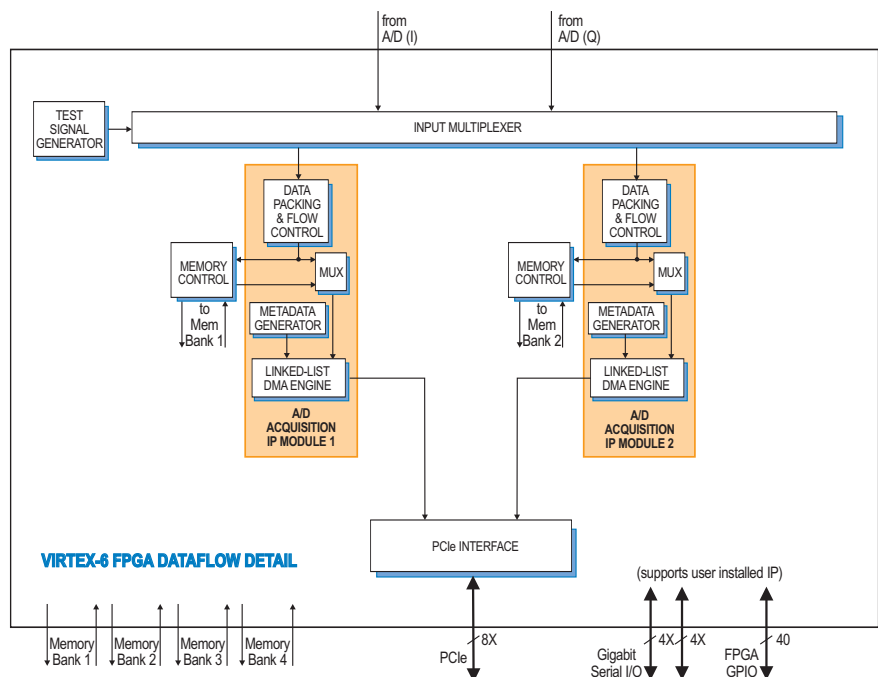
PCI Express Interface

The Model 53690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK
Development Systems

Ordering Information

Model	Description
53690	L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX

Options:

-062	XC6VLX240T FPGA
-064	XC6VSX315T FPGA
-104	LVDS FPGA I/O to VPX P2
-105	Gigabit serial FPGA I/O to VPX P1
-150	Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160	Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155	Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165	Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model	Description
8267	VPX Development System. See 8267 Datasheet for Options

➤ Built-in memory functions include multichannel A/D data capture, tagging and streaming. The factory-installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user IP within the FPGA.

Fabric-Transparent Crossbar Switch

The 53690 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuner
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
$freq_{VCO} = (N.F) \times freq_{REF}$
where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference ($freq_{REF}$**):** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
***Usable Full-Scale Input Range:** –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources: On-board timing generator/synthesizer
A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/ sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/ PPS inputs
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector for serial protocols
Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No