New!

Model 5350

Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX

Model 5350 commercial (left) and conduction-cooled version

GateFlow ReadyFlow Board Support Package

Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 1 GB of DDR2 SDRAM
- Two Xilinx Virtex-5 FPGAs
- Up to 2.56 seconds of data capture at 200 MHz
- LVPECL clock/sync bus for multiboard synchronization
- Up to 32 pairs of LVDS connections to the Virtex-5 FPGAs for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including:
  VITA-46 (VPX Baseline Standard)
  VITA-48 (VPX REDI)
  VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5350 is a high-speed data converter suitable for connection as the HF or IF input of a communications system. It features four 200 MHz, 16-bit A/Ds. These are supported by an array of data processing and transport resources ideally matched to requirements of high-performance systems.

The 5350 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts four full scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-5 FPGA for signal processing or for routing to other board resources.

Virtex-5 FPGAs

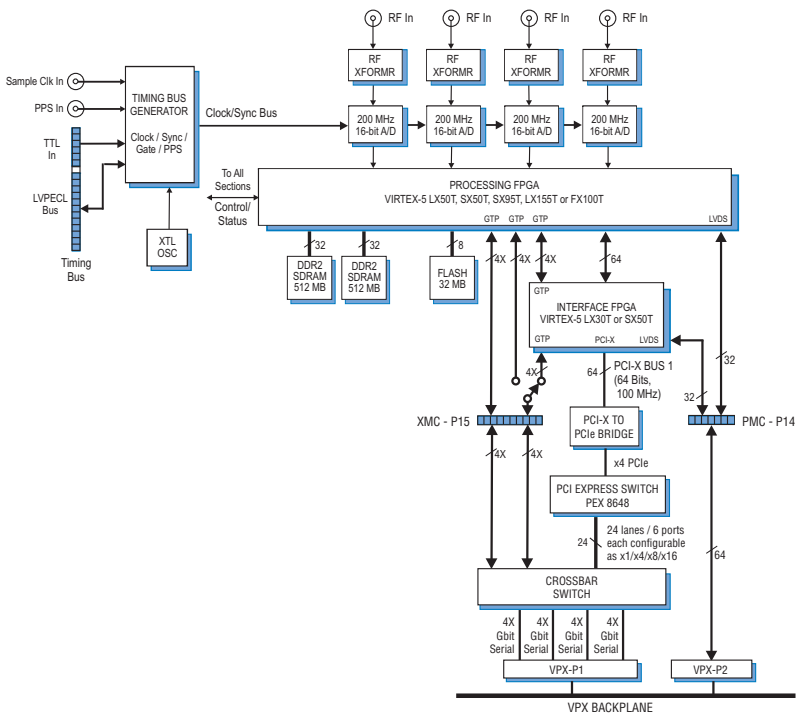
The Model 5350 architecture includes two Virtex-5 FPGAs. All data and control paths are accessible by the FPGAs, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control. In addition, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits facilitate integration of user-created IP.

There are two FPGA types on the 5350: processing and interface. The processing FPGA serves as a control and status engine with data and programming interfaces to each of the onboard resources including the A/D converters, DDR2 SDRAM memory, interface FPGA, programmable LVPECL I/O and clock, gate and synchronization circuits. The processing FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: Virtex-5 SX50T, SX95T, LX50T, LX155T and FX100T.

The SXT parts feature between 288 and 640 DSP48E Slices and are ideal for demodulation/modulation, decoding/encoding, decryption/encryption, digital delay and channelization of the signals between reception and transmission. For applications requiring more FPGA logic cells, the Model 5350 can be optionally configured with an LX155T in the processing FPGA position for 155,648 logic cells.

The interface FPGA provides board connections including PCI-X or PCI Express, preserving the processing FPGA resources for signal processing. The interface FPGA can be configured as an LXT or an SXT family part, providing not only interface functionality, but processing resources up to an additional 640 DSP48E Slices.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the processing FPGA, and 16 pairs of LVDS connections to the interface FPGA for custom I/O. ➤



PENTEK

Pentek, Inc. One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201·818·5900 ◆ Fax: 201·818·5904 ◆ Email: info@pentek.com
www.pentek.com

Model 5350

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Clocking and Synchronization

The Model 5350 architecture includes a flexible timing and synchronization circuit for each bank of four A/D converters, allowing the A/Ds to be clocked by internal or external clock sources and a multiboard timing bus.

Each timing bus includes a clock, a sync, two gate or trigger signals and a PPS signal. The timing bus can be driven by an internal crystal oscillator, a front panel reference input or the LVPECL bus.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVPECL inputs that drive the clock, sync, gate and PPS signals for the internal timing bus.

In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Up to three slave 5350s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. More boards can be synchronized with an external clock and sync generator.

Memory Resources

Up to two independent 512 MB banks of DDR2 SDRAM are available to the processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. Each memory bank can be easily accessed through the PCI interface using the on-board DMA controllers.

Custom user-installed functions within the FPGA can take advantage of all three banks to support various applications.

Fabric-Transparent Crossbar Switch

The 5350 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (x1) lanes, or groups of four lanes (x4).

PCI Express Switch

Model 5350 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Internal Clock:** 200 MHz crystal osc.
- **External Clock:** 10 to 200 MHz
- **Resolution:** 16 bits

A/D Data Reduction Mode: Data from the A/Ds can be decimated by any value between 1 and 4096

Clock Sources: Selectable from onboard crystal oscillators, external or LVPECL clocks

External Clock
- **Type:** Front panel female SMC connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms
- **Sync/Gate Bus:** 26-pin connector, clock/sync/gate/PPS input/output LVPECL bus; one gate/trigger and one sync/PPS input TTL signal

Field Programmable Gate Array
- **Processing FPGA:** Xilinx Virtex-5 XC5VSX50T standard; XC5VLX50T, XC5VSX95T, XC5VLX155T or XC5VFX100T, optional
- **Interface FPGA:** Xilinx Virtex-5 XC5VLX30T std.; XC5VSX50T optional

Custom I/O
- **Option -104:** Provides GPIO to VPX-P2 with 16 LVDS pairs to processing FPGA (SX95T, LX155T or FX100T only) and 16 pairs to interface FPGA

Memory
- **DDR2 SDRAM:** Up to 1 GB in two banks

PCI to PCIe Interface
- **PCI-X Bus:** 64-bits, 100 MHz and 64- or 32-bits at 33 or 66 MHz
- **DMA:** 4 channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:
- **Processing FPGA:** Two 4X ports to Fabric-Transparent Switch; one can be alternately routed to interface FPGA
- **VPX-P1**: Four 4X ports to Fabric-Transparent Crossbar Switch
- **PCI Express:** Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental
- **Operating Temperature:**
  Forced-Air Cooled: 0° to 50° C std; -20° to 65° C (Level L2)
  Conduction-Cooled: -40° to 70° C (Level L3)

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs - 3U VPX
Options:	
-104	FPGA I/O to VPX-P2
-5xx	Gigabit Serial I/O to VPX-P1- four full duplex 4X paths
-703	Level L3 Conduction-Cooled Version

Contact Pentek for additional available options.

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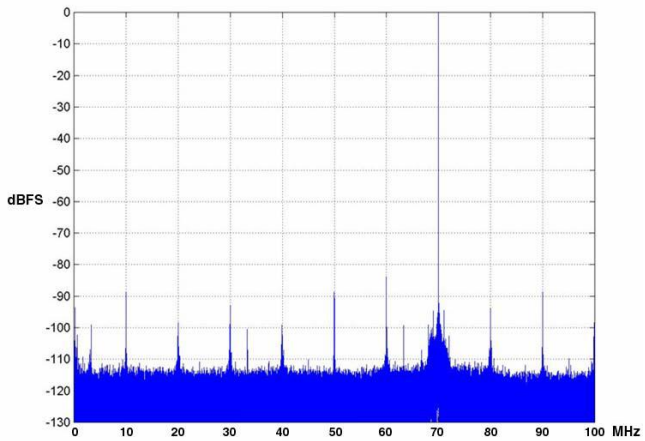
www.pentek.com

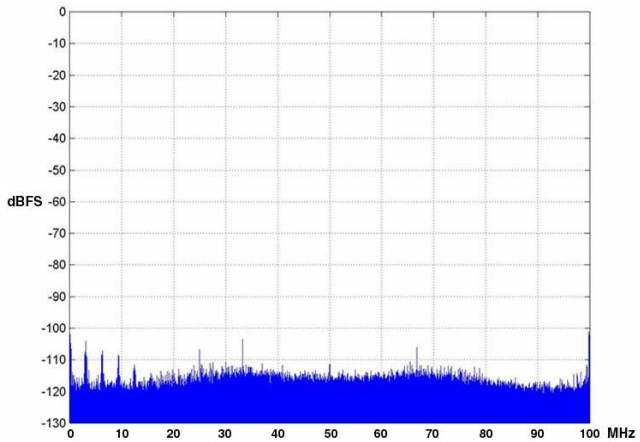
A/D Performance

Spurious-Free Dynamic Range



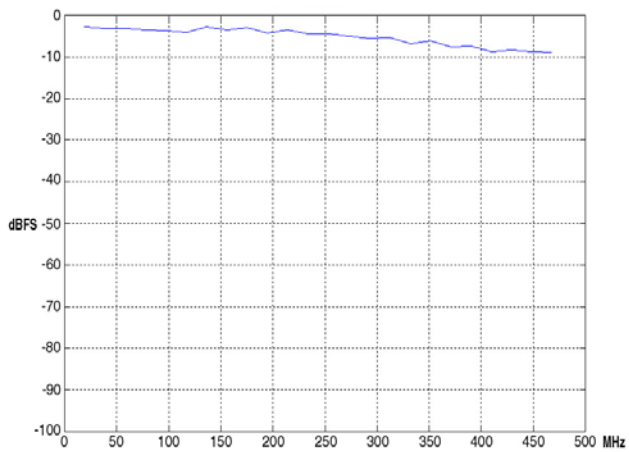
f_{in}= 70 MHz, f_s= 200 MHz, Internal Clock

Spurious Pickup



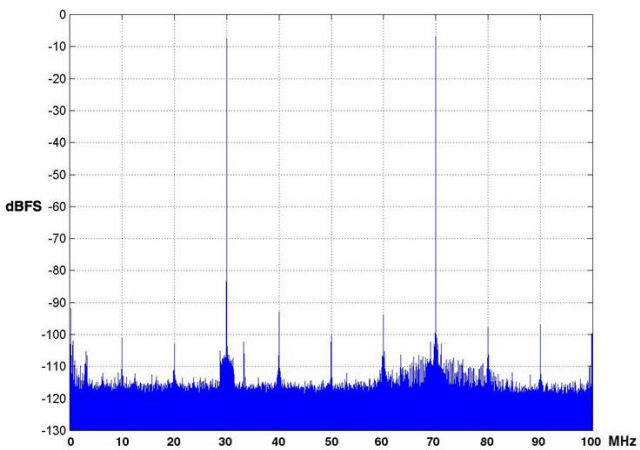
f_s= 200 MHz, Internal Clock

Input Frequency Response



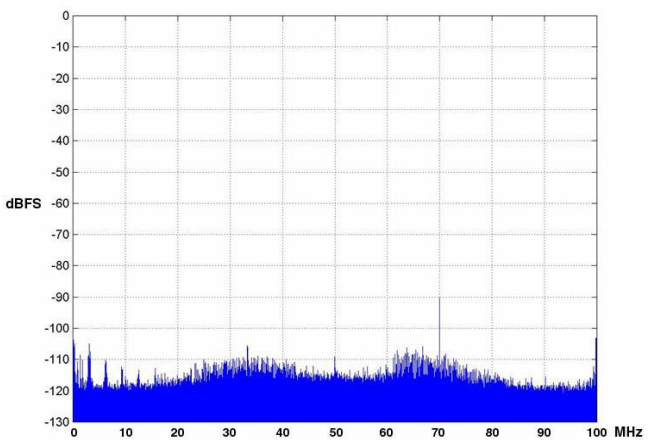
f_s= 200 MHz, Int. Clock

Two-Tone SFDR



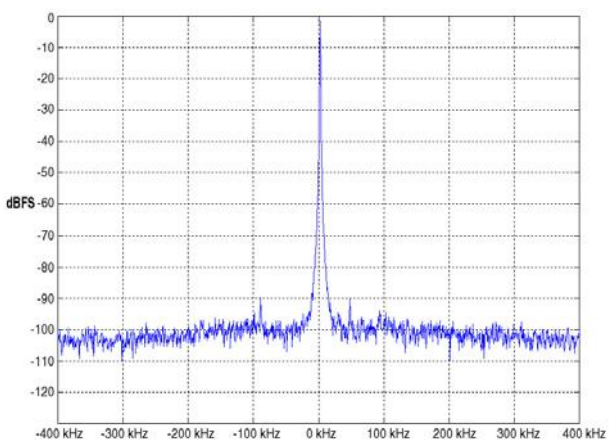
f_{in1}= 30 MHz, f_{in2}= 70 MHz, f_s= 200 MHz, Int. Clock

Adjacent Channel Crosstalk



f_{in}= 70 MHz, A_{in}= 0 dBFS, f_s= 200 MHz, Int. Clock

Phase Noise at 70 MHz



f_s= 200 MHz, Int. Clock