New!

Model 5342-428 Installed Core

GateFlow Transceiver with Four Multiband DDCs and Interpolation Filter - 3U VPX

ReadyFlow Board Support Package

Features

- Complete software radio interface solution
- 3U VPX form factor
- GateFlow IP Core 428, with four high-performance multiband DDCs and one Interpolation Filter, factory-installed
- Two sets of 18-bit user-programmable FIR filter coefficients
- Decimation range from 2 to 65,536 in steps of 1
- Interpolation range from 2 to 32,768 in steps of 4
- LVDS clock/sync bus for multiboard synchronization

General Information

Model 5342-428 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters with built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch bridges numerous interfaces and components on the board with no latency.

A/D and D/A Converter Stages

The front end accepts four full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into Linear Technology LTC2255 14-bit 125 MHz A/D converters.

The digital outputs are delivered to the Virtex-4 FPGA for signal processing or for routing to other board resources.

A TI DAC5686 digital upconverter (DUC) and D/A accepts a baseband real or complex data stream from the FPGA with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog output samples at up to 320 MHz to the 16-bit D/A converter. Output is through a front panel MMCX connector at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as an interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Core 428 Multiband DDCs

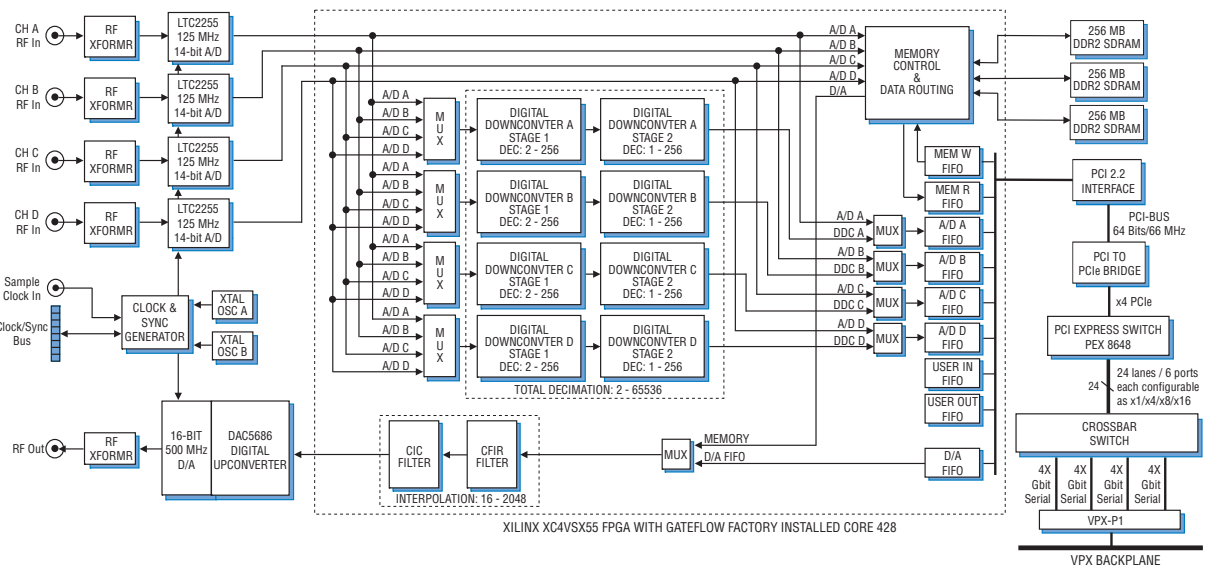
The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. Each filter is capable of any decimation from 2 to 256. The decimations of the first stage filter and the second stage filter multiply to yield overall decimation factors up to 65,536. The second stage FIR may be bypassed for decimations of 256 or lower. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain is primarily used to compensate for bit growth in the filter at different decimations but may also be used to amplify small signals after out of band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 5342-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overal decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

Core 428 Interpolation Filter

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC's built-in interpolation, creating a maximum interpolation factor of 32,768. ➤



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Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the input and output signals.

Each timing bus includes a clock, a sync, and a gate or trigger signal. Signals from either Timing Bus A or B can be selected as the timing source for the A/Ds, the downconverters, the upconverters and the D/As. Two external reference clocks are accepted, one for each timing bus and two internal clocks may be used for each timing bus.

Front panel 26-pin LVDS Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 5342-428's can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications like tracking receivers. User-installed functions within the FPGA can take advantage of the SDRAM for many other purposes.

Fabric-Transparent Crossbar Switch

The 5342-428 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5342-428 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +10 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
- **Sampling Rate:** 1 MHz to 125 MHz
- **Internal Clock:** 125 MHzcrystal oscillator
- **External Clock:** 1 to 125 MHz
- **Resolution:** 14 bits
- **A/D Data Reduction Mode:** Data from the A/Ds can be written directly into the FPGAs at a rate equal to A/D clock decimated by any value between 1 and 4096

Front Panel Analog Signal Output
- **Output Type:** Transformer-coupled, front panel female MMCX connectors
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 60 kHz to 300 MHz

Digital Upconverter
- **Type:** TI DAC5686
- **Input Bandwidth:** 40 MHz, max.
- **Output IF:** DC to 160 MHz
- **Output Signal:** Analog, real or quadrature
- **Sampling Rate:** 320 MHz, max; 500 MHz max. with upconversion disabled
- **Resolution:** 16 bits

Clock Sources: Selectable from onboard A or B crystal oscillators, external or LVDS clocks

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC- coupled, 50 ohms

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Arrays
- **Type:** Xilinx Virtex-4 XC4VSX55 and Xilinx Virtex-4 XC4VFX60

Memory
- **DDR2 SDRAM:** 768 MB in three banks of 256 MB each

PCI to PCIe Interface
- **PCI Bus:** 64-bit, 66 MHz
- **DMA:** 9 channel demand-mode and chaining controller

Gigabit Serial I/O
- **VPX-P1**: Four 4X ports to Fabric-Transparent Crossbar Switch
- **PCI Express:** Six ports to Fabric-Transparent Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
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Contact Pentek for available options

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