

New!

Model 5341

Dual Multiband Transceiver with FPGA - 3U VPX



Features

- Complete software radio interface solution for 3U VPX systems
- Supports Gigabit Serial Fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 125 MHz 14-bit A/Ds
- Four digital downconverters
- One digital upconverter
- Two 500 MHz 16-bit D/As
- 512 MB of DDR SDRAM
- Xilinx Virtex-II Pro FPGA
- Up to 1.28 seconds of delay or data capture at 100 MHz
- Dual timing buses for independent input and output clock rates
- LVDS clock/sync bus for multiboard synchronization
- 32 pairs of LVDS connections to the Virtex-II Pro FPGA for custom I/O
- Compatible with several VITA standards including:
 - VITA-46 (VPX Baseline Standard)
 - VITA-48 (VPX REDI)
 - VITA-65 (OpenVPX™ System Specification)

General Information

Model 5341 is a software radio transceiver suitable for connection to HF or IF ports of a communications system. It features two A/D and two D/A converters, and is capable of bandwidths to 50 MHz and above.

The 5341 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration adds gigabit serial data paths for Xilinx Aurora or Serial RapidIO applications.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel MMCX connectors at +10 dBm into 50 ohms with transformer coupling into LTC2255 14-bit 125 MHz A/Ds.

The digital outputs are delivered into the Virtex-II Pro FPGA for signal processing or for routing to other module resources.

Digital Downconverter Stage

The 5341 features a TI/Graychip GC4016 quad digital downconverter, accepting either four 14-bit inputs or three 16-bit digital inputs from the FPGA, which determines the source of GC4016 input data. These sources include the A/Ds, FPGA signal

processing engine, SDRAM delay memory and data sources on the VPX backplane.

Each GC4016 channel may be set for independent tuning frequency and bandwidth. For an A/D sample clock frequency of 100 MHz, the output bandwidth for each channel ranges from 5 kHz up to 2.5 MHz. By combining channels, output bandwidth of up to 5 or 10 MHz can be achieved.

Digital Upconverter Stage

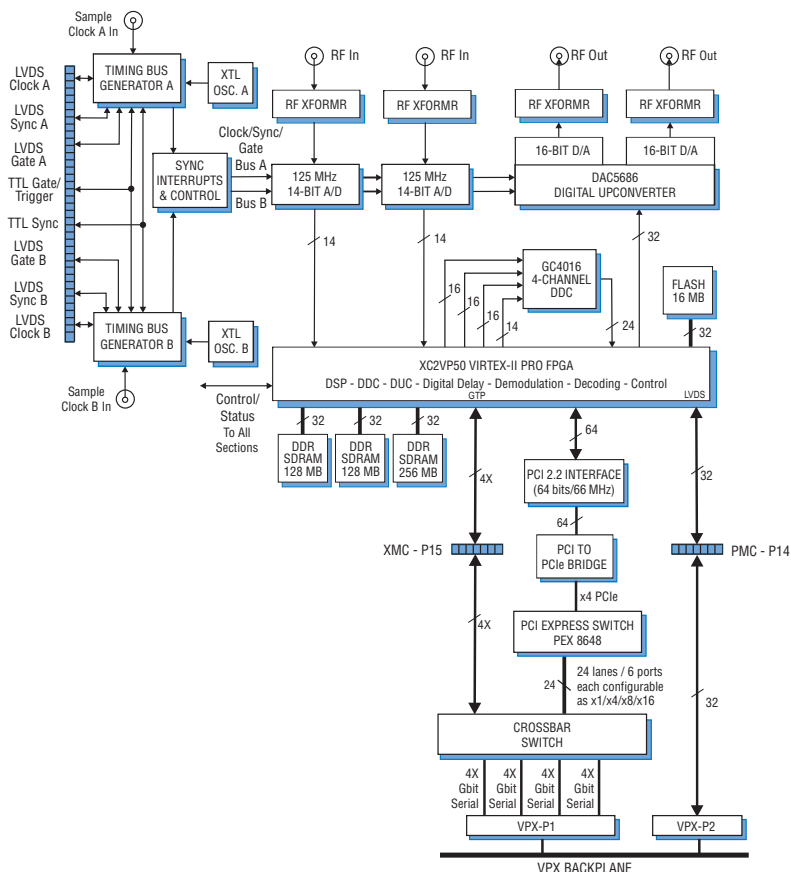
A TI DAC5686 digital upconverter and dual D/A is attached to the FPGA, accepting baseband real or complex data streams with signal bandwidths up to 40 MHz.

When operating as an upconverter, it interpolates and translates real or complex baseband input signals to any IF center frequency between DC and 160 MHz. It delivers real or quadrature (I+Q) analog outputs through two 320 MHz 16-bit D/A converters to two front panel MMCX connectors at +4 dBm into 50 ohms.

If translation is disabled, the DAC5686 acts as a two channel interpolating 16-bit D/A with output sampling rates up to 500 MHz.

Virtex-II Pro FPGAs

A Xilinx XC2VP50 Virtex-II Pro FPGA serves as a control and status engine with ▶



Fabric-Transparent Crossbar Switch

The 5341 features a unique high-speed switching configuration. A fabric-transparent crossbar switch connects the PCI Express switch with the VPX-P1 connector using gigabit serial data paths with no latency. This allows the user to select the desired output port on VPX-P1. Programmable signal input equalization and output pre-emphasis settings on the Crossbar Switch enable optimization.

PCI Express Switch

Model 5341 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Ordering Information

Model	Description
5341	Dual Multiband Transceiver with FPGA - 3U VPX
Options:	
-002	Full-scale output: -2 dBm into 50 ohms; 3 dB passband: 400 kHz to 800 MHz
-050	XC2VP50 Virtex-II Pro FPGA
-100	100 MHz Bus A and Bus B oscillators
-101	TI DAC5687 replaces the TI DAC5686
-104	FPGA I/O to VPX-P2
-125	125 MHz Bus A and 100 MHz Bus B internal oscillators
-420	Dual wideband DDC and digital interpolation filter cores, factory-installed in FPGA
-430	256-channel narrowband DDC core, factory-installed in FPGA
-5xx	Gigabit Serial I/O to VPX-P1 - four full-duplex 4X paths

► data and programming interfaces to each of the on-board resources including the A/D converters, digital downconverter, digital upconverter and D/A converters. Factory installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Option -104 provides general purpose I/O to VPX-P2 with 16 pairs of LVDS connections to the FPGA. Option -5xx adds four full duplex 4X gigabit serial paths to VPX-P1 connector.

Clocking and Synchronization

Two independent internal timing buses can provide either a single clock or two different clock rates for the corresponding input and output signals.

Each timing bus includes a clock, sync, and gate or trigger signal. Signals from either Timing Bus can be selected as the timing source for the A/Ds, downconverter, upconverter and D/As. Two external reference clocks or two internal clocks may be used for each timing bus.

A front panel 26-pin LVDS Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, each accepts differential LVDS inputs that drive the clock, sync and gate signals for the two internal timing buses.

In the master mode, the LVDS bus can drive one or both sets of timing signals from the two internal timing buses for synchronizing multiple boards.

Up to seven slave 5341 boards can be driven from the LVDS bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

Three independent banks of SDRAM are available to the FPGA (to 1 GB max.). Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering; a D/A waveform generator mode; and an A/D data delay mode for applications such as tracking receivers.

The SDRAMs are also available as a resource for the two PowerPC processor cores within the FPGA. A 16 MB FLASH memory supports booting and program store for these processors.

Specifications

Analog Signal Inputs

Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC1-1TLB
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 250 kHz to 300 MHz

A/D Converters

Type: Linear Technology LTC2255
Sampling Rate: 1 MHz to 125 MHz
Internal Clock: Crystal osc. (2 per A/D)
External Clock: 1 to 125 MHz
Resolution: 14 bits

Digital Downconverter

Type: TI/Graychip GC4016
Decimation: 32 to 16,384; with channel combining mode: 8 or 16
Data Source: A/D, FPGA, or PCI interface
Control Source: FPGA or PCI interface
Output: Parallel complex data

Receiver Bypass Mode: Data from the A/Ds can be written directly into the FPGAs at a rate equal to the A/D clock decimated by any integer between 1 and 4096

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female MMCX connectors
Full Scale Output: +4 dBm into 50 ohms
Option -002: -2 dBm into 50 ohms
3 dB Passband: 60 kHz to 300 MHz
Option -002: 400 kHz to 800 MHz

Digital Upconverter

Type: TI DAC5686
Input Bandwidth: 40 MHz, max.
Output IF: DC to 160 MHz
Output Signal: Analog, real or quadrature
Sampling Rate: 320 MHz, max; 500 MHz max. with upconversion disabled
Resolution: 16 bits

Clock Sources: Selectable from onboard crystal oscillators, external or LVDS clocks

External Clocks

Type: Female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohm

Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Field Programmable Gate Array

Type: Xilinx Virtex-II Pro
Option -050: XC2VP50
Option -104: 64 lines (32 pairs)

Memory

DDR SDRAM: 512 MB in three banks
FLASH: One bank of 16 MB

PCI to PCIe Interface

PCI Bus: 64-bit, 66 MHz
DMA: 9-channel demand-mode and chaining controller per PCI bus

Gigabit Serial I/O:

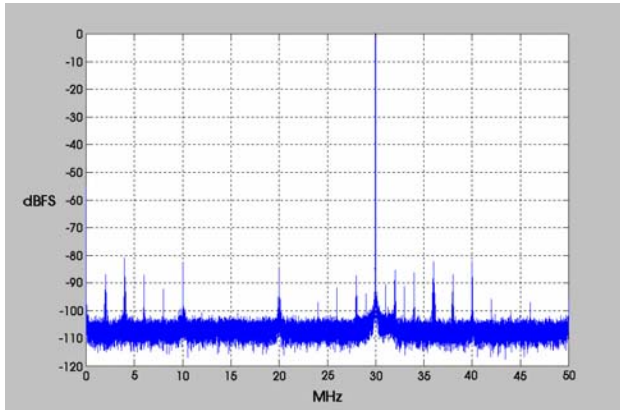
FPGA: One 4X port to Crossbar Switch
VPX-P1: Four 4X ports to Crossbar Switch
PCI Express: Six ports to Crossbar Switch, each configurable as x1, x4, x8 or x16 lanes, 24 lanes total

Environmental (Commercial version)

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

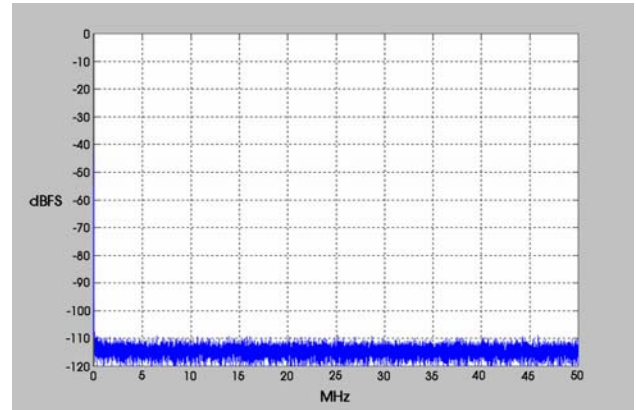
A/D Performance

Spurious Free Dynamic Range



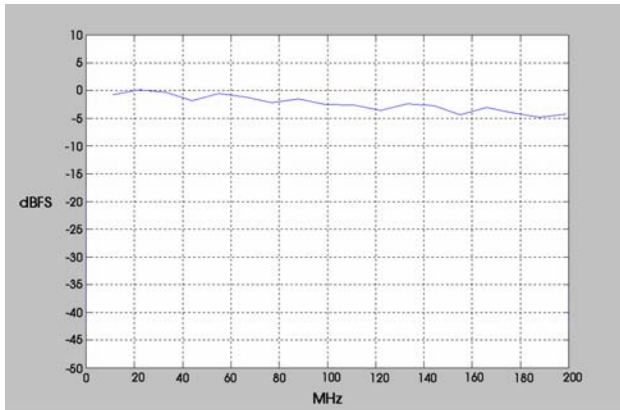
$f_{in} = 70 \text{ MHz}, f_s = 100 \text{ MHz}$

Spurious Pick-up



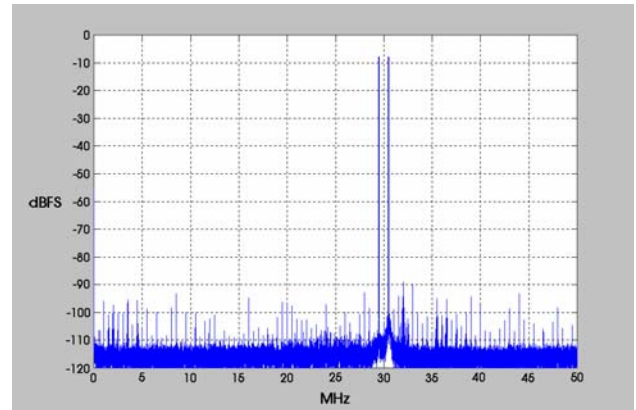
$f_s = 100 \text{ MHz}, 32k \text{ point FFT}, 8 \text{ averages}$

Input Frequency Response



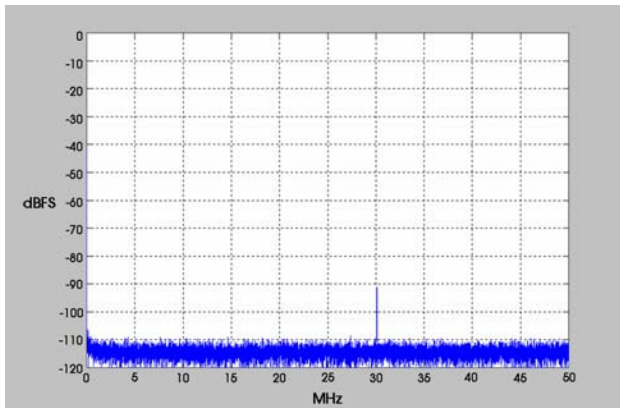
$f_s = 100 \text{ MHz}$

Two-Tone SFDR



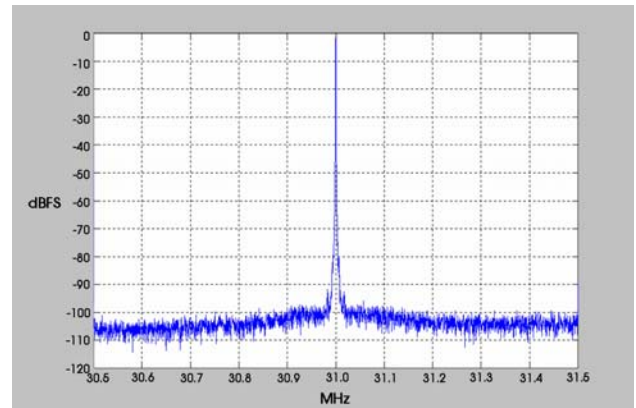
$f_1 = 29.5 \text{ MHz}, f_2 = 30.5 \text{ MHz}, f_s = 100 \text{ MHz}$

Crosstalk



$f_{in \text{ Ch2}} = 69 \text{ MHz}, f_s = 100 \text{ MHz}, \text{ Ch 1 shown}$

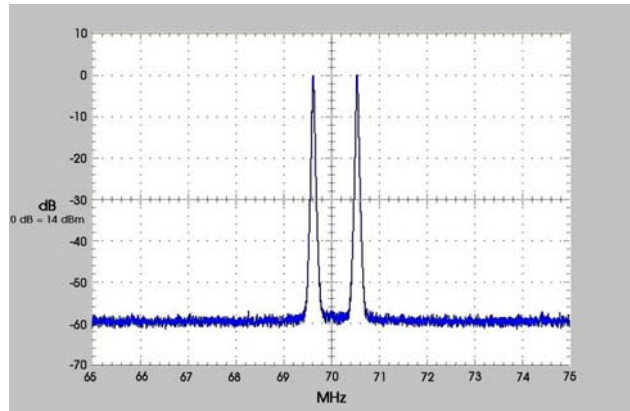
Phase Noise



$f_{in} = 69 \text{ MHz}, f_s = 100 \text{ MHz}$
Phase Noise @ 100 kHz = $-102 - 10 \cdot \log(610) = -129.8 \text{ dB/Hz}$

D/A Performance

Two-Tone Intermodulation Distortion



$f_1 = 69.5 \text{ MHz}$, $f_2 = 70.5 \text{ MHz}$, $f_s = 100 \text{ MHz}$