General Information

The Flexor® Model 3316 is a multi-channel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3316 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3316

The true performance of the 3316 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

A/D Acquisition IP Modules

With the 3316 installed on a Pentek FMC carrier, the FlexorSet features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s task of identifying and executing on the data.

Features

- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available

Features

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- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available
8-Channel 250 MHz, 16-bit A/D - FMC

SPARK Development Systems
SPARK systems are fully-integrated saving engineers and system integrators the time and expense associated with building and testing a development system. SPARK systems ensure the optimum performance of Pentek boards and are available in 3U VPX (Model 8267) and in a PC environment (Model 8266).

Ordering Information

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<th>Model</th>
<th>Description</th>
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<tr>
<td>3316</td>
<td>8-Channel 250 MHz 16-bit A/D - FMC module</td>
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Options:
- 3316-990 Reference design for 3316 installed on Xilinx VC707 Evaluation Kit

3U VPX FlexorSet Description
- 5973-316 8-Channel 250 MHz A/D with Virtex-7 FPGA
- 5973-317 8-Channel 250 MHz A/D, Virtex-7 FPGA with 8 multiband DDCs and interpolator
- 5983-317 8-Channel 250 MHz A/D, Kintex UltraScale FPGA with 8 multiband DDCs and interpolator

PCle FlexorSet Description
- 7070-316 8-Channel 250 MHz A/D with Virtex-7 FPGA - x8
- 7070-317 8-Channel 250 MHz A/D, Virtex-7 FPGA with 8 multiband DDCs and interpolator - x8

Contact Pentek for availability of rugged and conduction-cooled versions and other support options

Model 3316 Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBM into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- Type: Front panel connector, sine wave, 0 to +10 dBM, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin-Count FMC

FMC Interface
The Model 3316 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3316 and the FMC carrier.
## Pentek FlexorSet Models

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<td>8 Ch 250 MHz 16-bit A/D</td>
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<td>Kintex UltraScale</td>
<td>Navigator BSP</td>
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<td>4 Ch 250 MHz A/D &amp; 2 Ch 800 MHz D/A with 4 multiband DDCs &amp; interpolation filters</td>
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</table>
General Information

Model 5973-316 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Features
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCIe Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical configuration for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 5973-316 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS421869 dual 250 MHz, 16-bit A/D converters.
Memory Resources

The 5973-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 5973-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Option -076: Xilinx Virtex-7 XC7VX690T-2
- Custom FPGA I/O
  - 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
  - Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
  - Optical (Option -110): VITA-66.4, 12X optical interface
- Memory
  - Type: DDR3 SDRAM
  - Size: Four banks, 1 GB each
  - Speed: 800 MHz (1600 MHz DDR)
- PCI-Express Interface
  - PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
  - Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information
Model 5973-317 is a member of the Flexor family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 5973-317 includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture
Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The 5973-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8^*f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.
Memory Resources
The 5973-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 5973-317 includes an industry-standard interface fully compliant with PCI-e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

SPARK Development Systems
The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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Options:
-104    | LVDS FPGA I/O to VPX P2                          |
-110    | VITA-66.4 12X optical interface                  |

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267
VPX Development System
See 8267 Datasheet for Options

In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage
The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to fs
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.

### Features

- **VITA-57.4 HSPC FMC+ site** offers access to a wide range of possible I/O
- **Supports Xilinx Kintex UltraScale FPGA**
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB and 5 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- **PCI Express (Gen. 1, 2 & 3)** interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- **LVDS connections to the Kintex UltraScale FPGA** for custom I/O and synchronization
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-85 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
**A/D Acquisition IP Modules**

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of the transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

**A/D Converter Stage**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

**Memory Resources**

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

**PCI Express Interface**

The Model 5983-317 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported.
GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Eight channels
- Decimation Range: 2x to 32,768x in three stages of 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale XCKU060-2
- Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- Type: DDR4 SDRAM
- Size: Two banks, one 4 GB and one 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: −20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -763: L3 (conduction cooled)
  - Operating Temp: −40° to 70° C
  - Storage Temp: −50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:
- SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information
Model  Description
5983-317 8-Channel 250 MHz A/D with DDCs and Kintex Ultra Scale FPGA - 3U VPX

Options:
-087  XCKU115-2 FPGA
-110  VITA-66.4 12X optical interface
-180  GPS Support
-702  Air cooled, Level L2
-763  Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model  Description
8267  VPX Development System
See 8267 Datasheet for Options
General Information

Model 7070-316 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPOptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting. Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control.

The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The first option to load is an alternate image from FLASH through software control.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

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Memory Resources
The 7070-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface
The Model 7070-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled,
  - **Size:** 4.376 in. x 7.948 in (111.2 mm x 201.6 mm)

Ordering Information

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<td>8266</td>
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**General Information**

Model 7070-317 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-317 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**The Flexor Architecture**

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-317 to operate as a turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The 7070-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

Option -104 provides 16 pairs of LVDS interboard communication between the FPGA and a card-edge connector for custom I/O.
FlexorSet Model 7070-317

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

- Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MT optical connector is presented on the PCIe slot panel.

A/D Acquisition IP Modules

The 7070-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress\textsuperscript{R}, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate user image left in nonvolatile memory or a test signal generator.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.
Memory Resources

The 7070-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 7070-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

SPARK Development Systems

The Model 8266 is a fully-integrated PC development system for Pentek PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Digital Downconverters

Quantify: Eight channels

Decimation Range: 2x to 65,536x in two stages of 2x to 256x

LO Tuning Freq. Resolution: 32 bits, 0 to fs

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O

Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled,

Size: 4.376 in. x 7.948 in (111.2 mm x 201.6 mm)
Pentek offers the option -990 reference design with software and IP support for the Pentek Model 3316 when installed on the Xilinx VC707 Evaluation Kit board.

The Virtex®-7 FPGA VC707 Evaluation Kit is a PCIe platform using the Virtex-7 XC7VX485T-2FFG1761C. It includes basic components of hardware, design tools, IP, and preverified reference designs.

When coupled with Pentek’s option -990 reference design for the 3316, the user has a complete development environment for custom applications. The industry-standard FPGA Mezzanine Connectors (FMC) are directly compatible with the 3316.

**Features**

- Supports the Xilinx Virtex-7 FPGA
- Complete development environment with Pentek’s reference design
- Supports the Pentek Model 3316 FMC I/O Module

**Ordering Information**

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The Xilinx Virtex®-7 FPGA VC707 Evaluation Kit gives designers an easy starting point for evaluating and leveraging devices that deliver breakthrough performance, capacity, and power efficiency. Out of the box, this platform speeds time to market for the full-range of Virtex-7 FPGA-based applications including advanced systems for wired and wireless communications, aerospace and defense. The highly flexible kit combines fully integrated hardware, software, and IP with preverified reference designs that maximize productivity and let designers immediately focus on their unique project requirements.

The Flexor® Model 3316 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.