Founded in 1986, Pentek has become the premier source for high-speed real-time recording systems, DSP (Digital Signal Processing), SDR (Software-Defined Radio), and data acquisition products. Our customers enjoy our ISO 9001 SGS certification and the performance and flexibility afforded by our board- and system-level commercial and ruggedized product lines and our world-class applications support.

Pentek is the leading board and system manufacturer offering COTS and ruggedized products in formats such as VPX, PMC/XMC, PCI Express, AMC, FMC, CompactPCI, and PCI, featuring the latest Xilinx Virtex and Kintex FPGAs.

Pentek’s data acquisition line is extensive and includes A/Ds, D/As, Digital Receivers/Transmitters, Digital I/O, Analog RF downconverters, High-speed recorders, Development systems and more.

No other embedded vendor can provide such seasoned, in-depth technical expertise in data acquisition, digital signal processing and software-defined radio.

Pentek’s mission is to provide the embedded community with leading edge board- and system-level solutions for the most demanding requirements in data acquisition, digital signal processing and software radio applications through excellence and innovation.

We support an aggressive new product development cycle to meet market demands as we design the next generation of embedded products.

We consistently invest more than 15% of revenues in product development, engineering and applications support.

We will help you solve the most challenging DSP problems through our dedicated staff of systems engineers who are trained to provide the answers to your hardware, software or applications questions.

We recognize today’s time-to-market pressures and budget constraints on development resources and we offer low-risk, easy-to-use embedded solutions.

You can select from the industry’s most extensive line of advanced analog and digital I/O products, along with exclusive development tools that help you create a custom system. Many of these products include Xilinx Virtex or Kintex FPGAs for customized processing.

High-Speed Real-Time Recording Systems
- Economical alternatives to in-house development
- Fully tested and ready to run right out-of-the-box
- Easy to use with full-featured software installed

Processor Engines
- Xilinx Virtex and Kintex FPGAs

Data Acquisition
- Single or multichannel A/Ds and D/As
- Sampling rates to 3.6 GHz
- Resolution to 24 bits

Software Radio
- Up to 1100 channels per slot
- Narrow-, wide- and multi-band versions
- Digital downconverters and upconverters
- Analog downconverters
- Development systems

For more information about us, please visit: http://pentek.com/about/about.cfm?HID2=TM
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<td>Jade 71841</td>
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<td>PC Development System for PCIe Cobalt, Onyx, Jade and Flexor Boards</td>
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**Customer Information**

**Last updated: March 2018**
Model 71620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - XMC

General Information

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board’s analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Modules

The 71620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven module. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back the dual D/As waveforms stored in either onboard memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71620’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Options:

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<th>Option Code</th>
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<td>XC6VLX240T FPGA</td>
</tr>
<tr>
<td>-064</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O through P14 connector</td>
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<td>-105</td>
<td>Gigabit serial FPGA I/O through P16 connector</td>
</tr>
<tr>
<td>-150</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)</td>
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<tr>
<td>-160</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)</td>
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<tr>
<td>-155</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
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<tr>
<td>-165</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
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Ordering Information

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<th>Model</th>
<th>Description</th>
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<tr>
<td>71620</td>
<td>3-Ch. 200 MHz A/D and 2-Ch. 800 MHz D/A with Virtex-6 FPGA - XMC</td>
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Specifications

Front Panel Analog Signal Inputs

<table>
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<tr>
<th>Input Type</th>
<th>Transformer-coupled, front panel female SSMC connectors</th>
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<tr>
<td>Transformer Type</td>
<td>Transformer Type: Coil Craft</td>
</tr>
<tr>
<td>WBC4-6TLB</td>
<td>Full Scale Input: +8 dBm into 50 ohms</td>
</tr>
<tr>
<td>3 dB Passband: 300 kHz to 700 MHz</td>
<td></td>
</tr>
</tbody>
</table>

A/D Converters

| Type | Texas Instruments ADS5485 |
| Resolution | 16 bits |

D/A Converters

| Type | Texas Instruments DAC5688 |
| Input Data Rate | 250 MHz max. |
| Output IF | DC to 400 MHz max. |
| Output Signal | 2-channel real or 1-channel with frequency translation |
| Output Sampling Rate | 800 MHz max. with interpolation |
| Resolution | 16 bits |

Front Panel Analog Signal Outputs

| Output Type | Transformer-coupled, front panel female SSMC connectors |
| Transformer Type | Transformer Type: Coil Craft |
| WBC4-6TLB | Full Scale Output: +4 dBm into 50 ohms |
| 3 dB Passband: 300 kHz to 700 MHz |

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

| Clock Source | Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus |
| Synchronization | VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz |
| Clock Dividers | External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock |

External Clock

| Type | Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference |

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

| Standard | Xilinx Virtex-6 XC6VLX130T |
| Optional | Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T |

Custom I/O

| Option -104 | Installs the PMC P14 connector with 20 LVDS pairs to the FPGA |
| Option -105 | Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA |

Memory

| Option 150 or 160 | Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR |
| Option 155 or 165 | Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR |

PCI-Express Interface

| PCI Express Bus | Gen. 1 x4 or x8; Gen. 2: x4 |

Environmental

| Operating Temp | 0° to 50° C |
| Storage Temp | -20° to 90° C |
| Relative Humidity | 0% to 95%, non-cond. |
| Size | Standard XMC module, 2.91 in. x 5.87 in. |

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
General Information

Model 71621 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71621 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface completely the factory-installed functions and enable the 71621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Modules

The 71621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a linked definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Core

In addition to the DDCs, the 71621 features a complete beamforming subsystem. Each DDC core contains programmable I & Q filters, gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module for reading over the PCIe. For larger systems, multiple 71621’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71621 factory-installed functions include a sophisticated D/A Waveform Playback IP Module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stage
The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71621's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources
The 71621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two bank of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface
The Model 71621 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71621 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple modules.

PCI Express Interface
The Model 71621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Digital Downconverters**

- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to ƒs
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

**Digital Interpolator**

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

**Beamformer**

- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One channel in and one channel out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

**Front Panel Analog Signal Outputs**

- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VXCO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Clock Dividers**

- **Type:** Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VXCO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**

- **Type:** Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VXCO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard XMC module, 2.91 in. x 5.87 in.

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC</td>
</tr>
</tbody>
</table>

**Options:**

- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS FPGA I/O through P14 connector
- 150 Two 8 MB QDR II+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDR II+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

**Memory:**

- Option 150 or 160: Two 8 MB QDR II+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

**Environmental**

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

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**Contact Pentek for availability of rugged and conduction-cooled versions**
Model 71624 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 71624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

### Adaptive Relay Input Overview

The Model 71624 digitizes two analog IF inputs using two 200 MHz 16-bit A/Ds. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

### Adaptive Relay Output Overview

The Model 71624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory. DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation). The translated DUC outputs are directed to either of two summation blocks, each...
associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 71624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8 \times f_s / N$, where $N$ is the decimation setting and $f_s$ is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 71624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 71624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.
A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to \( f_s \) where \( f_s \) is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

**Summation Blocks**

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

**D/A Converters**

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71624’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**PCI Express XMC Interface**

The Model 71624 complies with the VITA 42.0 XMC specification. The primary XMC connector on P15 supports an industry-standard interface fully compliant with PCIe Gen. 1 x8, bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the module.

**Form Factor Adaptors**

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.
### Dual-Channel, 34-Signal Adaptive IF Relay - XMC

**Ordering Information**

<table>
<thead>
<tr>
<th>Model 71624</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dual-Channel 34-Signal</td>
</tr>
<tr>
<td></td>
<td>Adaptive IF Relay - XMC</td>
</tr>
</tbody>
</table>

**Options:**

- 064      XC6VSX315T (required)  
- 702      L2 (air cooled)      
- 712      L2 (conduction cooled)  
- 730      2-slot heatsink

**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors  
- **Transformer Type:** Coil Craft WBC4-6TLB  
- **Full Scale Input:** +8 dBm into 50 ohms  
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Quantity:** 2  
- **Type:** Texas Instruments ADS5485  
- **Sampling Rate:** 10 MHz to 200 MHz  
- **Resolution:** 16 bits

**Digital Downconverters**

- **Quantity:** 34  
- **Decimation Range:** 512 to 8192, in steps of 8  
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)  
- **LO SFDR:** >100 dB  
- **Phase Offset:** 1 bit, 0 or 180 degrees  
- **FIR Filter:** 18-bit coefficients  
- **Output:** Complex, 16-bit I + 16-bit Q  
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Input Gain Blocks**

- **Quantity:** 34  
- **Data:** Complex, 16-bit I + 16-bit Q  
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

**Output Gain Blocks**

- **Quantity:** 34  
- **Data:** Complex, 16-bit I + 16-bit Q  
- **Gain Range:** 16-bit Q8.8 format, approximately +/- 48 dB

**Digital Upconverters**

- **Quantity:** 34  
- **Interpolation Range:** 512 to 8192, in steps of 8  
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)  
- **LO SFDR:** >120 dB  
- **FIR Filter:** 18-bit coefficients, 16-bit output  
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**

- **Analog Output Channels:** 2  
- **Type:** Texas Instruments DAC5688  
- **Input Data Rate:** 200 MHz max.  
- **Output Signal:** Real  
- **Output Sampling Rate:** 800 MHz max. with 4x interpolation  
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus  
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz  
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Field Programmable Gate Array**

- **Required:** Xilinx Virtex-6 XC6VSX315T

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8;

**Environmental**

- **Standard:**  
  - Operating Temp: 0° to 50° C  
  - Storage Temp: -20° to 90° C  
  - Relative Humidity: 0 to 95%, non-cond.

- **Option 702 L2 Extended Temp (air-cooled):**  
  - Operating Temp: -20° to 65° C  
  - Storage Temp: -40° to 100° C  
  - Relative Humidity: 0 to 95%, non-cond.

- **Option 712 L2 Extended Temp (conduction-cooled):**  
  - Operating Temp: -20° to 65° C  
  - Storage Temp: -40° to 100° C  
  - Relative Humidity: 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.
Model 71630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

General Information

Model 71630 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71630 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or S315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.
The Model 71630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**A/D Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The Model 71630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

**Memory Resources**

The Model 71630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

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**Figure:**

Diagram showing the integration of the A/D and D/A modules with various signals and connectivity interfaces.
**Model 71630**

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

**XMC Interface**

The Model 71630 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71630 supports 8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

**PCI Express Interface**

The Model 71630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **A/D Converter**
  - **Type:** Texas Instruments ADS5400
  - **Sampling Rate:** 100 MHz to 1 GHz
  - **Resolution:** 12 bits
- **D/A Converter**
  - **Type:** Texas Instruments DAC5681Z
  - **Input Data Rate:** 1 GHz max.
  - **Interpolation Filter:** bypass, 2x or 4x
  - **Output Sampling Rate:** 1 GHz max.
  - **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**

- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
  - **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
- **Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input**

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

**Memory**

- **Option 150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen.1: x4 or x8; Gen 2: x4

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

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<th>Description</th>
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<tr>
<td>71630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - XMC</td>
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<tr>
<td>-002* -2 FPGA speed grade</td>
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<tr>
<td>-062 XC6VLX240T FPGA</td>
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<td>-105 Gigabit serial FPGA I/O through P16 connector</td>
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<tr>
<td>-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)</td>
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<tr>
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<td>*This option is always required</td>
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**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Model 8266**

PC Development System

See 8266 Datasheet for Options

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Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
General Information

Model 71640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71640 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols. 

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multimodule synchronization
- PCI Express Gen. 2 interface x8 wide
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O


A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 71640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 71640s can be synchronized using the Cobalt high speed sync module to drive the sync bus.

Memory Resources

The 71640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71640 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 5 GHz bit clock. With dual XMC connectors, the 71640 supports x8 PCIe on the first XMC connector leaving the optional second connector free to support user-installed transfer protocols specific to the target application.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
- Type: Texas Instruments ADC12D1800
- Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- Resolution: 12 bits
- Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- Full Scale Input: +2 dBm to +4 dBm, programmable
- Sample Clock Sources: Front panel SSMC connector
- Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
- Type: Front panel female SSMC connector, TTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size
- Standard XMC module, 2.91 in. x 5.87 in.

Model 81640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC

PCI Express Interface

The Model 71640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The 8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

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<td>71640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC</td>
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Options:
- -002* -2 FPGA speed grade
- -062 XC6VLX240T
- -064 XC6VSX315T
- -104 LVDS FPGA I/O through P14 connector
- -105 Gigabit serial FPGA I/O through P16 connector
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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<tr>
<td>8266</td>
<td>PC Development System</td>
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See 8266 Datasheet for Options
General Information

Model 71641 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, Model 71641 includes an optional connection to the Virtex-6 FPGA for custom I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤
A/D Acquisition IP Module

The 71641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Clocking and Synchronization

The 71641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 71641’s can be synchronized with a simple cable. For larger systems, multiple 71641’s can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

Memory Resources

The 71641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

Clocking and Synchronization

The 71641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 71641’s can be synchronized with a simple cable. For larger systems, multiple 71641’s can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

Memory Resources

The 71641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - XMC

PCI Express Interface
The Model 71641 complies with the VITA 42.3 XMC specification and includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector
Sync Bus: Multipin front panel connector, includes gate, reset, and in and out ref clock
External Trigger Input
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include trigger and gate
Field Programmable Gate Array:
Xilinx Virtex-6 XC6VSX315T-2
Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model Description
71641 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-6 FPGA - XMC
Options:
-002* -2 FPGA speed grade
-064* XC6VSX315T
-104 LVDS FPGA I/O through P14 connector
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8266 PC Development System
See 8266 Datasheet for Options
General Information

Model 71650 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71650 includes optional general-purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multichannel synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
A/D Acquisition IP Modules

The 71650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 71650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building systems by providing a complete development environment. The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building systems by providing a complete development environment.

XMC Interface

The Model 71650 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71650 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VLX315T-2

Custom I/O

- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

- PCI Express Bus: Gen.1 or Gen.2, x4 or x8

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 71651 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71651 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

A/D Acquisition IP Modules

The 71651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \cdot f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Core

In addition to the DDCs, the 71651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71651’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71651's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71651 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71651 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple modules.

PCI Express Interface

The Model 71651 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tr>
<th>Model</th>
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<tbody>
<tr>
<td>71651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC</td>
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</tbody>
</table>

Options:

- **-002**: -2 FPGA speed grade
- **-014**: 400 MHz, 14-bit A/Ds
- **-062**: XC6VLX240T FPGA
- **-064**: XC6VSX315T FPGA
- **-104**: LVDS FPGA I/O through P14 connector
- **-150**: Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-155**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Model 8266

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - XMC

Specifications

**Front Panel Analog Signal Inputs**
- **Input Type**: Transformer-coupled, front panel female SSMS connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: ±5 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters (standard)**
- **Type**: Texas Instruments ADS5463
- **Sampling Rate**: 20 MHz to 500 MHz
- **Resolution**: 12 bits

**A/D Converters (option -014)**
- **Type**: Texas Instruments ADS5474
- **Sampling Rate**: 20 MHz to 400 MHz
- **Resolution**: 14 bits

Digital Downconverters
- **Quantity**: Two channels
- **Decimation Range**: 2x to 131,072x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \)
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type**: Texas Instruments DAC5688
- **Input Data Rate**: 250 MHz max.
- **Output IF**: DC to 400 MHz max.
- **Output Signal**: 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate**: 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution**: 16 bits

DigitalInterpolator
- **Interpolation Range**: 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation**: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain**: One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients**: I & Q with 16-bit resolution
- **Gain Coefficients**: 16-bit resolution
- **Channel Summation**: 24-bit
- **Multiboard Summation Expansion**: 32-bit

Front Panel Analog Signal Outputs
- **Output**: Transformer-coupled, front panel female SSMS connectors
- **Transformer**: Coil Craft WBC4-6TLB
- **Full Scale Output**: ±4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type**: Front panel female SSMS connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard**: Xilinx Virtex-6 XC6VLX240T-2
- **Optional**: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104**: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
- **Option -150**: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option -155 or -165**: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus**: Gen. 2: x4 or x8

Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information
Model 71660 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Virtex-6 FPGA
LX130T, LX240T or SX315T

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71660 ➤
Model 71660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>71660</td>
<td>4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC</td>
</tr>
</tbody>
</table>

Options:

-062  XC6VLX240T FPGA
-064  XC6VSX315T FPGA
-104  LVDS FPGA I/O through P14 connector
-105  Gigabit serial FPGA I/O through P16 connector
-150  Two 8 MB QDR II+ SRAM Memory Banks (Banks 1 and 2)
-160  Two 8 MB QDR II+ SRAM Memory Banks (Banks 3 and 4)
-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- **Type:** Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

PC Development System

See 8266 Datasheet for Options

Pentek, Inc.  One Park Way  ●  Upper Saddle River  ●  New Jersey 07458
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com  www.pentek.com
General Information

Model 71661 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71661 includes a general purpose connector to the Virtex-6 FPGA for custom I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.
A/D Acquisition IP Modules

The 71661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Core

In addition to the DDCs, the 71661 features a complete beamforming subsystem. Each DDC core contains a programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.
### XMC Interface

The Model 71661 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71661 supports 8x PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beam-forming across multiple boards.

### Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building a development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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#### Options:

- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS FPGA I/O
- **-150** Two 8 MB QDRII+ SRAM Banks (Banks 1 and 2)
- **-160** Two 8 MB QDRII+ SRAM Banks (Banks 3 and 4)
- **-155** Two 512 MB DDR3 SDRAM Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Banks (Banks 3 and 4)

#### Contact Pentek for availability of rugged and conduction-cooled versions

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See 8266 Datasheet for Options

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### 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - XMC

- A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

- Multiple 71661’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

### Memory Resources

The 71661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

### PCI Express Interface

The Model 71661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

### Specifications

#### Front Panel Analog Signal Inputs

- **Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** ±8 dBm into 50 ohms
- **3 dB Bandpass:** 300 kHz to 700 MHz

#### A/D Converters

- **Type:** Texas Instruments AD55485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

#### Digital Downconverters

- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user programmable coefficients

- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

#### Beamformer

- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

#### Sample Clock Sources:

- On-board clock synthesizer

#### Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

#### External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

#### Timing Bus:

- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

#### Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

#### Custom I/O

- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

#### Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

#### PCI-Express Interface

- **PCI Express Bus:** Gen. 1: x4 or x8;
  Gen. 2: x4

#### Environmental

- **Operating Temp.:** 0° to 50° C
- **Storage Temp.:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard XMC module, 2.91 in. x 5.87 in.

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Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  www.pentek.com

Contact Pentek for availability of rugged and conduction-cooled versions.
Model 71662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

General Information

Model 71662 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of communications or radar systems. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 71662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable serial gigabit interfaces
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Acquisition IP Modules**

The 71662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s \)/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of \( f_s \)/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other modules.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.
Model 71662

Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71662 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71662 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters

- Quantity: Four 8-channel banks, one per acquisition module
- Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description

8266 PC Development System

See 8266 Datasheet for Options

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

Ordering Information

Model 71662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - XMC

Options:
- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS FPGA I/O through P14 connector
- 105 Gigabit serial FPGA I/O through P16 connector
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Ordering Information

Model 8266

PC Development System

See 8266 Datasheet for Options

Contact Pentek for availability of rugged and conduction-cooled versions

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.
**General Information**

Model 71663 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 71663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**GSM Channelizer Cores**

The 71663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 71663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 71663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz/13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across PCIe. There are four superchannel mask words, one for each bank.

**Superchannel Packets and Headers**

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

**PCI Express Interface**

The Model 71663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 71663 and host.
Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 71663
1100-Channel GSM Channelizer with Quad A/D - XMC

Specifications

Front Panel Analog Signal Inputs
• Input Type: Transformer-coupled, front panel female SSMC connectors
• Transformer Type: Coil Craft WBC4-6TLB
• Full Scale Input: +8 dBm into 50 ohms
• 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
• Type: Texas Instruments ADS5485
• Sampling Rate: 10 MHz to 200 MHz
• Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
• Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
• Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
• Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
• Type: Front panel female SSMC connector, LVTTTL
• Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
• DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
• Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks

DDC Channels
• Channel Spacing: 200 kHz, fixed
• DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
• < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
• > 18 dB attenuation at ±100 kHz
• > 78 dB attenuation at ±170 kHz
• > 83 dB attenuation at ±600 kHz
• > 93 dB attenuation at ±800 kHz
• > 96 dB attenuation at > ±3 MHz

DDC Output Rate \( f_s \); Resampled to 180 MHz\( \times 13/2160 = 1.0833333 \) MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
• Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
• Frequency Offsets for each DDC:
  - First: \(-f_s/4\) (-270.8333 kHz)
  - Second: 0 Hz
  - Third: \(+f_s/4\) (+270.8333 kHz)
  - Fourth: \(+f_s/2\) (+541.666 kHz)
• Superchannel Sample Rate: \( f_s \)
• Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
• PCI Express Bus: Gen. 2 x8

Environmental
• Operating Temp: 0° to 50° C
• Storage Temp: -20° to 90° C
• Relative Humidity: 0 to 95%, non-cond.
• Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

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Contact Pentek for availability of rugged and conduction-cooled versions
Model 71664

4-Ch. 200 MHz A/D w. DDCs, VITA-49.0, Virtex-6 FPGA - XMC

General Information

Model 71664 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 71664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71664 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX315 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules

The 71664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \(f_s\), where \(f_s\) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536, providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8\(f_s\)/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \(f_s\)/N.

Beamformer IP Core

In addition to the DDCs, the 71664 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71664s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

This allows summation across channels on multiple boards.

**VITA 49.0**

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey timestamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 71664 supports fully the VITA 49.0 specification.
Model 71664

4-Ch. 200 MHz A/D w. DDCs, VITA-49.0, Virtex-6 FPGA - XMC

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71664’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 71664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**XMC Interface**

The Model 71664 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71664 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple boards.
Model 8266

The Model 8266 is a PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8266

Ordering Information

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<td>71664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA-49.0 and Virtex-6 FPGA - XMC</td>
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</tbody>
</table>

Options:

-062  XC6VLX240T
-064  XC6VSX315T
-104  LVDS FPGA I/O
-150  Two 8 MB QDRII+ SRAM Banks (Banks 1 and 2)
-160  Two 8 MB QDRII+ SRAM Banks (Banks 3 and 4)
-155  Two 512 MB DDR3 SDRAM Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model 71664

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters

- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to ƒs
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer

- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O

- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 71670 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel μSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71670 μSync connectors enabling multiple 71670 channels synchronous configurations.

Memory Resources

The 71670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71670 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71670 supports 8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

D/A Converters
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max.
with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs
Quantity: Four D/A outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Ordering Information

Model Description
71670 4-Channel 1.25 GHz D/A with Virtex-6 FPGA - XMC

Options:
-002* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8266 PC Development System

See 8266 Datasheet for Options
Model 71671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC

General Information

Model 71671 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SX6 FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multichannel synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverting and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a waveform, real or complex, and delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a waveform of length 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is provided through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 71671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - XMC

Model 71671

The Model 71671 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71671 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

**XMC Interface**

The Model 71671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specfications**

- **D/A Converters**
  - **Type:** TI DAC3484
  - **Input Data Rate:** 312.5 MHz max.
  - **Output Bandwidth:** 250 MHz max.
  - **Output Sampling Rate:** 1.25 GHz max. with interpolation
  - **Interpolation:** 2x, 4x, 8x or 16x
  - **Resolution:** 16 bits

- **Digital Interpolator**
  - **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

- **Front Panel Analog Signal Outputs**
  - **Quantity:** Four D/A outputs
  - **Output Type:** Transformer-coupled, front panel female SSMC connectors
  - **Full Scale Output:** Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
  - **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
  - **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

- **External Clock**
  - **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

- **External Trigger Input**
  - **Type:** Front panel female SSMC connector
  - **Function:** Programmable functions include: trigger, gate, sync and PPS

- **Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

- **Field Programmable Gate Array:**
  - **Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2**

- **Custom I/O**
  - **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
  - **Option -105:** Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

- **Memory**
  - **Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR**

- **PCI-Express Interface**
  - **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8

- **Environmental**
  - **Operating Temp:** 0° to 50°C
  - **Storage Temp:** -20° to 90°C
  - **Relative Humidity:** 0 to 95%, non-cond.
  - **Size:** Standard XMC module, 2.91 in. x 5.87 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through P14 connector
- **-105** Gigabit serial FPGA I/O through P 16 connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

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Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
Model 71690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

General Information

Model 71690 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71690 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds digitize the I + Q signals synchronously
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multinode synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**A/D Clocking and Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

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**A/D Acquisition IP Modules**

The 71690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Model 8266

The Model 8266 is a fully-integrated board system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was designed to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 71690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

➤ Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA.

XMC Interface

The Model 71690 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71690 supports x8 PCIe on the first XMC connector leaving x8 PCIe on the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiplexed DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Input

- Connector: Front panel female SSMC
- Impedance: 50 ohms

L-Band Tuner

- Type: Maxim MAX2112
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer:
  - freqVCO = (N.F) x freqREF
  - Where integer N = 19 to 251 and fractional F is a 20-bit binary value
  - PLL Reference (freqREF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter
- Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps
- *Usable Full-Scale Input Range: -50 dBm to +10 dBm
- Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters

- Type: Texas Instruments AD55485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources

- On-board timing generator/synthesizer

A/D Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus

- 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Quantity: 2
- Type: Front panel female SSMC connector, 50 ohms
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.
Model 71720
3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - XMC

General Information
Model 71720 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71720 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.  

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched-fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
**Model 71720**

**A/D Acquisition IP Modules**

The 71720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 71720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either onboard memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-Pcie configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s Pcie interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or routing to other module resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.
Model 71720

Memory Resources

The 71720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description

- Option -105: Gigabit serial FPGA I/O
- Option -104: LVDS FPGA I/O through P16 connector
- Option -076: XC7VX690T-2 FPGA
- Option -073: XC7VX330T-2 FPGA

Ordering Information

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Options:

- Option -073: XC7VX330T-2 FPGA
- Option -076: XC7VX690T-2 FPGA
- Option -104: LVDS FPGA I/O through P14 connector
- Option -105: Gigabit serial FPGA I/O through P 16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

Memory Resources

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description

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D/A Converters

| Type: Texas Instruments DAC5688 |
| Input Data Rate: 250 MHz max. |
| Output IF: DC to 400 MHz max. |
| Output Signal: 2-channel real or 1-channel with frequency translation |
| Output Sampling Rate: 800 MHz max. with interpolation |
| Resolution: 16 bits |

Front Panel Analog Signal Outputs

| Output Type: Transformer-coupled, front panel female SSMC connectors |
| Transformer Type: Coil Craft WBC4-6TLB |
| Full Scale Output: +4 dBm into 50 ohms |
| 3 dB Passband: 300 kHz to 700 MHz |

Sample Clock Sources

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

PCI Express Interface

| The Model 71720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. |
| Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA |
| Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA |

Contact Pentek for availability of rugged and conduction-cooled versions

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Specifications

Front Panel Analog Signal Inputs

| Input Type: Transformer-coupled, front panel female SSMC connectors |
| Transformer Type: Coil Craft WBC4-6TLB |
| Full Scale Input: +8 dBm into 50 ohms |
| 3 dB Passband: 300 kHz to 700 MHz |

A/D Converters

| Type: Texas Instruments ADS5485 |
| Sampling Rate: 10 MHz to 200 MHz |
| Resolution: 16 bits |

Environmental

| Operating Temp: 0° to 50° C |
| Storage Temp: -20° to 90° C |
| Relative Humidity: 0 to 95%, non-cond. |

Contact Pentek for availability of rugged and conduction-cooled versions

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Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

**General Information**

Model 71721 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/A and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71721 includes an optional connection to the Virtex-7 FPGA for custom I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelizing of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules

The 71721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

Beamformer IP Core

In addition to the DDCs, the 71721 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71721’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 71721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

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3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized in the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71721’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.
XMC Interface
The Model 71721 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8x link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71721 supports 8 PCIe lanes on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple modules.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model Description
71721 3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - XMC

Options:
- 076 XC7VX690T-2 FPGA
- 104 LVDS FPGA I/O through P14 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
PC Development System
See 8266 Datasheet for Options

Memory Resources
The 71721 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 71721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f, LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 71730 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71730 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interface. The 71730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
**A/D Acquisition IP Module**

The 71730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 71730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ **GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply resets to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture, or for routing to other module resources.

**D/A Converter Stage**

The 71730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GS/sec, allowing it to accept full-rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
Model 71730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - XMC

XMC Interface

The Model 71730 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71730 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<th>Description</th>
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<td>Options:</td>
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<td>XC7VX330T-2 FPGA</td>
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<td>-105</td>
<td>Gigabit serial FPGA I/O through P16 connector</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

PC Development System See 8266 Datasheet for Options

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 71730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.
Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

General Information
Model 71741 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features
- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- μSync clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
**A/D Acquisition IP Module**

The 71741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate and executing on the host computer and loaded through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel IP core, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.
**Model 71741**

**Memory Resources**

The 71741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>71741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC</td>
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</table>

**Options:**

- 073  XC7VX330T-2 FPGA
- 076  XC7VX690T-2 FPGA
- 104  LVDS FPGA I/O through P14 connector
- 105  Gigabit serial FPGA I/O through P16 connector

**Contact Pentek for availability of rugged and conduction-cooled versions**

**A/D Converter**

Type: Texas Instruments ADC12D1800

**Sampling Rate:**

- Single-channel mode: 500 MHz to 3.6 GHz
- Dual-channel mode: 150 MHz to 1.8 GHz

**Resolution:**

12 bits

**Input Bandwidth:**

- Single-channel mode: 1.75 GHz
- Dual-channel mode: 2.8 GHz

**Full Scale Input:**

- +2 dBm to +4 dBm, programmable

**Digital Downconverters**

- **Modes:** One or two channels, programmable
- **Supported Sample Rate:**
  - Single-channel mode: 3.6 GHz
  - Two-channel mode: 1.8 GHz

**Clocking and Synchronization**

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

**PCI Express Interface**

The Model 71741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Clocking and Synchronization**

The 71741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71741’s can be synchronized with a simple cable. For larger systems, multiple 71741’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

General Information

Model 71751 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connections to communications or radar systems. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71751 includes a general purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71751 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48A1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**A/D Acquisition IP Modules**

The 71751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

**D/A Waveform Playback IP Module**

The Model 71751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Oryx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reconfiguring the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course...
of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71751’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71751 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71751 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming access across multiple modules.

PCI Express Interface

The Model 71751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option -014)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- LO Tuning Freq. Resolution: 32 bits, 0 to fs
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
- Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz
- Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus
- Type: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model Description
71751 2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - XMC

Options:
- 014 400 MHz, 14-bit A/Ds
- 076 XC7VX690T-2 FPGA
- 104 LVDS FPGA I/O through P14 connector
- 105 Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 71760 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.
A/D Acquisition IP Modules

The 71760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 8266**

The Model 8266 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

**Memory**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
- **Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs**

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard XMC module, 2.91 in. x 5.87 in.
4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC

Model 71761

General Information

Model 71761 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71761 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 71761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
**A/D Acquisition IP Modules**

The 71761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**Beamformer IP Core**

In addition to the DDCs, the 71761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71761’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple modules.

➤ **GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from ➤.
FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71761 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71761 supports x8 PCIe on the first XMC connector. The second connector is used for the Aurora interface and provides a dedicated board-to-board interface for beamforming across multiple modules.
Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Channel Summation: 24-bit

Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model 71761
- **Description:** 4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - XMC

Options:
- **-076** XC7VX690T-2 FPGA
- **-104** LVDS FPGA I/O through P14 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
- **Description:** PC Development System
- **See 8266 Datasheet for Options**
General Information

Model 71791 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 71791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 71791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS to match the specific requirements of external custom I/O connections to the FPGA.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.
A/D Acquisition IP Modules

The 71791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where capture is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 for most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converters and DDCs**

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

**A/D Clocking & Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

**PCI Express Interface**

The Model 71791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - XMC

Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuner
Type: Maxim MAX2121
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
\[ \text{freq}_{\text{VCO}} = (N \times \text{freq}_{\text{REF}}) \]
where integer \( N \) = 19 to 251 and fractional \( F \) is a 20-bit binary value
PLL Reference (freq_{REF}): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters
Type: Texas Instruments ADS5463
Sampling Rate: 10 MHz to 500 MHz
Resolution: 12 bits
Option -014: 400 MHz, 14-bit A/Ds
Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Quantity: 2
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3*: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCIe boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 71791

Ordering Information

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<td>L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - XMC</td>
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Options:
- 014 400 MHz, 14-bit A/Ds
- 076 XCVX690T-2 FPGA
- 100 27 MHz crystal for MAX2121
- 104 LVDS FPGA I/O through P14 connector
- 105 Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
PCIe Development System
See 8266 Datasheet for Options

* Gen 3 requires a compatible backplane and SBC
General Information

Model 71131 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71131 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through.
Model 71131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

A/D Acquisition IP Modules

The 71131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with eight full duplex gigabit links to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three additional modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, the Model 7893 System Synchronizer supports additional modules in increments of eight.

Memory Resources

The 71311 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 71131 includes an industry-standard interface fully compliant with PCI.
Model 71131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

➤ Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface
The Model 71131 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71131 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >108 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female MMCX connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: −20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: −20° to 65° C
Storage Temp: −40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: −40° to 70° C
Storage Temp: −50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information
Model  Description
71131  8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC
Options:
-084  XCKU060-2 FPGA
-087  XCKU115-2 FPGA
-104  LVDS FPGA I/O through P14 connector
-105  Gigabit serial FPGA I/O through P16 connector
-702  Air cooled, Level L2
-713  Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions
Model 71132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

General Information
Model 71132 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.

Features
- Complete radar and software radio interface solution
- Supports Powerful Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \(0.8f_s/N\), where \(N\) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC60 delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O. Option -105 installs the P16 XMC connector with eight full duplex gigabit links to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCMX connectors with transformer coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCMX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCMX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Up to three additional modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. For larger systems, the Model 7893 System Synchronizer supports additional modules in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications.
Model 71132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

PCI Express Interface

The Model 71132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2, and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71132 complies with the VITA 42.0 XMC specification. A connector provides a single 8x link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71132 supports x8 PCIe on the first XMC connector leaving the second free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female MMCX connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Wideband Digital Downconverters
- Quantity: Eight channels
- Decimation Range: 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: $>120$ dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, $<0.3$ dB passband ripple, $>100$ dB stopband attenuation

Multiband Digital Downconverters
- Quantity: Eight banks, 8 channels per bank
- Decimation Range: 16x to 1024x in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$, independent tuning for each channel
- LO SFDR: $>120$ dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, $<0.3$ dB passband ripple, $>100$ dB stopband attenuation
- Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female MMCX connector, sine wave, 0 to $+10$ dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus
- 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female MMCX connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0°C to 50°C
  - Storage Temp: -20°C to 90°C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20°C to 65°C
  - Storage Temp: -40°C to 100°C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (condenser cooled)
  - Operating Temp: -40°C to 70°C
  - Storage Temp: -50°C to 100°C
  - Relative Humidity: 0 to 95%, non-condensing
- Size: XMC module 2.910 in x 5.870 in
  (74.00 mm x 149.00 mm)

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

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<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>71132</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC</td>
</tr>
</tbody>
</table>

Options:
- -084 XCKU060-2 FPGA
- -087 XCKU115-2 FPGA
- -104 LVDS FPGA I/O through P14 connector
- -105 Gigabit serial FPGA I/O through P16 connector
- -702 Air cooled, Level L2
- -713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions
General Information

Model 71141 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/A and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KL035 through KU115. The KU115 features 5520 DSP48E2 slices.
Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

A/D Acquisition IP Module
The 7141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module
The Model 71141 factory installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.
Option -105 installs the P16 XMC connector with 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage
A TTI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources
The 7141 architecture supports a 5 GB bank of DDR4 SDRAM memory.
User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface
The Model 7141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization
The 7141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.
A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7192 high-speed sync module can be used to drive the sync bus to synchronize multichannel systems.
**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converter**
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

**D/A Converters**
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

**Sample Clock Source:** Front panel SSMC connector

**Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105 (only available with option -084 or -087):** Installs the XMC P16 connector configurable as one 8X gigabit serial link to the FPGA

**Memory**
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**
- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp:** -40° to 70° C
  - **Storage Temp:** -50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

**Size:** XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
### General Information

Model 71821 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

### The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

The 71821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 71821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

### Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.
The Model 71821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_u$ where $f_u$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_u / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_u / N$.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the P16 XMC connector to support serial protocols.

### A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

### Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

![Diagram](https://via.placeholder.com/150)

**Model 71821**

**3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC**

**A/D Acquisition IP Modules**

The 71821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_u$ where $f_u$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_u / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_u / N$.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the P16 XMC connector to support serial protocols.

### A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

### Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.
When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71821’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

XMC Interface

The Model 71821 complies with the VITA 42.0 XMC specification. Each of two connectors provides a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71821 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +5 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters**
- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

**Digital Downconverters**
- **Quantity**: Two channels
- **Decimation Range**: 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to f_s
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**
- **Type**: Texas Instruments DAC5688
- **Input Data Rate**: 250 MHz max.
- **Output IF**: DC to 400 MHz max.
- **Output Signal**: 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate**: 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution**: 16 bits

**Digital Interpolator Core**
- **Interpolation Range**: 2x to 32,768x in three stages of 2x to 32x
- **Total Interpolation Range (D/A and interpolator core combined)**: 2x to 262,144x

**Front Panel Analog Signal Outputs**
- **Output**: Transformer-coupled, front panel female SSMC connectors
- **Transformer**: Coil Craft WBC4-6TLB
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**Sample Clock Sources**
- **On-board clock synthesizer generates two clocks**: one A/D clock and one D/A clock

**Clock Synthesizer**
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization**
- **VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz**

**Clock Dividers**
- **External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock**

**External Clock**
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus**
- **26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate(trigger and sync/PPS inputs**

**Field Programmable Gate Array**
- **Standard**: Xilinx Kintex UltraScale XCKU035-2
- **Option -084**: Xilinx Kintex UltraScale XCKU060-2
- **Option -087**: Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104**: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105**: Provides one 8X gigabit link between the FPGA and XMC P16 connector to support serial protocols.

**Memory**
- **Type**: DDR4 SDRAM
- **Size**: 5 GB
- **Speed**: 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8

**Environmental**
- **Standard**: L0 (air cooled)
- **Operating Temp**: 0° to 50°C
- **Storage Temp**: -20° to 90°C
- **Relative Humidity**: 0 to 95%, non-condensing

- **Option -072**: L2 (air cooled)
- **Operating Temp**: -20° to 65°C
- **Storage Temp**: -40° to 100°C
- **Relative Humidity**: 0 to 95%, non-condensing

- **Option -073**: L3 (condensation cooled)
- **Operating Temp**: -40° to 70°C
- **Storage Temp**: -50° to 100°C
- **Relative Humidity**: 0 to 95%, non-condensing

**Size**: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)
Model 71841 is a member of the Jade family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - XMC

**D/AD Acquisition IP Module**

The 71841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \(0.8 \times f_s/N\), where \(N\) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.
Model 71841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - XMC

Memory Resources

The 71861 architecture supports a 5 GB bank of DDR4 SDRAM memory.
User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 71841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 71841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.
A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71841’s can be synchronized with a simple cable. For larger systems, multiple 71841’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: May be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters

Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: Decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: Decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: The DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X gigabit serial link to the FPGA

Memory

Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)
Operating Temp: 0° to 50°C
Storage Temp: –20° to 90°C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65°C
Storage Temp: –40° to 100°C
Relative Humidity: 0 to 95%, non-condensing

Environment

Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70°C
Storage Temp: –50° to 100°C
Relative Humidity: 0 to 95%, non-condensing
Size: Standard XMC module, 2.91 in. x 5.87 in.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
General Information

Model 71851 is a member of the Jade family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 71851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 71851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multinode synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 71851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator. Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*$f_s$/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s$/N.

D/A Waveform Playback IP Module

The Model 71851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the P16 XMC connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.
Model 71851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - XMC

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

XMC Interface

The Model 71851 complies with the VITA 42.0 XMC specification. Each of two connectors provide a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71851 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

PCI Express Interface

The Model 71851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz
- **A/D Converters (standard)**
  - **Type:** Texas Instruments ADS5463
  - **Sampling Rate:** 20 MHz to 500 MHz
  - **Resolution:** 12 bits
- **A/D Converters (option -014)**
  - **Type:** Texas Instruments ADS5474
  - **Sampling Rate:** 20 MHz to 400 MHz
  - **Resolution:** 14 bits
- **Digital Downconverters**
  - **Quantity:** Two channels
  - **Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
  - **LO TuningFreq. Resolution:** 32 bits, 0 to $f_s$
  - **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **D/A Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Signal:** 2-channel real or 1-channel with frequency translation
  - **Output Sampling Rate:** 800 MHz max.
  - **Resolution:** 16 bits
- **Digital Interpolator Core**
  - **Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
- **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x
- **Front Panel Analog Signal Outputs**
  - **Output:** Transformer-coupled, front panel female SSMC connectors
  - **Transformer:** Coil Craft WBC4-6TLB
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Array**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105:** Provides one 8X gigabit link between the FPGA and XMC P16 connector to support serial protocols

**Memory**
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**
- **Standard:** L0 (air cooled)
  - **Operating Temp.:** 0° to 50° C
  - **Storage Temp.:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp.:** -20° to 65° C
  - **Storage Temp.:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp.:** -40° to 70° C
  - **Storage Temp.:** -50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

**Size:** XMC module 2,910 in x 5,870 in (73.91 mm x 149.10 mm)
Model 71861

General Information

Model 71861 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
**A/D Acquisition IP Modules**

The 71861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s \)/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s \)/N.

**Xilinx Kintex UltraScale FPGA**

The Xilinx Kintex UltraScale FPGA can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X gigabit link to the FPGA to support serial protocols.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

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**Diagram**

[Diagram of the 4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC]
Model 71861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped for a development system. Each platform includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71861 complies with the VITA 42.0 XMC specification. Each of two connectors provide a single 8x link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71861 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +8 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

A/D Converters

- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

Digital Downconverters

- **Quantity**: Four channels
- **Decimation Range**: 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to f_s
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources:

- **Clock Source**: On-board clock synthesizer

Clock Synthesizer

- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers:

- **External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock**

External Clock

- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

- **26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs**

External Trigger Input

- **Type**: Front panel female SSMC connector, LVTTL

Function:

- **Programmable functions include: trigger, gate, and sync and PPS**

Field Programmable Gate Array

- **Standard**: Xilinx Kintex UltraScale XCKU035-2
- **Option -084**: Xilinx Kintex UltraScale XCKU060-2
- **Option -087**: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- **Option -010**: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -015**: Installs the XMC P16 connector with one 8X gigabit serial link to the FPGA

Memory

- **Type**: DDR4 SDRAM
- **Size**: 5 GB
- **Speed**: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8

Environmental

- **Standard**: L0 (air cooled)
  - **Operating Temp**: 0°C to 50°C
  - **Storage Temp**: -20°C to 90°C
  - **Relative Humidity**: 0 to 95%, non-condensing
- **Option -070**: L2 (air cooled)
  - **Operating Temp**: -20°C to 65°C
  - **Storage Temp**: -40°C to 100°C
  - **Relative Humidity**: 0 to 95%, non-condensing
- **Option -073**: L3 (conduction cooled)
  - **Operating Temp**: -40°C to 70°C
  - **Storage Temp**: -50°C to 100°C
  - **Relative Humidity**: 0 to 95%, non-condensing

Size:

- **XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)**

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

 Pentek, Inc. One Park Way ▪ Upper Saddle River ▪ New Jersey 07458
Tel: 201-818-5900 ▪ Fax: 201-818-5904 ▪ Email: info@pentek.com
www.pentek.com
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

General Information

Model 71862 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new stream-lined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.
**A/D Acquisition IP Modules**

The 71862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a linked definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

- **Within each A/D Acquisition IP Module are two powerful DDC IP cores.** A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

- **Each wideband DDC has an independent 32-bit tuning frequency setting** that ranges from DC to f_s where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

- **Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting** that ranges from DC to f_s where f_s is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

- **The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients.** The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

- **Option-104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.**

- **Option-105 installs the P16 XMC connector with one 8X gigabit link to the FPGA to support serial protocols.**

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front-panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple modules can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 71862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

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**Model 71862**

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

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Pentek, Inc.  One Park Way  ●  Upper Saddle River  ●  New Jersey 07458
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com

www.pentek.com
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Model 71862

PCI Express Interface

The Model 71862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

XMC Interface

The Model 71862 complies with the VITA 42.0 XMC specification. Each of two connectors provides a single 8x link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71862 supports 8x PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Wideband Digital Downconverters

- Quantity: Four channels
- Decimation Range: 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters

- Quantity: Four banks, 8 channels per bank
- Decimation Range: 2x to 1024x
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s, independent tuning for each channel
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector with one 8x gigabit serial link to the FPGA

Memory

- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0% to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0% to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0% to 95%, non-condensing

Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Ordering Information

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<td>4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - XMC</td>
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Options:

- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O through P14 connector
- 105 Gigabit serial FPGA I/O through P16 connector
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
General Information

Model 71800 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The 71800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with an 8X gigabit link to the FPGA to support serial protocols.

Front Panel Digital I/O Interface

The 71800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Features

- Hi-performance co-processor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
PCI Express Interface

The Model 71800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

XMC Interface

The Model 71800 complies with the VITA 42.0 XMC specification. Each of two connectors provides an 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71800 supports x8 PCIe on the first XMC connector leaving the second one free to support user-installed transfer protocols specific to the target application.

Specifications

Front Panel Digital I/O

- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

Field Programmable Gate Array

- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Memory Resources

The 71800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Memory

- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -702:** L2 (air cooled)
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** -40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -713:** L3 (conduction cooled)
- **Operating Temp:** -40° to 70° C
- **Storage Temp:** -50° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Size:** XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Ordering Information

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</table>

**Options:**

- **084** XCKU060-2 FPGA
- **087** XCKU115-2 FPGA
- **104** LVDS FPGA I/O through P14 connector
- **105** Gigabit serial FPGA I/O through P16 connector
- **702** Air cooled, Level L2
- **713** Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
General Information

The Bandit® Model 7120 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PMC/XMC module with front-panel connectors for easy integration into RF systems, the module offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7120 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 7120 accepts RF signals on two front-panel SSMS connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 7120 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 7120 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 7120 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤
### Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC

#### Specifications

**RF Input**
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** -60 dBm to -20 dBm
- **Flatness:** ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- **RF Attenuator:** Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

**Phase Noise**
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- **Connector Type:** SSMC
- **Input/Output Impedance:** 50 ohms

**Reference Input Signal**
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

**Reference Output Signal**
- **Frequency:** 10 MHz
- **Level:** 0 dBm, sine wave

**OCXO Reference**
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm

**Aging**
- **Daily:** ±10 ppb/day
- **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 KHz Offset: –148 dBc/Hz
- 10 KHz Offset: –154 dBc/Hz
- 100 KHz Offset: –155 dBc/Hz

**IF Output**
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

**Programming**
- **Functions:** RF Atten, IF Atten, Int/Ext
- **Reference Select, LO Synthesizer Frequency Interface:** USB
- **Connector Type:** MicroUSB

**Power**
- **Voltage:** +12 VDC
- **Current:** 1.5 A

**PMC/XMC Interface:** Power only on PMC P11 (option -104) or XMC P15 (option -105)

**Size:** Standard PMC module, 2.91 in. x 5.87 in.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<td>7120</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC</td>
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<table>
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<th>Option</th>
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<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
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<tr>
<td>-104</td>
<td>PMC P11 Power</td>
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<tr>
<td>-105</td>
<td>XMC P15 Power</td>
</tr>
<tr>
<td>-106</td>
<td>PCIe 6-pin connector (Power only)</td>
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<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
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<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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<tr>
<td>MODEL</td>
<td>DESCRIPTION</td>
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<tr>
<td>Cobalt 72620, 73620, 74620</td>
<td>3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Cobalt 72621, 73621, 74621</td>
<td>3/6-Ch 200 MHz A/D, DDCs, DUC, 2/4-Ch. 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
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<td>Cobalt 72624, 73624, 74624</td>
<td>1-Ch 1 GHz A/D and 1-2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Cobalt 72630, 73630, 74630</td>
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<tr>
<td>Cobalt 72640, 73640, 74640</td>
<td>12/8-Channel 200 MHz A/D with DDCs, Beamformer and Virtex-6 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Cobalt 72660, 73660, 74660</td>
<td>4/8-Channel 200 MHz A/D with DDcs, Wideband DDC, Virtex-6 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Cobalt 72670, 73670, 74670</td>
<td>1/2-Ch 1.25 GHz D/A with DUC, Extended Interpol. and Virtex-6 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Cobalt 72690, 73690, 74690</td>
<td>2-Ch 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
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<td>Onyx 72720, 73720, 74720</td>
<td>3-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Onyx 72730, 73730, 74730</td>
<td>1-Ch 1 GHz A/D and 1-/2-Ch 1 GHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
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<td>Onyx 72741, 73741, 74741</td>
<td>12-Bit and 2-Ch 1 GHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Onyx 72751, 73751, 74751</td>
<td>2-Ch 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Onyx 72760, 73760, 74760</td>
<td>4/8-Channel 200 MHz A/D with DDcs and Virtex-7 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Onyx 72761, 73761, 74761</td>
<td>4-Channels 200 MHz, 16-bit A/D with DDcs and Virtex-7 FPGA - 6U/3U cPCI</td>
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<tr>
<td>Jade 72131, 73131, 74131</td>
<td>L-Band RF Tuner, 2-Ch 200 MHz A/D, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72132, 73132, 74132</td>
<td>3-Ch 200 MHz A/D, DDC, DUC, 2-Ch 800 MHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72141, 73141, 74141</td>
<td>1-Ch 1 GHz A/D and 1-Ch 1 GHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72821, 73821, 74821</td>
<td>2-Ch 500 MHz A/D, DDC, DUC, 2-Ch 800 MHz D/A, Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72841, 73841, 74841</td>
<td>4-Channels 200 MHz, 16-bit A/D with DDcs and Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72851, 73851, 74851</td>
<td>8-Channels 250 MHz A/D with DDcs and Kintex UltraScale FPGA - 6U/3U cPCI</td>
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<tr>
<td>Jade 72861, 73861, 74861</td>
<td>3-Channels 200 MHz A/D, DDC, DUC 2-Ch 800 MHz D/A, Kintex FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72862, 73862, 74862</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Wideband DDC, Kintex FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Jade 72800, 73800, 74800</td>
<td>2-Ch 500 MHz A/D, DDC, DUC, 2-Ch 800 MHz D/A, Kintex FPGA - 6U/3U cPCI</td>
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<tr>
<td>Bandit 7220, 7320, 7420</td>
<td>4-Channels 200 MHz A/D with DDcs and Kintex UltraScale FPGA - 6U/3U cPCI</td>
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<tr>
<td></td>
<td>Kintex UltraScale FPGA Coprocessor - 3U/6U cPCI</td>
</tr>
<tr>
<td></td>
<td>Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI</td>
</tr>
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</table>

Customer Information
### General Information

Models 72620, 73620 and 74620 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71620 XMC modules mounted on a PCI carrier board.

Model 72620 is a 6U cPCI board while the Model 73620 is a 3U cPCI board; both are equipped with one Model 71620 XMC. Model 74620 is a 6U cPCI board with two XMC modules rather than one.

These models include three or six A/Ds, one or two DUCs, two or four D/As and four or eight banks of memory.

### The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solution, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73620; J3 connector, Model 72620; J3 and J5 connectors, Model 74620.

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

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**Block Diagram, Model 72620**

Model 74620 doubles all resources except the PCI-to-PCI Bridge

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**Models 72620, 73620 and 74620**

3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73620: 32 bits only.

Specifications

Model 72620 or Model 73620: 3 A/Ds, 1 DUC, 2 D/As
Model 74620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

D/A Converters (2 or 4)

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs (2 or 4)

Output Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthetizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73620; J3 connector, Model 72620; J3 and J5 connectors, Model 74620

Memory Banks (1 or 2)

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 72620: 32 bits only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board
**General Information**

Models 72621, 73621 and 74621 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71621 XMC modules mounted on a cPCI carrier board.

Model 72621 is a 6U cPCI board while the Model 73621 is a 3U cPCI board; both are equipped with one Model 71621 XMC. Model 74621 is a 6U cPCI board with two XMC modules rather than one.

These models include three or six A/Ds, three or six multiband DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX/T part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

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<td>Complete radar and software radio interface solution</td>
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<td>One or two multiboard programmable beamformers</td>
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<td>Sample clock synchronization to an external system reference</td>
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<td>LVPECL clock/sync bus for multiboard synchronization</td>
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</table>

**Block Diagram, Model 72621**

Model 74621 doubles all resources except the PCI to PCI Bridge.
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via the built-in Xilinx Aurora gigabit serial interfaces through the J3 and J5 connectors. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions include sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

D/A Waveform Playback IP Modules

Each module has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via the built-in Xilinx Aurora gigabit serial interfaces through the J3 and J5 connectors. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions include sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

D/A Waveform Playback IP Modules

Each module has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.
A/D Converter Stage
The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage
One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73621: 32 bits only.
Specifications

Model 72621 or Model 73621: 3 A/Ds, 3 DDCs, 1 DUC, 2 D/As
Model 74621: 6 A/Ds, 6 DDCs, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters (3 or 6)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolators (1 or 2)
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformers (1 or 2)
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via J3 connector using Aurora protocol; via J3 and J5 for Model 74621
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73621: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Options:
-062 XC6VLX240T
-064 XC6VSX315T
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI

General Information

Models 72624, 73624 and 74624 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71624 XMC modules mounted on a cPCI carrier board. Model 72624 is a 6U cPCI board while the Model 73624 is a 3U cPCI board; both are equipped with one Model 71624 XMC. Model 74624 is a 6U cPCI board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCI-X system interface supports control, status and data transfers.

Adaptive Relay Input Overview

These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCI-X system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCI-X to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The output stage of these models consists of 34 or 68 DUCs (digital upconverters) and two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals, and then delivers them to an I+Q DAC output. The DAC output stage of these models consists of two or four 200 MHz 16-bit D/A converters.
➤ signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the adaptive relay of these models. Because of the complexity and proprietary nature of these functions, the FPGAs cannot be extended or modified by the user.

A/D Converters

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 or 68 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8f_s/N$, where $N$ is the decimation setting and $f_s$ is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to -48 dB.

Receive DMA Controllers

Two or four output DMA engines deliver data across the PCI-X interface into user-specified memory locations in PCI-X target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs of the first XMC module. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of Model 74624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begin filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCI-X target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to -48 dB.
2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - cPCI

Digital Upconverters
The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to $f_s$, where $f_s$ is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks
Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters
One or two TI DAC5688 dual-channel D/As accept the summed upconverted data streams, one from each summation block, and operate in their non-translating dual, real baseband mode. Their built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

Clocking and Synchronization
Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from one or two on-board programmable VCXOs (voltage-controlled crystal oscillators). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73624: 32 bits only.

Form Factor Adaptors
All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.
Specifications

Models 72624 & 73624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As
Model 74624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Quantity: 2 or 4
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: 34 or 68
Decimation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >100 dB
Phase Offset: 1 bit, 0 or 180 degrees
FIR Filter: 18-bit coefficients
Output: Complex, 16-bit I + 16-bit Q
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
Quantity: 34 or 68
Data: Complex, 16-bit I + 16-bit Q
Gain Range: +/–48 dB

Output Gain Blocks
Quantity: 34 or 68
Data: Complex, 16-bit I + 16-bit Q
Gain Range: +/–48 dB

Digital Upconverters
Quantity: 34 or 68
Interpolation Range: 512 to 8192, in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
FIR Filter: 18-bit coefficients, 16-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
Analog Output Channels: 2 or 4
Type: Texas Instruments DAC5688
Input Data Rate: 200 MHz max.
Output Signal: Real
Output Sampling Rate: 800 MHz max. with 4x interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
On-board clock synthesizers generate two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
Type: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Required: Xilinx Virtex-6 XC6VSX315T

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73624: 32 bits only

Environmental
Standard:
 Operating Temp: 0° to 50° C
 Storage Temp: -20° to 90° C
 Relative Humidity: 0 to 95%, non-cond.

Option 702 L2 Extended Temp (air-cooled):
 Operating Temp: -20° to 65° C
 Storage Temp: -40° to 100° C
 Relative Humidity: 0 to 95%, non-cond.

Option 712 L2 Extended Temp (conduction-cooled):
 Operating Temp: -20° to 65° C
 Storage Temp: -40° to 100° C
 Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board
### General Information

Models 72630, 73630 and 74630 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a cPCI carrier board.

Model 72630 is a 6U cPCI board while the Model 73630 is a 3U cPCI board; both are equipped with one Model 71630 XMC. Model 74630 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

### The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP module. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts one or two analog HF or IF input on front panel SSIMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7292 and Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multi-channel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
### 1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - cPCI

**PCI-X Interface**

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73630: 32 bits only.

### Specifications

**Model 72630 or Model 73630:** 1 A/D, 1 D/A  
**Model 74630:** 2 A/Ds, 2 D/As

**Front Panel Analog Signal Inputs (1 or 2)**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converters (1 or 2)**

- **Type:** Texas Instruments ADS5400  
- **Sampling Rate:** 100 MHz to 1 GHz  
- **Resolution:** 12 bits

**D/A Converters (1 or 2)**

- **Type:** Texas Instruments DAC5681Z  
- **Input Data Rate:** 1 GHz max.  
- **Interpolation Filter:** bypass, 2x or 4x  
- **Output Sampling Rate:** 1 GHz max.  
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs (1 or 2)**

- **Output Type:** Transformer-coupled, front panel female SSMC connectors

**Sample Clock Sources (1 or 2)**

- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizers (1 or 2)**

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock

**VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz  
**Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz  
**Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 independently for the A/D clock and D/A clock

**External Clocks (1 or 2)**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

**Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input**

- **Type:** Front panel female SSMC connector, LVTTL  
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2  
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option 104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630

**Memory Banks (1 or 2)**

- **Option 150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR  
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-X Interface**

- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz  
- **Model 73630:** 32 bits only

**Environmental**

- **Operating Temp:** 0° to 50° C  
- **Storage Temp:** –20° to 90° C  
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard 6U or 3U cPCI board

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74630</td>
<td>Two 1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**

- **-002**: -2 FPGA speed grade  
- **-062**: XC6VLX240T FPGA  
- **-064**: XC6VSX315T FPGA  
- **-104**: LVDS I/O between the FPGA and J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630  
- **-160**: Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)  
- **-155**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)  
- **-165**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)  

* This option is always required
1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

### General Information

Models 72640, 73640 and 74640 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board.

Model 72640 is a 6U cPCI board while the Model 73640 is a 3U cPCI board; both are equipped with one Model 71640 XMC. Model 74640 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

### The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640.

### Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SX8 FPGAs
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 or 4 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

➤ A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization
These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources
The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s data and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73640: 32 bits only.

A/D Acquisition IP Modules
These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
# Models 72640, 73640 and 74640

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

## Specifications

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>72640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74640</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

### Field Programmable Gate Array (1 or 2)
- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

### Custom I/O
- **Option -104**: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640

### Memory Banks (1 or 2)
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

### PCI-X Interface
- **PCI-X Bus**: 32 or 64 bits at 33 or 66 MHz
- **Model 73640**: 32 bits only

### Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: Standard 6U or 3U cPCI board

### Ordering Information

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<tr>
<td>74640</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

### Options:
- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required
General Information

Models 72641, 73641 and 74641 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71641 XMC modules mounted on a cPCI carrier board.

Model 72641 is a 6U cPCI board while the Model 73641 is a 3U cPCI board; both are equipped with one Model 71641 XMC. Model 74641 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73641; J3 connector, Model 72641; J3 and J5 connectors, Model 74641.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Features

- Ideal radar and software radio interface solution
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 or 4 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

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[Diagram of Model 72641, 73641, and 74641 block diagrams with key components labeled such as VRTEX6 FPGA, S3X31ST, PCIe, and various I/O interfaces.]

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Pentek, Inc. 
One Park Way • Upper Saddle River • New Jersey 07458 
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to ƒs where ƒs is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*ƒs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of ƒs/N.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

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**VIRTTEX-6 FPGA DATAFLOW DETAIL**

Programmable decimation of 8, 16 or 32 available in one channel mode.
### PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73641: 32 bits only.

### Specifications

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<tbody>
<tr>
<td>72641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74641</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U cPCI</td>
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</tr>
</tbody>
</table>

**Options:**
- 002* - 2 FPGA speed grade
- 064* - XC6VSX315T
- 104 - LVDS I/O between the FPGA and J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640
- 155* - Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165* - Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

**Sample Clock Sources (1 or 2)**
Front panel SSMC connector

**Sync Bus (1 or 2)**
Multi-pin connectors, bus includes gate, reset and in and out ref clock

**External Trigger Input (1 or 2)**
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**
Xilinx Virtex-6 XC6VSX315T-2

**Custom I/O**
- Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640

**Memory Banks (1 or 2)**
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-X Interface**
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73641: 32 bits only

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

**Size:** Standard 6U or 3U cPCI board
Models 72650, 73650 and 74650

2- or 4-Channel 500 MHz A/D, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

General Information
Models 72650, 73650 and 74650 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71650 XMC modules mounted on a cPCI carrier board.

Model 72650 is a 6U cPCI board while the Model 73650 is a 3U cPCI board; both are equipped with one Model 71650 XMC. Model 74650 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, one or two DUCs, two or four D/As and four banks of memory.

The Cobalt Architecture
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog inter- faces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 72650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

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![Block Diagram, Model 72650](image)

Model 72650 doubles all resources except the PCI-to-PCI Bridge

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![Virtex-6 FPGA](image)

LX130T, LX240T or SX315T

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![Cobalt Architecture](image)

Models 73650 and 74650 are equipped with one Model 71650 XMC. Model 74650 doubles all resources except the PCI-to-PCI Bridge.
A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs and D/As accept a baseband real or complex data streams from the FPGA and provide that input to the upconverter, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the
2- or 4-Channel 500 MHz A/D, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - cPCI

- board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI-X Interface**

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73650: 32 bits only.

**Specifications**

Models 72650 and 73650: 2 A/Ds, 1 DUC, 2 D/As
Model 74650: 4 A/Ds, 2 DUCs, 4 D/As
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits
A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits
D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz, max.
Output IF: DC to 400 MHz, max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz, max. with interpolation
Resolution: 16 bits
Front Panel Analog Signal Outputs (2 or 4)
Output Type: Transformer-coupled, front panel female SSCM connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

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**Ordering Information**

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<th>Model</th>
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<tr>
<td>72650</td>
<td>Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73650</td>
<td>Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74650</td>
<td>Four 500 MHz A/Ds, Two DUCs, Four 800 MHz D/As with Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**
- 002* -2 FPGA speed grade
- 014 400 MHz, 14-bit A/Ds
- 062 XC6VLSX240T FPGA
- 064 XC6VLSX315T FPGA
- 104 LVDS I/O between the FPGA and J2 connector, Model 73650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

**Sample Clock Sources (2 or 4)**

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock.

**Clock Synthesizers (1 or 2)**

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers**

External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clocks (1 or 2)**

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus (1 or 2):** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Inputs (1 or 2)**

Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VLSX315T-2

**Custom I/O**

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73650; J3 connector, Model 72650; J3 and J5 connectors, Model 74650

**Memory Banks (1 or 2)**

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-X Interface**

**PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
Model 73650: 32 bits only

**Environmental**

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard 6U or 3U cPCI board

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Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
General Information

Models 72651, 73651 and 74651 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board.

Model 72651 is a 6U cPCI board while the Model 73651 is a 3U cPCI board; both are equipped with one Model 71651 XMC. Model 74651 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As and three or six banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface completely the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extensible IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX3 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.
**A/D Acquisition IP Modules**

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**Beamformer IP Core**

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple models can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

**D/A Waveform Playback IP Modules**

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to three or six independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73651: 32 bits only.
## Specifications

Model 72651 or Model 73651: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/A

Model 74651: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/A

### Front Panel Analog Signal Inputs (2 or 4)

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### A/D Converters (standard) (2 or 4)

- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

### A/D Converters (Option -014) (2 or 4)

- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

### Digital Downconverters (2 or 4)

- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### D/A Converters (2 or 4)

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

### Digital Interpolators (1 or 2)

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

### Beamformers (1 or 2)

- **Summation:** Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via a dual 4X connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

### Front Panel Analog Signal Outputs (2 or 4)

- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### Sample Clock Sources (2 or 4)

- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

### Clock Synthesizers (1 or 2)

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

### External Clocks (1 or 2)

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

### Field Programmable Gate Arrays (1 or 2)

- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

### Memory (1 or 2)

- **Option -150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option -155 or -165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

### PCI-X Interface

- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz

### Environmental

- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard 6U or 3U cPCI board

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**Ordering Information**

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<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>72651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74651</td>
<td>4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U cPCI</td>
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</tbody>
</table>

**Options:**

- **002***: -2 FPGA speed grade
- **014**: 400 MHz, 14-bit A/Ds
- **062**: XC6VLX240T FPGA
- **064**: XC6VSX315T FPGA
- **150**: Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **155**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **165**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required
General Information

Models 72660, 73660 and 74660 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a cPCI carrier board.

Model 72660 is a 6U cPCI board while the Model 73660 is a 3U cPCI board; both are equipped with one Model 71660 XMC. Model 74660 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660. 

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Converter Stage

The front end accepts four or eight full-scale analog HF or LF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An onboard clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73660: 32 bits only.
Specifications

Model 72660 or Model 73660: 4 A/Ds
Model 74660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)
On-board clock synthesizers

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73660: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

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<th>Model</th>
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<tr>
<td>72660</td>
<td>4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U cPCI</td>
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<tr>
<td>73660</td>
<td>4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74660</td>
<td>8-Channel 200 MHz, 16-bit A/D with two Virtex-6 FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- -062   XC6VLX240T FPGA
- -064   XC6VSX315T FPGA
- -104   LVDS I/O between the FPGA and J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660
- -150   Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- -160   Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- -155   Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165   Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
General Information
Models 72661, 73661 and 74661 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a cPCI carrier board.

Model 72661 is a 6U cPCI board while the Model 73661 is a 3U cPCI board; both are equipped with one Model 71661 XMC. Model 74661 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, four or eight multiband DDCs and four or eight banks of memory.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or 32 MB or 64 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage.
PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73661: 32 bits only.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72661 or Model 73661: 4 A/Ds
Model 74660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters (4 or 8)

Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to fs
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board
General Information

Models 72662, 73662 and 74662 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a cPCI carrier board.

Model 72662 is a 6U cPCI board while the Model 73662 is a 3U cPCI board; both are equipped with one Model 71662 XMC. Model 74662 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, 32 or 64 multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- 32 or 64 channels of multiband DDCs (digital downconverters)
- Up to 2 or 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

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Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662.
is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

**A/D Converter Stage**

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with DDR3 SDRAM.
Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the Board’s DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI-X Interface**

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73662: 32 bits only.

### Specifications

**Model 72662 or Model 73662: 4 A/Ds, 32 DDCs**

**Model 74660: 8 A/Ds, 64 DDCs**

**Front Panel Analog Signal Inputs (4 or 8)**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters (4 or 8)**

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Digital Downconverters (32 or 64)**

- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

### Sample Clock Sources (1 or 2)

- On-board clock synthesizer

### Clock Synthesizers (1 or 2)

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

### External Clocks (1 or 2)

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

### Timing Bus (1 or 2): 26-pin connector

- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### External Trigger Inputs (1 or 2)

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array (1 or 2)

- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

### Custom I/O

- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73662; J3 connector, Model 72662; J3 and J5 connectors, Model 74662

### Memory Banks (1 or 2)

- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

### PCI-X Interface

- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz Model 73662: 32 bits only

### Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

### Size

- **Standard 6U or 3U cPCI Board**
New! New! New! New! New!

Models 72663, 73663 and 74663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

General Information

Models 72663, 73663 and 74663 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a cPCI carrier board.

Model 72663 is a 6U cPCI board while the Model 73663 is a 3U cPCI board; both are equipped with one Model 71663 XMC. Model 74663 is a 6U cPCI board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors. The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/ Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤
GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insures that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once compete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73663: 32 bits only.

The PCI-X interface is also used as the programming interface for all status and control between these models and host.
1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

Specifications

Model 72663 or Model 73663: 4 A/Ds
Model 74663: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks (1 or 2)
DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz,
where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 KHz
> 96 dB attenuation at > ±3 MHz

DDC Output Rate fs: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:
First: -fs/4 (-270.8333 kHz)
Second: 0 Hz
Third: +fs/4 (+270.8333 kHz)
Fourth: +fs/2 (+541.666 kHz)

Superchannel Sample Rate: fs
Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Arrays (1 or 2)
Xilinx Virtex-6 XC6VSX315T

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73663: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

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<th>Model</th>
<th>Description</th>
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<td>1100-Channel GSM Channelizer with Quad A/D - 6U cPCI</td>
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<td>1100-Channel GSM Channelizer with Quad A/D - 3U cPCI</td>
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<tr>
<td>74663</td>
<td>2200-Channel GSM Channelizer with Octal A/D - 6U cPCI</td>
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</table>
General Information

Models 72664, 73664 and 74664 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71664 XMC modules mounted on a cPCI carrier board.

Model 72664 is a 6U cPCI board while the Model 73664 is a 3U cPCI board; both are equipped with one Model 71664 XMC. Model 74664 is a 6U cPCI board with two XMC modules rather than one.

The output of these models supports fully the VITA 49.0 Radio Transport (VRT) Standard. These models include four or eight A/Ds, four or eight multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Features

- Complete radar and software radio interface solutions
- Support VITA 49.0 Radio Transport (VRT) Standard
- Support Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

Block Diagram, Model 72664

Model 74664 doubles all resources except the PCI-to-PCI Bridge.

- A/D Clock/Sync Bus
- Timing Bus
- VCXO
- Clock / Sync / Gate / PPS
- TTL Gate / Trigger / Sync / PPS
- Sample Clock
- Reference Clock
- GPIOs

Virtex-6 FPGA

Xilinx Virtex-6 FPGA

QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to 1/2fs where fs is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of fs/N.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC output cores. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

These models support fully the VITA 49.0 specification.
Models 72664, 73664 and 74664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - cPCI

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73664: 32 bits only.
# Specifications

**Model 72664 or Model 73664: 4 A/Ds**
- **Front Panel Analog Signal Inputs (4 or 8):**
  - **Input Type:** Transformer-coupled, front panel female SSMC connectors
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Input:** +8 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters (4 or 8):**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Digital Downconverters (4 or 8):**
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Beamformers (1 or 2):**
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

**Sample Clock Sources (1 or 2):**
- On-board clock synthesizer

**Clock Synthesizers (1 or 2):**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clocks (1 or 2):**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**External Trigger Inputs (1 or 2):**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2):**
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

**Memory Banks (1 or 2):**
- **Option 150 or 160:** Two 8 MB QDRII+ SDRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-X Interface:**
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz

**Environmental:**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard 6U or 3U cPCI board

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## Ordering Information

<table>
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<tr>
<th>Model</th>
<th>Description</th>
</tr>
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<tr>
<td>72664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA 49.0, one Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74664</td>
<td>8-Channel 200 MHz A/D with DDCs, VITA 49.0, two Virtex-6 FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**
- **062** XCV6LX240T
- **064** XCV6SX315T
- **150** Two 8 MB QDRII+ SDRAM Memory Banks (Banks 1 and 2)
- **155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **160** Two 8 MB QDRII+ SDRAM Memory Banks (Banks 3 and 4)
- **165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
General Information

Models 72670, 73670 and 74670 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a cPCI carrier board.

Model 72670 is a 6U cPCI board while the Model 73670 is a 3U cPCI board; both are equipped with one Model 71670 XMC. Model 74670 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight D/A, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670.
Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by factors, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 74670.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

2, 4, 8, or 16 to provide lower frequency D/A clocks. A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7292, 7392 and 7492 or the 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73670: 32 bits only.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked list controllers support waveform generation to the four or eight D/A channels from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 74670.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
Specifications

Models 72670 and 73670: 4-Channel DUC, 4-channel D/A
Model 74670: 8-Channel DUC, 4-channel D/A

D/A Converters (4 or 8)
- Type: TI DAC3484
- Input Data Rate: 312.5 MHz max.
- Output Bandwidth: 250 MHz max.
- Output Sampling Rate: 1.25 GHz max. with interpolation
- Interpolation: 2x, 4x, 8x or 16x
- Resolution: 16 bits

Front Panel Analog Signal Outputs (4 or 8)
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO or front panel external clock
- VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
- Type: Front panel female SSMC connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670

Memory Banks (1 or 2)
- Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73670: 32 bits only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
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<tr>
<td>72670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI</td>
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<tr>
<td>73670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74670</td>
<td>8-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- -002* -2 FPGA speed grade
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS I/O between the FPGA and J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required
4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - cPCI

General Information
Models 72671, 73671 and 74671 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71671 XMC modules mounted on a cPCI carrier board.

Model 72671 is a 6U cPCI board while the Model 73671 is a 3U cPCI board; both are equipped with one Model 71671 XMC. Model 74671 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671. —

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/ sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectible IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, these models feature an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog outputs are through front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel μSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7292, 7392 and 7492 or the 9192 Cobalt Synchronizers can drive multiple μSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Models 72671, 73671 and 74671
4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - cPCI

➤ PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73671: 32 bits only.

Specifications
Models 72671 and 73671: 4-Channel DUC, 4-channel D/A
Model 74671: 8-Channel DUC, 8-channel D/A
D/A Converters (4 or 8)
   Type: TI DAC3484
   Input Data Rate: 312.5 MHz max.
   Output Bandwidth: 250 MHz max.
   Output Sampling Rate: 1.25 GHz max.
   with interpolation
   Interpolation: 2x, 4x, 8x or 16x
   Resolution: 16 bits
Digital Interpolator
   Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Front Panel Analog Signal Outputs (4 or 8)
   Output Type: Transformer-coupled, front panel female SSMC connectors
   Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
   Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15
Clock Synthesizers (1 or 2)
   Clock Source: Selectable from on-board programmable VCXO or front panel external clock
   VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
   Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
   Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
   Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
   Type: Front panel female SSMC connector
   Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
   Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
   Option -04: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671

Memory Banks (1 or 2)
   Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
   PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
   Model 73671: 32 bits only

Environmental
   Operating Temp: 0° to 50° C
   Storage Temp: –20° to 90° C
   Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

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</tr>
<tr>
<td>74671</td>
<td>8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U cPCI</td>
</tr>
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</table>

Options:
- -002* -2 FPGA speed grade
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS I/O between the FPGA and J2 connector, Model 73671; J3 connector, Model 72671; J3 and J5 connectors, Model 74671
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* These options are always required
General Information

Models 72690, 73690 and 74690 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a cPCI carrier board.

Model 72690 is a 6U cPCI board while the Model 73690 is a 3U cPCI board; both are equipped with one Model 71690 XMC. Model 74690 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as well as source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications that require large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74690.

Features

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB QDRII+ SRAM
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

➤ RF Tuner Stage

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LN Bs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. ➤
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA.

PCI-X Interface

The models include an industry-standard interface compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73690: 32 bits only.

Specifications

Model 72690 or Model 73690: 1 RF tuner, 2 A/Ds
Model 74690: 2 RF tuners, four A/Ds
Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuners (1 or 2)
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
\[ \text{freq}_{\text{VCO}} = (N.F) \times \text{freq}_{\text{REF}} \]
where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference (freq\_REF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
*Usable Full-.Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters (2 or 4)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer
A/D Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Inputs (1 or 2)
Type: Front panel female SSMC connector, sine wave. 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (2 or 4)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Option -100, 12 to 30 MHz
Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73690: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board
3- or 6-Channel 200 MHz A/D, 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

General Information

Models 72720, 73720 and 74720 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71720 XMC modules mounted on a cPCI carrier board.

Model 72720 is a 6U cPCI board while the Model 73720 is a 3U cPCI board; both are equipped with one Model 71720 XMC. Model 74720 is a 6U cPCI board with two XMC modules rather than one.

These models include three or six A/Ds, one or two D/As, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCI-X interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Pentek, Inc.
One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where the external media drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine automatically constructs metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware configuration simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages. 

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73620: 32 bits only.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72720</td>
<td>3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73720</td>
<td>3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74720</td>
<td>6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A and two Virtex-7 FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- 073: XC7VX330T-2 FPGA
- 076: XC7VX690T-2 FPGA
- 104: LVDS I/O between the FPGA and J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720

Specifications

Model 72620 or Model 73620: 3 A/Ds, 1 DUC, 2 D/As
Model 74620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- Input Type: Transformere-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

D/A Converters (2 or 4)
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with interpolation
- Resolution: 16 bits

Front Panel Analog Signal Outputs (2 or 4)
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73720; J3 connector, Model 72720; J3 and J5 connectors, Model 74720

Memory Banks (1 or 2)
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
- Model 73620: 32 bits only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGA - cPCI

**General Information**

Models 72721, 73721 and 74721 are members of the Onyx family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71721 XMC modules mounted on a cPCI carrier board.

Model 72721 is a 6U cPCI board while the Model 73721 is a 3U cPCI board; both are equipped with one Model 71721 XMC. Model 74721 is a 6U cPCI board with two XMC modules rather than one.

These models include three or six A/Ds, programmable DDCs, one or two DUCs, two or four D/A and four or eight banks of memory.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains one or two interpolation IP cores, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs
- Two or four 800 MHz 16-bit D/As
- One or two DUCs
- Multiboard programmable beamformer
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

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**Block Diagram, Model 72721**

Model 74721 doubles all resources except the PCI-to-PCI Bridge
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUC (digital upconverters) and D/A's accept baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesize circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73721: 32 bits only.
Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72721 or Model 73721: 3 A/Ds, 1 DUC, 2 D/As
Model 74721: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
Input: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters (3 or 6)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolators (1 or 2)
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources (2 or 4)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for input/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73721: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board
Models 72730, 73730 and 74730

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - cPCI

General Information

Models 72730, 73730 and 74730 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a cPCI carrier board.

Model 72730 is a 6U cPCI board while the Model 73730 is a 3U cPCI board; both are equipped with one Model 71730 XMC. Model 74730 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730.

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Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a linked definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP Modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCI-X interface. At power up, the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts one or two analog HF or IF input on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458 Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72730 or Model 73730: 1 A/D, 1 D/A
Model 74730: 2 A/Ds, 2 D/As
Front Panel Analog Signal Inputs (1 or 2)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converters (1 or 2)
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730

Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73730: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: −20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board
New Information

Models 72741, 73741 and 74741 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a cPCI carrier board.

Model 72741 is a 6U cPCI board while the Model 73741 is a 3U cPCI board; both are equipped with one Model 71741 XMC. Model 74741 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741.

Pentek, Inc., One Park Way, Upper Saddle River, New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com

Model 74741 Model 73741

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**General Information**

Models 72741, 73741 and 74741 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a cPCI carrier board.

Model 72741 is a 6U cPCI board while the Model 73741 is a 3U cPCI board; both are equipped with one Model 71741 XMC. Model 74741 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs.

In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741.
**A/D Acquisition IP Module**

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/D or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
Models 72741, 73741 and 74741

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - cPCI

Memory Resources

The Onyx architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73741: 32 bits only.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74741</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FGPA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- -073 XC7VX330T-2 FPGA
- -076 XC7VX690T-2 FPGA
- -104 LVDS I/O between the FPGA and J2 connector, Model 73741: J3 and J5 connectors, Model 72741: J3 and J5 connectors, Model 74741

-037 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U cPCI
-076 XC7VX690T-2 FPGA
-104 LVDS I/O between the FPGA and J2 connector, Model 73741: J3 and J5 connectors, Model 72741: J3 and J5 connectors, Model 74741

Specifications

Model 72741 or Model 73741: One A/D
Model 74741: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to 1/2
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741: J3 connector, Model 72741: J3 and J5 connectors, Model 74741

Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73741: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
General Information
Models 72650, 73650 and 74650 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a cPCI carrier board.

Model 72751 is a 6U cPCI board while the Model 73751 is a 3U cPCI board; both are equipped with one Model 71751 XMC. Model 74751 is a 6U cPCI board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/A and four or eight banks of memory.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T.

The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the J2 connector.

The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the J2 connector.

Pentek, Inc.  One Park Way  ●  Upper Saddle River  ●  New Jersey 07458  
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com  
www.pentek.com
**A/D Acquisition IP Modules**

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072, providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**D/A Waveform Playback IP Module**

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

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**GateXpress for FPGA Configuration**

The Oryn architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course
of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, Texas Instruments ADS5474 400 MHz, 14-bit A/Ds may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept the baseband real or complex data stream from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog outputs are through front-panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73751: 32 bits only.

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# Models 72751, 73751 and 74751

| 2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A with Virtex-7 FPGA - cPCI |

## Specifications

**Model 72751 or Model 73751:**
- 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As

**Model 74751:**
- 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

### Front Panel Analog Signal Inputs (2 or 4)
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### A/D Converters (standard) (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

### A/D Converters (option -014) (2 or 4)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

### Digital Downconverters (2 or 4)
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \(f_s\)
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### D/A Converters (2 or 4)
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

### Digital Interpolators (1 or 2)
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x
- **Total Interpolation Range (D/A and Digital combined):** 2x to 524,288x

### Front Panel Analog Signal Outputs (2 or 4)
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

### Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

### Clock Dividers
- External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

### External Clocks (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

### Timing Bus (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### Field Programmable Gate Arrays (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

### Custom I/O
- **Option -104:** Provides 24 LVDS pairs between the FPGA and the J2 connector, Model 72751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751

### Memory (1 or 2)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

### PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
- **Model 73751:** 32 bits only

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

### Size
- **Standard 6U or 3U cPCI board**

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72751</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73751</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74751</td>
<td>4-Channel 500 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-7 FGPA - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**
- **-014** 400 MHz, 14-bit A/Ds
- **-076** XC7VX690T-2 FPGA
- **-104** LVDS I/O between the FPGA and J2 connector, Model 73751; J3 connector, Model 72751; J3 and J5 connectors, Model 74751
General Information

Models 72760, 73760 and 74760 are members of the Onyx\textsuperscript{TM} family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a cPCI carrier board.

Model 72760 is a 6U cPCI board while the Model 73760 is a 3U cPCI board; both are equipped with one Model 71760 XMC. Model 74760 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73760: 32 bits only.

Specifications
Model 72760 or Model 73760: 4 A/Ds
Model 74760: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
General Information

Models 72761, 73761 and 74761 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71761 XMC modules mounted on a cPCI carrier board.

Model 72761 is a 6U cPCI board while the Model 73761 is a 3U cPCI board; both are equipped with one Model 71761 XMC. Model 74761 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds, programmable DDCs and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- Multiboard programmable beamformer
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \(f_s\), where \(f_s\) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \(0.8 \times f_s/N\), where \(N\) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

Beamformer IP Core

In addition to the DDCs, these models feature a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from.
FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73761: 32 bits only.
Specifications

Model 72761 or Model 73761: 4 A/Ds, Model 74761: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters (4 or 8)
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources (1 or 2)
- On-board clock synthesizer

Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2) 26-pin connector
- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Memory Banks (1 or 2)
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
- Model 73761: 32 bits only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>72761</td>
<td>4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 6U cPCI</td>
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<tr>
<td>73761</td>
<td>4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74771</td>
<td>8-Channel 200 MHz A/D with DDCs, Virtex-7 FGPA - 6U cPCI</td>
</tr>
</tbody>
</table>

Option:
-076  XC7VX690T-2 FPGA
Models 72791, 73791 and 74791 1 or 2 L-Band RF Tuners, 2- or 4-Channel 500 MHz A/Ds, Virtex-7 FPGAs - cPCI

General Information

Models 72791, 73791 and 74791 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71791 XMC modules mounted on a cPCI carrier board.

Model 72791 is a 6U cPCI board while the Model 73791 is a 3U cPCI board; both are equipped with one Model 71791 XMC. Model 74791 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds, two or four DDCs and four or eight banks of memory, one or two general purpose connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features one or two Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The factory-installed functions include two or four A/D acquisition IP modules, four or eight DDR3 memory controllers, two or four DDCs, RF tuner controllers, clock and synchronization generators, and one or two test signal generators.

Thus, these models can operate as complete turnkey solutions with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791. ➤
A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accomodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
Models 72791, 73791 and 74791

➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The analog tuner outputs are digitized by two or four Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two or four independent A/D and DDC channels are now available for digitizing and downconverting signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

One or two internal timing generators provide all timing, gating, triggering and synchronization functions required by the A/D converters. They also serve as optional sources for the L-Band tuner references.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent 1 GB DDR3 SDRAMs for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be used to support custom user-installed IP within the FPGA.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73791: 32 bits only. ➤
## Specifications

**Model 72791 or Model 73791:** 1 L-band Tuner, 2 A/Ds, 2 DDCs, 1 FPGA

**Model 74791:** 2 L-Band Tuners, 4 A/Ds, 4 DDCs, 2 FPGAs

### Front Panel Analog Signal Inputs (1 or 2)
- Connector: Front panel female SSMC
- Impedance: 50 ohms

### L-Band Tuner (1 or 2)
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** –97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:**
  \[ \text{freq}_{\text{VCO}} = (N, F) \times \text{freq}_{\text{REF}} \]
  where integer \( N \) = 19 to 251 and fractional \( F \) is a 20-bit binary value
- **PLL Reference** (freq\textsubscript{REF}): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** –50 dBm to +10 dBm
- **Baseband Low Pass Filter:** 3 dB cutoff frequency: 123.75 MHz

### A/D Converters (2 or 4)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

### Sample Clock Sources (1 or 2)
- On-board timing generator/synthesizer

### A/D Clock Synthesizers (1 or 2)
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

### Timing Generator External Clock Input (1 or 2)
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

### Timing Generator Bus (1 or 2)
- 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### External Trigger Input (2 or 4)
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array (1 or 2)
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

### Custom I/O
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791

### Memory Banks (4 or 8)
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

### PCI-X Interface
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
- **Model 73791:** 32 bits only

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Standard 6U or 3U cPCI board

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## Ordering Information

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72791</td>
<td>L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73791</td>
<td>L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74791</td>
<td>2 L-Band RF Tuners with 4-Channel 500 MHz A/D with DDCs and two Virtex-7 FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

### Options:
- **-014** 400 MHz, 14-bit A/Ds
- **-076** XC7VX690T-2 FPGA
- **-100** 27 MHz crystal for MAX2121
- **-104** LVDS I/O between the FPGA and J2 connector, Model 73791; J3 connector, Model 72791; J3 and J5 connectors, Model 74791
8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - cPCI

General Information

Models 72131, 73131 and 74131 are members of the Jade family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71131 XMC modules mounted on a cPCI carrier board. Model 72131 is a 6U board while Model 73131 is a 3U board; both have one Model 71131 module. Model 74131 is equipped with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections and the option for a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation.
A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or a test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients.

The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

➤ encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73131; J3 connector, Model 72131; J3 and J5 connectors, Model 74131.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73131: 32 bits only.
Specifications

Models 72131 and 73131: 8 A/Ds
Model 74131: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8 or 16)
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Digital Downconverters (8 or 16)
- Quantity: Four channels
- Decimation Range: 2x to 32,768x in three stages of 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
- On-board clock synthesizer

Clock Synthesizer (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104: LVDS I/O between the FPGA and J2 connector, Model 73131; J3 connector, Model 72131; J3 and J5 connectors, Model 74131

Memory
- Type: DDR4 SDRAM
- Size: 5 GB Models 72131 and 73131; 10 GB Model 74131
- Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
- Model 73131: 32 bits only

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Option -702: L2 (air cooled)
- Operating Temp: –20° to 65° C
- Storage Temp: –40° to 100° C
- Relative Humidity: 0 to 95%, non-condensing

Size: Standard 6U or 3U cPCI board

Ordering Information

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<tr>
<td>72131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74131</td>
<td>16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- -084 XCKU060-2 FPGA
- -087 XCKU115-2 FPGA
- -104 LVDS FPGA I/O
- -702 Air cooled, Level L2
**General Information**

Models 72132, 73132 and 74132 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71132 XMC modules mounted on a cPCI carrier board. Model 72132 is a 6U board while Model 73132 is a 3U board; both have one Model 71132 module. Model 74132 is equipped with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections and a large DDR4 memory.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.
A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or one or two test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The 80% default filters deliver an output bandwidth of 0.8\( f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

When using decimation levels of 2 to 32, 32-bit IQ samples are output. These are aligned to the base sample rate of 1024 times the A/D sampling frequency. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the KU060 FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132.

A/D Converter Stage

The front end accepts eight or 16 analog HF or IF inputs on front panel MMCX connectors with transformer coupling into four or eight TI ADS42LB69 dual 250 MHz, 16-bit A/Ds.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73132: 32 bits only.
Specifications

Models 72132 and 73132: 8 A/Ds
Model 74132: 16 A/Ds

Front Panel Analog Signal Inputs (8 or 16)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (8 or 16)
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Wideband Digital Downconverters (8 or 16)
- Decimation Range: 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (64 or 128)
- Decimation Range: 16x to 1024x in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$ independent tuning for each channel
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
- On-board clock synthesizer

Clock Synthesizer (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
- External Clock (1 or 2)
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -010: LVDS I/O between the FPGA and J2 connector, Model 72132; J3 connector, Model 72132; J3 and J5 connectors, Model 74132

Memory
- Type: DDR4 SDRAM
- Size: 5 GB Models 72132 and 73132; 10 GB Model 74132
- Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz; Model 73132: 32 bits only

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Ordering Information

<table>
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<tr>
<th>Model</th>
<th>Description</th>
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<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U cPCI</td>
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<td>73132</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U cPCI</td>
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<tr>
<td>74132</td>
<td>16-Channel 250 MHz A/D with DDCs and two Kintex UltraScale FPGAs - 6U cPCI</td>
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Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 702 Air cooled, Level L2
General Information

Models 72141, 73141 and 74141 are members of the Jade family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a cPCI carrier board. Model 72141 is a 6U cPCI board while the Model 73141 is a 3U cPCI board; both are equipped with one Model 71141 XMC. Model 74141 is a 6U cPCI board with two XMC modules rather than one.

They include two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. These models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include two or four A/D acquisition IP modules.

Each of the acquisition IP modules contains a programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.
A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either onboard memory or off-board host memory.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7292 high-speed sync boards to drive the sync bus.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA(s) can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73141: 32 bits only.
Specifications

Model 72141 or Model 73141: Two A/Ds
Model 74141: Four A/Ds
Model 72141 or Model 73141: Two D/A
Model 74141: Four D/A

Front Panel Analog Signal Inputs (2 or 4)
   Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter (2 or 4)
   Type: ADC12DJ3200
   Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
   Resolution: 12 bits
   Input Bandwidth: Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters (2 or 4)
   Type: Texas Instruments DAC38RF82
   Output Sampling Rate: 6.4 GHz.
   Resolution: 14 bits

Sample Clock Source (1 or 2)
   Front panel SSMC connector

Timing Bus (1 or 2)
   19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)
   Type: Front panel female SSMC connector, LVTTL
   Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
   Standard: Xilinx Kintex UltraScale
   Option -084: Xilinx Kintex UltraScale
   Option -087: Xilinx Kintex UltraScale

Custom I/O
   Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74141

Memory (1 or 2)
   Type: DDR4 SDRAM
   Size: GB
   Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
   PCI-X Bus: 32 or 64 bits at 33 or 66 MHz

Environmental
   Standard: L0 (air cooled)
      - Operating Temp: 0° to 50° C
      - Storage Temp: -20° to 90° C
      - Relative Humidity: 0 to 95%, non-condensing

   Option -702: L2 (air cooled)
      - Operating Temp: -20° to 65° C
      - Storage Temp: -40° to 100° C
      - Relative Humidity: 0 to 95%, non-condensing

   Size: 6U board 9.187 in x 6.717 in
      (233.3 mm x 170.6 mm)

Ordering Information

Model  Description

72141  1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI

73141  1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI

74141  2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and two Kintex UltraScale FPGAs - 6U cPCI

Options:
- 084   XCKU060-2 FPGA
- 087   XCKU115-2 FPGA
-104   LVDS I/O between the FPGA and J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74841
-702   Air cooled, Level L2
3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

General Information

Models 72821, 73821 and 74821 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71821 XMC modules mounted on a cPCI carrier board. Model 72821 is a 6U cPCI board while the Model 73821 is a 3U cPCI board; both are equipped with one Model 71821 XMC. Model 74821 is a 6U cPCI board with two XMC modules rather than one. They include three or six A/Ds, complete multiboard clock and sync sections, large DDR4 memory, three or six DDCs, one or two DUCs and two or four D/As. In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The factory-installed functions for these models include three or six A/D acquisition and one or two waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three or six powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; programmable interpolators, and a PCI-X interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from three A/Ds, or the test signal generators.

Each acquisition module has a DMA engine for easily moving A/D data through the PCI-X interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the D/A's waveform stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition rate etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

D/A Converter Stage

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

ADA Converter Stage

Within each A/D Acquisition IP Module is a powerful D/A IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73821; J3 connector, Model 72821; J3 and J5 connectors, Model 74821.
Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73821: 32 bits only.
Specifications

Model 72821 or Model 73821: 3 A/Ds, 1 DUC, 2 D/As
Model 74821: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters (3 or 6)
- Decimation Range: 2x to 32,768x in three stages of 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (1 or 2)
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max.
- Resolution: 16 bits

Digital Interpolator Core (1 or 2)
- Interpolation Range: 2x to 32,768x in three stages of 2x to 32x
- Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array (1 or 2)
- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73821; J3 connector, Model 72821; J3 and J5 connectors, Model 74821

Memory (1 or 2)
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
- Model 73821: 32 bits only

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size:
- 6U board 9.187 in x 6.717 in
- (233.3 mm x 170.6 mm)
- 3U board 3.937 in. x 6.717 in.
- (100.00 mm x 170.61 mm)

Options:
- -084 XCKU060-2 FPGA
- -087 XCKU115-2 FPGA
- -104 LVDS FPGA I/O
- -702 Air cooled, Level L2

Contact Pentek for complete specifications of rugged version
General Information

Models 72841, 73841 and 74841 are members of the Jade family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a cPCI carrier board. Model 72841 is a 6U cPCI board while the Model 73841 is a 3U cPCI board; both are equipped with one Model 71841 XMC. Model 74841 is a 6U cPCI board with two XMC modules rather than one.

They include one or two A/Ds, programmable DDCs, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O

Pentek, Inc.
One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high-speed sync boards to drive the sync bus.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16. In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely. The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8\times f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the J3 (or J2 connector, Model 73841) for custom interfaces or logic.
1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz 12-bit A/Ds, with Wideband DDCs, Kintex Ultrascale FPGAs - CompactPCI

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73841: 32 bits only.

Specifications

Model 72841 or Model 73841: One A/D
Model 74841: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841

Memory Banks (1 or 2)
Type: DDR4 SDRAM
Size: One or two banks, 5 GB each
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73741: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>72841</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73841</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74841</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Kintex UltraScale FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS I/O between the FPGA and J2 connector, Model 73841; J3 connector, Model 72841; J3 and J5 connectors, Model 74841
- 702 Air cooled, Level L2
General Information

Models 72851, 73851 and 74851 are members of the Jade family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71851 XMC modules mounted on a cPCI carrier board. Model 72851 is a 6U cPCI board while the Model 73851 is a 3U cPCI board; both are equipped with one Model 71851 XMC. Model 74851 is a 6U cPCI board with two XMC modules rather than one.

They include two or four A/Ds, a complete multiblock clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As. In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The factory-installed functions of these models include two or four A/D acquisition and two or four waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: two or four powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for data clocking and synchronization functions; test signal generators; programmable interpolators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions thereby saving the time of IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own custom IP for data processing.
Models 72851  73851 and 74851

2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

**A/D Acquisition IP Modules**
These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**
Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

**D/A Waveform Playback IP Modules**
The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/As waveforms stored in either on-board memory or off-board host memory.

**Xilinx Kintex UltraScale FPGA**
Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851.

**A/D Converter Stage**
The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.
2- or 4-Channel 500 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - cPCI

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A sections.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73851: 32 bits only.
Specifications

Model 72851: 2 A/Ds
Model 73851: 2 A/Ds
Model 74851: 4 A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard) (2 or 4)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits

A/D Converters (option -014) (2 or 4)
Type: Texas Instruments ADS5474
Sampling Rate: 20 MHz to 400 MHz
Resolution: 14 bits

Digital Downconverters (2 or 4)
Quantity: Two channels
Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters (2 or 4)
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits

Digital Interpolator Core (1 or 2)
Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs (2 or 4)
Output: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: (1 or 2)
26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73851; J3 connector, Model 72851; J3 and J5 connectors, Model 74851

Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73851: 32 bits only

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 6U Board 9.187 in x 6.717 in
3U Board 3.937 in x 6.717 in

Contact Pentek for complete specifications of rugged version

Pentek, Inc., One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com

WWW.pentek.com
Models 72861, 73861 and 74861 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71861 XMC modules mounted on a cPCI carrier board. Model 72861 is a 6U board while Model 73861 is a 3U board; both have one Model 71861 module. Model 74861 is equipped with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available
where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73861; J3 connector, Model 72861; J3 and J5 connectors, Model 74861.

**A/D Converter Stage**

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors or test signal generators. Each DDC accepts a unique set of user-supplied 24-bit coefficients. A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, providing a wide range to satisfy most applications.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Models 72861
73861 & 74861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73861: 32 bits only.

Specifications

Models 72861 and 73861: 4 A/Ds
Model 74861: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters (4 or 8)
Quantity: Four channels
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: (1 or 2)
On-board clock synthesizer
Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Sample Clock Sources: (1 or 2)
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Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Specifications

Models 72861 and 73861: 4 A/Ds
Model 74861: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
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Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Environmental

Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Ordering Information

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<td>8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U cPCI</td>
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Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS I/O between the FPGA and J 2 connector, Model 73861; J 3 connector, Model 72861; J 3 and J 5 connectors, Model 74861
- 702 Air cooled, Level L2
**General Information**

Models 72862, 73862 and 74862 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71862 XMC modules mounted on a cPCI carrier board. Model 72862 is a 6U board while Model 73862 is a 3U board; both have one Model 71862 module. Model 74862 is equipped with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDR4 IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight wideband DDCs and
- 32 or 64 multiband DDCs (digital downconverters)
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized version available

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**Table**

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A/D Acquisition IP Modules
These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores
Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862.

A/D Converter Stage
The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal processing or routing to other board resources.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

![Kintex UltraScale FPGA Dataflow](image-url)
Models 72862 73862 & 74862

4- or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - cPCI

➤ PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73862: 32 bits only.

Specifications

Models 72861 and 73861: 4 A/Ds
Model 74861: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Wideband Digital Downconverters (4 or 8)
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to fₛ
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters (4 or 8)
Decimation Range: 2x to 1024x
LO Tuning Freq. Resolution: 32 bits, 0 to fₛ, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
On-board clock synthesizer

Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: LVDS I/O between the FPGA and J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862

Memory (1 or 2 banks)
Type: DDR4 SDRAM
Size: 5 GB or 10 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50°C
Storage Temp: −20° to 90°C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: −20° to 65°C
Storage Temp: −40° to 100°C
Relative Humidity: 0 to 95%, non-condensing

Size: 6U board 6.299 in x 9.173 in
(160.00 mm x 233.00 mm)
3U board 3.937 in x 6.299 in
(100.00 mm x 160.00 mm)

Ordering Information

Model Description
72862 4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U cPCI
73862 4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 3U cPCI
74862 8-Channel 200 MHz A/D with multiband DDCs and two Kintex UltraScale FPGAs - 6U cPCI

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS I/O between the FPGA and J2 connector, Model 73862; J3 connector, Model 72862; J3 and J5 connectors, Model 74862
- 702 Air cooled, Level L2
General Information

Models 72800, 73800 and 74800 are members of the Jade™ family of high-performance CompactPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a cPCI carrier board. Model 72800 is a 6U cPCI board while the Model 73800 is a 3U cPCI board; both are equipped with one Model 71800 XMC. Model 74800 is a 6U cPCI board with two XMC modules rather than one.

In addition to supporting PCI-X as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73800; J3 connector, Model 72800; J3 and J5 connectors, Model 74800.

Features

- High-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- 5 or 10 GB of DDR4 SDRAM
- Optional LVDS connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled version available
**PCI-X Interface**

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73800: 32 bits only.

**Memory Resources (1 or 2)**

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

**Specifications**

**Front Panel Digital I/O Interface**

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

**Field Programmable Gate Array (1 or 2)**

- **Standard**: Xilinx Kintex UltraScale XCKU035-2
- **Option -084**: Xilinx Kintex UltraScale XCKU060-2
- **Option -087**: Xilinx Kintex UltraScale XCKU115-2

**Custom I/O (1 or 2)**

- **Option -104**: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73800; J3 connector, Model 72800; J3 and J5 connectors, Model 74800

**Environmental**

- **Standard**: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- **Option -702**: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

**PCI-X Interface**

- **PCI-X Bus**: 32 or 64 bits at 33 or 66 MHz
  - Model 73800: 32 bits only

**Ordering Information**

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<td>74800</td>
<td>Kintex UltraScale FPGA Coprocessor - 6U cPCI</td>
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**Options:**
- **-084**: XCKU060-2 FPGA
- **-087**: XCKU115-2 FPGA
- **-104**: LVDS FPGA I/O
- **-702**: Air cooled, Level L2

Contact Pentek for complete specifications of rugged version.
**Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI**

**General Information**

These Bandit® models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded cPCI boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 7320 is a 3U cPCI board while Model 7220 is a 6U cPCI board; both provide two channels, while Model 7420 is a double-density 6U cPCI board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

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**Features**

- Accept RF signals from 400 MHz to 4000 MHz
- Accept RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

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**Model 7420**

**Model 7320**

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**Diagram:**

A diagram illustrating the Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI, showing the flow of signals from RF input to IF output, with options for input filter, quadrature mixers, and tuning control.

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**Pentek, Inc.**  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201.818-5900  Fax: 201.818-5904  Email: info@pentek.com  www.pentek.com
Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI

Specifications

RF Input
- Connector Type: SS/MC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

Phase Noise
- 1 kHz Offset: –90 dBc/Hz
- 100 kHz Offset: –110 dBc/Hz
- 1 MHz Offset: –130 dBc/Hz

Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SS/MC
- Reference Input Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave
- Reference Output Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  - (20 years): ±4.60 ppm

Phase Noise
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 KHz Offset: –148 dBc/Hz
- 10 KHz Offset: –154 dBc/Hz
- 100 KHz Offset: –155 dBc/Hz

IF Output
- Connector Type: SS/MC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI Interface
- PCI Bus: 32-bit, 66 MHz (supports 33 MHz), power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board

Ordering Information

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<td>Oven Controlled Reference Oscillator</td>
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<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
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<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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<td>Cobalt 78620</td>
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<td>Onyx 78761</td>
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<td>Jade 78821</td>
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<td>Jade 78841</td>
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<tr>
<td>Jade 78851</td>
<td>2-Channels 500 MHz A/D, DUC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - x8 PCIe</td>
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<td>Jade 78861</td>
<td>4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe</td>
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<td>8266</td>
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General Information

Model 78620 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78620 includes optional general-purpose and gigabit serial card edge connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78620 factory-installed functions include three A/D acquisition and a D/A waveform for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
A/D Conversion Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78620’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

PCI Express Interface

The Model 78620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference
- **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 78621 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78621 includes an optional general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
A/D Acquisition IP Modules

The 78621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*$f_s$/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s$/N.

Beamformer IP Core

In addition to the DDCs, the 78621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

D/A Waveform Playback IP Module

The Model 78621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily playback to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78621’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
### Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Digital Downconverters**
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

**Digital Interpolator**
- **Interpolation Range:** 2x to 65,36x in two stages of 2x to 256x

**Beamformer**
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Multiboard Summation Expansion:** 32-bit

**Front Panel Analog Signal Outputs**
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Clock Synthesizer Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Clock Synthesizer Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 in. x 7.13 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>78621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- **-062:** XC6VLX240T
- **-064:** XC6VSX315T
- **-104:** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-150:** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-160:** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155:** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165:** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

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<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
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</tbody>
</table>
General Information

Model 78624 is a member of the Cobalt® family of high-performance PCI Express boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 78624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 78624 digitizes two analog IF inputs using two 200 MHz 16-bit A/Ds. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 78624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory. DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation). The translated DUC outputs are directed to either of two summation blocks, each —

Features
- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/A
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8
associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

**Xilinx Virtex-6 FPGA**

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 78624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

**A/D Converters**

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

**Digital Downconverters**

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to 0.8\( f_s \)/\( N \), where \( N \) is the decimation setting and \( f_s \) is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s \)/\( N \).

**Input Gain Blocks**

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

**Receive DMA Controller**

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 78624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

**Transmit DMA Controller**

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 78624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

**Output Gain Blocks**

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

**Digital Upconverters**

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.
A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to $f_s$, where $f_s$ is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

**Summation Blocks**

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

**D/A Converters**

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78624’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**PCI Express Interface**

The Model 78624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

**Form Factor Adaptors**

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Quantity: 2
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: 34
- Decimation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >100 dB
- Phase Offset: 1 bit, 0 or 180 degrees
- FIR Filter: 18-bit coefficients
- Output: Complex, 16-bit I + 16-bit Q
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
- Quantity: 34
- Interpolation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- FIR Filter: 18-bit coefficients, 16-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Analog Output Channels: 2
- Type: Texas Instruments DAC5688
- Input Data Rate: 200 MHz max.
- Output Signal: Real
- Output Sampling Rate: 800 MHz max. with 4x interpolation
- Resolution: 16 bits

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Required: Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Standard:
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model 78624
- Dual-Channel 34-Signal Adaptive IF Relay - PCIe

Options:
- 064 XC6VSX315T (required)
- 730 2-slot heatsink

Model 8266
- PC Development System
  - See 8266 Datasheet for Options
Model 78630

1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

General Information

Model 78630 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 2 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
A/D Acquisition IP Module

The 78630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the A/D/Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GSPS, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7892 and Model 9192 Cobalt Synchronizers can drive multiple 78630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTT external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 78630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Model 78630

1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

PCI Express Interface
The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - A/D Converter:
    - Type: Texas Instruments ADS5400
    - Sampling Rate: 100 MHz to 1 GHz
    - Resolution: 12 bits
  - D/A Converter:
    - Type: Texas Instruments DAC5681Z
    - Input Data Rate: 1 GHz max.
    - Interpolation Filter: bypass, 2x or 4x
    - Output Sampling Rate: 1 GHz max.
    - Resolution: 16 bits

Front Panel Analog Signal Outputs
  - Output Type: Transformer-coupled, front panel female SSMC connectors
  - Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  - VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  - Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
  - Standard: Xilinx Virtex-6 XC6VLX130T-2
  - Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
  - Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
  - Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory
  - Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  - Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
  - PCI Express Bus: Gen.1: x4 or x8
    - Gen. 2: x4

Environmental
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.
  - Size: Half length PCIe card, 4.38 in. x 7.13 in.
Model 78640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

General Information

Model 78640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 78640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78640 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 78640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 78640s can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The 78640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
  Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
  Type: Texas Instruments ADC12D1800
  Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  Resolution: 12 bits
  Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector
Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
  Type: Front panel female SSMC connector
  Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
  Standard: Xilinx Virtex-6 XC6VLX130T-2
  Optional: Xilinx Virtex-6 XC6VLX240T-2 XC6VSX315T-2

Custom I/O
  Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
  Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
  PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

Environmental
  Operating Temp: 0° to 50° C
  Storage Temp: -20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model 78640
  1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

Options:

-002* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O through 68-pin ribbon cable connector
-105 Gigabit serial FPGA I/O through two 4X top edge connectors
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Model 8266
  PC Development System
  See 8266 Datasheet for Options
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - x8 PCIe

**General Information**

Model 78641 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78641 includes an optional connection to the Virtex-6 FPGA for custom I/O.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**Features**

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Module

The 78641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

Clocking and Synchronization

The 78641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 78641’s can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The 78640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

![DDC IP Cores Diagram](image-url)
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - x8 PCIe

**PCI Express Interface**

The Model 78641 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converter**

- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm

**Digital Downconverters**

- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources:** Front panel SSMC connector

**Sync Bus:** Multi-pin connectors, bus includes gate, reset and in and out ref clock

**External Trigger Input**

- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Xilinx Virtex-6 XC6VSX315T-2**

**Custom I/O**

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Memory:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>78641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - x8 PCIe</td>
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</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

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<table>
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<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
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</table>
**General Information**

Model 78650 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78650 includes optional general-purpose and gigabit serial card connectors for application-specific I/O protocols.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

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**Features**

- Complete radar and software interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

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[Diagram of Model 78650 showing connectivity and components]
A/D Acquisition IP Modules

The 78650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter.

Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tbody>
<tr>
<td>78650</td>
<td>Two 500 MHz A/Ds, one DUC, two 800 MHz D/As, with Virtex-6 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-155** Two 512 MB DDR3 SRAM Memory Banks (Banks 1 and 2)
- **-160** Two 512 MB DDR3 SRAM Memory Banks (Banks 3 and 4)
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-002** 400 MHz, 14-bit A/Ds
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-05** Gigabit serial FPGA I/O through 2x 4X top edge connectors
- **-06** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-105** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)

**Specifications**

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)

- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option 014)

- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

D/A Converters

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max.
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus:** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- **Type:** Front panel female SSMC connector, LVTTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- **Option -016:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -015:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen.1: x4 or x8
- **Gen. 2:** x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - x8 PCIe

General Information

Model 78651 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 78651 includes two A/Ds, two D/A and four banks of memory. It features native support for PCI Express Gen 2.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78651 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core.

The waveform playback IP module contains an interoplation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+

memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX family features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/A
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- PCI Express (Gen. 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multmodule synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Acquisition IP Modules**

The 78651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**Beamformer IP Core**

In addition to the DDCs, the 78651 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78651’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

**D/A Waveform Playback IP Module**

The Model 78651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78651’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer耦合, 前面板上的SMMC连接器
- Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +5 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option -104)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 131,072x
- and one fixed 2x stage
- LO Tuning Freq. Resolution: 32 bits, 0 to fs
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or I & Q with frequency translation
- Output Sampling Rate: 800 MHz max.
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x
- in two stages of 2x to 256x

Beamformer
- Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via a dual 4x connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
- Output: Transformer耦合, 前面板上的SMMC连接器
  - Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SMMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX240T-2
- Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- Option -150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI-Express Bus: Gen. 2: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 78660 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78660 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications that require large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments AD5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

**Memory**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Half length PCIe card, 4.38 in. x 7.13 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

**Model** | **Description**
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78660 | 4-Channel 200 MHz A/D with Virtex-6 FPGA - PCIe

**Options:**

- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-160** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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**Model** | **Description**
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8266 | PC Development System See 8266 Datasheet for Options
**General Information**

Model 78661 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78661 includes an optional general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
A/D Acquisition IP Modules

The 78661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Core

In addition to the DDCs, the 78661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage.
PCI Express Interface

The Model 78661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe Links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>78621</td>
<td>4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

Options:
-062  XCV6LX240T FPGA
-064  XCV6SX315T FPGA
-104  LVDS FPGA I/O through 68-pin ribbon cable connector
-150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6T6L4
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 65,536 in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to fs
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 1 & Q with 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synchronizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- Operating Temp: 0°C to 50°C
- Storage Temp: -20°C to 90°C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 78662 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of communications or radar systems. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78662 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 78662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable serial gigabit interfaces
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Modules

The 78662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of \( f_s/N \). Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleave that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.
Model 78662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters

- **Quantity:** Four 8-channel banks, one per acquisition module
- **Decimation Range:** 16 to 1024 in steps of 8 and 1024 to 1024 in steps of 64
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
- **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 in. x 7.13 in.

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Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<td>78662</td>
<td>4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - PCIe</td>
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</table>

Options:

- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model 8266 PC Development System

See 8266 Datasheet for Options
Model 78663 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 78663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 78663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

New! New! New! New! New!

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

SUPER CHANNEL ENGINE

PACKET GENERATOR

FIFO & LINKED-LIST DMA ENGINE

Pentek, Inc. One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 78663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 78663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

### Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

### Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

### PCI Express Interface

The Model 78663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 78663 and host.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank:** two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank:** 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing:** 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 kHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate f_s:** Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: -f_s/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +f_s/4 (+270.8333 kHz)
  - Fourth: +f_s/2 (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 x 7.13 in.

Ordering Information

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<td>8266</td>
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General Information

Model 78664 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution. The 78664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78664 includes an optional general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX4 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXTP FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Modules

The 78664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Core

In addition to the DDCs, the 78664 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each program is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78664’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 78664 supports fully the VITA 49.0 specification.

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Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201.818.5900  Fax: 201.818.5904  Email: info@pentek.com  www.pentek.com
**A/D Converter Stage**

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 7864’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78644 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 78664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe Links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VXCO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs, TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half length PCIe card, 4.38 in. x 7.13 in.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - x8 PCIe</td>
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Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O through 68-pin ribbon cable connector
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model 8266 PC Development System
See 8266 Datasheet for Options
Model 78670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe

General Information

Model 78670 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78670 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Pentek, Inc.
One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user-selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync, and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator).

In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7892 or 9192 Cobalt Synchronizers can drive multiple 78670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 78670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

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**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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**Specifications**

**D/A Converters**

- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**

- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer \( G = 0 \) to 15

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Input**

- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus**

- **Type:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**

- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Half length PCIe card, 4.38 in. x 7.13 in.
Model 78671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

General Information
Model 78671 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4x gigabit serial links from the FPGA on XMC P16 to two 4x gigabit serial connectors along the top edge of the PCIe board.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user-selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 78671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7892 or 9192 Cobalt Synchronizers can drive multiple 78671 µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The 78671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Model 78671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

PCI Express Interface

The Model 78671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

D/A Converters

- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Digital Interpolator

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs

- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input

- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus:

- **Type:** 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array:

- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

- **Type:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size:

- Half length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

**Model 78671**

- **Description:** 4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - x8 PCIe

**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX224T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

**Model 8266**

- **Description:** PC Development System See 8266 Datasheet for Options

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
**General Information**

Model 78690 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78690 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA to PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

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**Features**

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

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**CENTRAL TIMING GENERATOR**

Clock / Sync / Gate / PPS

![Diagram](image-url)
**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**A/D Clocking and Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

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**A/D Acquisition IP Modules**

The 78690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D Acquisition Modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom-user-installed IP within the FPGA.

**PCI Express Interface**

The Model 78690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Analog Signal Input**
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

**L-Band Tuner**
- **Type:** Maxim MAX2112
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:** where integer N = 19 to 251 and fractional F is a 20-bit binary value
- **PLL Reference:** Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain:** 0 to 15 dB, in 1 dB steps*
- **Baseband Low Pass Filter:** Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board timing generator/synthesizer

**A/D Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

**Timing Generator External Clock Input**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus:** 26-pin front panel connector LVPECL bus includes, clock/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4x gigabit serial links from the FPGA on XMC P16 to two 4x gigabit serial connectors along the top edge of the PCIe board

**Memory**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2 x4

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.
4-Channel SFP Transceiver PCIe Module for Cobalt Boards

General Information

Model 7809 is a PCIe module that provides gigabit serial transceiver network cable links for Pentek’s Cobalt® family of high performance 786xx PCIe boards based on the Xilinx Virtex-6 FPGA.

The 7809 and the Cobalt board are installed in adjacent slots in a PCIe motherboard or backplane and joined with a gigabit serial flex circuit cable.

The 7809 takes advantage of the small form-factor pluggable (SFP) or Mini-GBIC standard, supporting a variety of hot-pluggable transceiver modules for optical and copper network cables. Up to four modules can be installed.

Since the 7809 is protocol transparent, it is compatible with many protocols including Serial FPDP, PCIe, Xilinx Aurora, Serial-RapidIO, Gigabit Ethernet, SONET, Fibre Channel, and others.

The Cobalt Connection

The 786xx series PCIe Cobalt boards feature two optional 4X gigabit serial connectors along the top edge of the circuit board. These two 4X ports are wired directly to P16 of the XMC module.

The 7809 circuit board has one 4X gigabit serial connector along its top edge. A short flex circuit cable is installed between the 7809 4X connector and one of the two Cobalt 4X connectors.

This provides a full-duplex 4X gigabit serial path between the modules that can operate at serial bit rates to 5 GHz. A second 7809 can be installed adjacent to the Cobalt board to support a second 4X transceiver link.

Each of the four gigabit serial links within a 4X port consists of a transmit pair and a receive pair connected to one SFP module through an equalizer circuit to improve transceiver performance. The Virtex-6 FPGA in the Cobalt module is used to implement the required protocol engine for the P16 4X links to the 7809.

Some Cobalt boards (such as the 78621 and 78661) are equipped with factory-installed FPGA IP supporting Xilinx Aurora links for cascade beamforming summation across multiple boards.

Pentek’s GateFlow FPGA Design Kit allows users to implement custom protocols for other applications. GateFlow is compatible with the Xilinx ISE Foundation Tool Suite, and includes a complete project file and VHDL source code.

SFP Modules

SFP transceiver modules support a variety of different transmitter and receiver types. These modules simply plug into the SFP sockets so they can be easily installed or replaced by users.

Users can choose the appropriate transceiver for each link to support the required distance and data rates. Both single-mode and multi-mode optical fibre devices are available for cable interconnection distances up to 550 m and 10 km, respectively.

Pentek offers the 7809 with options for either two or four 850 nm multi-mode fibre optical SFP modules installed.

Each 7809 is supplied with the gigabit serial flex circuit cable assembly for connection to a suitably equipped 786xx series PCIe Cobalt module.

Features

- Compatible with Pentek 786xx PCI Express Cobalt boards
- Extends range of gigabit serial I/O links
- Four SFP modules drive cable lengths up to 10 km
- Support for both optical and copper cables
- Single-mode and multi-mode fibre optical
- Data rates to 5 Gbits/sec
- Payload data rates to 500 MB/sec for each cable

Ordering Information

Model Description
7809 4-Channel SFP Transceiver PCIe Module

Options:
-002 Two 850 nm multi-mode fiber optical channel SFPs (500 m distance)
-004 Four 850 nm multi-mode fiber optical channel SFPs (500 m distance)

Contact Pentek for availability of other interfaces

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
General Information

Model 78720 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78720 includes optional general-purpose and gigabit-serial card edge connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA provides access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78720 factory-installed applications include three A/D acquisition and a D/A waveform transfer, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com

www.pentek.com
### A/D Acquisition IP Modules

The 78720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### D/A Waveform Playback IP Module

The Model 78720 factory-installed functions include a sophisticated D/A Waveform Playback IP Module. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

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#### GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIE interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

#### A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

#### Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

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![Diagram](diagram.png)
**Memory Resources**

The 78720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s FPGA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**Model 78720**

- When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

  If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

**PCI Express Interface**

The Model 78720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**D/A Converters**

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max.
- **Resolution:** 16 bits

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Ordering Information**

**Model**

| 78720 | 3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - PCIe |

**Options:**

- **-073** XC7VX330T-2 FPGA
- **-076** XC7VX690T-2 FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors

**Model**

| 8266 | PC Development System See 8266 Datasheet for Options |
**Model 78721**

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

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**General Information**

Model 78721 is a member of the Onyx® family of high performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/A ands and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78721 includes an optional connection to the Virtex-7 FPGA for custom I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or replace the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decryption, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/A
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
**A/D Acquisition IP Modules**

The 78721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A/ A/D Loopback Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**Beamformer IP Core**

In addition to the DDCs, the 78721 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module for reading over the PCIe. For larger systems, multiple 78721’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

**D/A Waveform Playback IP Module**

The Model 78721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.
Pentek, Inc.  One Park Way  ●  Upper Saddle River  ●  New Jersey 07458  
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com  ●  www.pentek.com

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe

Model 78721

- Memory Resources
  The 78721 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

- PCI Express Interface
  The Model 78721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

- Specifications
  Front Panel Analog Signal Inputs
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: ±8 dBm into 50 ohms (±3 dB Passband: 300 kHz to 700 MHz)
  A/D Converters
  - Type: Texas Instruments ADS5485
  - Sampling Rate: 10 MHz to 200 MHz
  - Resolution: 16 bits
  Digital Downconverters
  - Quantity: Three channels
  - Decimation Range: 2x to 65,536x in two stages of 2x to 256x
  - LO Tuning Freq. Resolution: 32 bits, 0 to f_s
  - LO SFDR: >120 dB
  - Phase Offset Resolution: 32 bits, 0 to 360 degrees
  - FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
  - Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
  - D/A Converters
    - Type: Texas Instruments DAC5688
    - Input Data Rate: 250 MHz max.
    - Output IF: DC to 400 MHz max.
    - Output Signal: 2-channel real or 1-channel with frequency translation
    - Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
    - Resolution: 16 bits
  - Digital Interpolator
    - Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Model 8266

- The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<th>Description</th>
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<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - x8 PCIe</td>
<td>-076  XCV690T-2 FPGA  -104  LVDS FPGA I/O through 68-pin ribbon cable connector</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

- PC Development System
  See 8266 Datasheet for Options

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 78730 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78730 includes optional general-purpose and gigabit serial card connectors for application specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

1 GHz A/D and 1 GHz D/A with Virtex-7 FPGA - x8 PCIe

Model 78730

Pentek, Inc.
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
**A/D Acquisition IP Module**

The 78730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 78730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

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**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without resetting the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The 78730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

**D/A Converter Stage**

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7892 and Model 9192 Cobalt Synchronizers can drive multiple 78730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 78730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Model 78741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

**General Information**

Model 78741 is a member of the Onyx family of high-performance PCIe modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78741 includes an optional connection to the Virtex-7 FPGA for custom 1/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

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**Features**

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- μSnc clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Module

The 78741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in transient mode or for storing data in persistent capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-Pcie configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
Memory Resources

The 78471 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tr>
<td>71741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - x8 PCIe</td>
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Options:
- 073   XCV7X330T-2 FPGA
- 076   XCV7X690T-2 FPGA
- 079   LVDS FPGA I/O through 68-pin ribbon cable connector
- 104   Gigabit serial FPGA I/O through two 4X top edge connectors

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78471 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

PCI Express Interface

The Model 78741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Clocking and Synchronization

The 78471 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 78471’s can be synchronized with a simple cable. For larger systems, multiple 78471’s can be synchronized using the Model 7892 high-speed sync board to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters

Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz; two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x; two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half-length PCIe card, 4.38 in. x 7.13 in.
Model 78751 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connections to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCIe Express Gen. 3 as a native interface, the Model 78751 includes a general purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA to two gigabit serial connectors along the top edge of the board.
two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the $80\%$ output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**D/A Waveform Playback IP Module**

The Model 78751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the D/A Waveforms stored in on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Orxy architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 ms on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course.
Model 78751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - x8 PCIe

➤ of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 71751’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
Specifications

Front Panel Analog Signal Inputs
- Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option -014)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
- Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- Type: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8266 Ordering Information

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<td>PC Development System See 8266 Datasheet for Options</td>
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Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.
Model 78760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

General Information

Model 78760 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78760 includes optional general-purpose and gigabit-serial connectors for application-specific I/O protocols.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Advanced reconfigurability features
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an input.
Model 78760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

➤ external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78760’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: ±8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer
Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to ±10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half length PCIe card, 4.38 in. x 7.13 in.
**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multicomponent synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

**General Information**

Model 78761 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78761 includes an optional connection to the Virtex-7 FPGA for custom I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 78761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
A/D Acquisition IP Modules

The 78761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit 1+24-bit Q or 16-bit 1+16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Core

In addition to the DDCs, the 78761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 78761’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from...
Model 78761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 78761 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.
4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- **Option -104:** Connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

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<td>4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - x8 PCIe</td>
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Options:
- **-076** XC7VX690T-2 FPGA
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector

<table>
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General Information

Model 78791 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 78791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 78791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decryption, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA to two gigabit serial connectors along the top edge of the board.
A/D Acquisition IP Modules

The 78791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.

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**A/D Acquisition IP Modules**

Model 78791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) downconverting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re- loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converters and DDCs**

The two analog tuner outputs are digitized by two Texas Inst. AD5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

**A/D Clocking & Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

**PCI Express Interface**

The Model 78791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
## Specifications

**Front Panel Analog Signal Input**
- Connector: Front panel female SSMC
- Impedance: 50 ohms

**L-Band Tuner**
- Type: Maxim MAX2121
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: $-97 \text{ dBc/Hz at 10 kHz}$
- Fractional-N PLL Synthesizer:
  - $f_{\text{VCO}} = (N/F) \times f_{\text{REF}}$
  - where integer $N$ = 19 to 251 and fractional $F$ is a 20-bit binary value
- PLL Reference ($f_{\text{REF}}$): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
- Usable Full-Scale Input Range: $-50 \text{ dBm to } +10 \text{ dBm}$
- Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

**A/D Converters**
- Type: Texas Instruments ADS5463
- Sampling Rate: 10 MHz to 500 MHz
- Resolution: 12 bits
- Option -014: 400 MHz, 14-bit A/Ds

**Sample Clock Sources**: On-board timing generator/synthesizer

**A/D Clock Synthesizer**
- Clock Source: Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VXCO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

**Timing Generator External Clock Input**
- Type: Front panel female SSMC connector, sine wave, 0 to $+10 \text{ dBm}$, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus**: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- Quantity: 2
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- Option -104: Connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- Option -105: Connects two 4X gigabit serial links from the FPGA to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: −20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 78131 is a member of the Jade family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through:
A/D Acquisition IP Modules

The 78131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a composite output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMX connectors with transformer-coupling into four Texas Instruments ADS421B69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 78131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 78131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - PCIe

PCI Express Interface

The Model 78131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters

- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to 360 degrees
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

TIMING BUS: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- **Option -104** connects 24 pairs of LVDS signals from the FPGA to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105** connects one 8X gigabit serial link from the FPGA to an 8X gigabit serial connector along the top edge of the PCIe board.

Memory

- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

- **Standard:** L0 (air cooled)
  - **Operating Temp.:** 0° to 50° C
  - **Storage Temp.:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing

- **Option -702:** L2 (air cooled)
  - **Operating Temp.:** -20° to 65° C
  - **Storage Temp.:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
Model 78132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - x8 PCIe

New!

General Information
Model 78132 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available

Supports Xilinx Kintex UltraScale FPGAs
- Complete multi-board clock and sync section and a large DDR4 memory
- In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

General Information
- Model 78132 is a member of the Jade™ family of high-performance PCIe boards.
- The Jade architecture embodies a streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today.
- Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.
- The 78132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.
- It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
- Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.
- Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.
- Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
- For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA
- The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight wideband DDCs (digital downconverters)
- 64 multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available
A/D Acquisition IP Modules

The 78132 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible down-conversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications.
PCI Express Interface
The Model 78132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Eight banks, 8 channels per bank
Decimation Range: 16x to 1024x in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \), independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female MMCX connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector providing 8X serial links to the FPGA

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Model 78132
8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VXI chassis (Model 8267) or a 6U VXI chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.
Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

**General Information**

Model 78141 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/A and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Module
The 78141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module
The Model 78141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz. The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage
A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources
The 78141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface
The Model 78141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization
The 78141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7892 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz
Resolution: 14 bits
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O
Option -105 (only available with option -084 or -087): provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: PCIe card 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

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<td>78141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe</td>
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Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
Model 78821 is a member of the Jade family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 78821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 78821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.
The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

A/D Acquisition IP Modules

The 78821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a single A/D module.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$. The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.
Model 78821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78821’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model Description
78821 3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

Options:
-084 XCKU060-2 FPGA
-087 XCKU115-2 FPGA
-104 LVDS FPGA I/O
-105 Gigabit serial FPGA I/O
-702 Air cooled, Level L2

Contact Pentek for complete specifications of rugged versions
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - PCIe

**General Information**

Model 78841 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, etc.
A/D Acquisition IP Module
The 78841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores
Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

KINTEX ULTRASCALE FPGA DATAFLOW DETAIL

Two-Channel mode shown. Programmable decimation of 4, or 8 to 256 in steps of 8 available.

From A/D
From A/D

INPUT MUX

TEST SIGNAL GENERATOR

SDRAM DDR4

Gigabit Serial I/O

PCIe

(supports user installed IP)
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

**Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

**Model 78841**

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - PCIe

**Memory Resources**

The 78861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

**PCI Express Interface**

The Model 78841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Clocking and Synchronization**

The 78841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 78841’s can be synchronized with a simple cable. For larger systems, multiple 78841’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **A/D Converter**
  - **Type:** Texas Instruments ADC12D1800
  - **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  - **Resolution:** 12 bits
  - **Input Bandwidth:** Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  - **Full Scale Input Level:** May be trimmed from +2 dBm to +4 dBm with a 15-bit integer

**Digital Downconverters**

- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz; two-channel mode: 1.8 GHz
- **Single-channel mode:** Decimation can be programmed to 8 or 16 to 512 in steps of 16
- **Dual-channel mode:** Decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
- **Either mode:** The DDC can be bypassed completely

- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Field Programmable Gate Array**

- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**

- **Option -104:** Installs a connector with 24 LVDS pairs to the FPGA
- **Option -105:** Installs a connector for one 8X gigabit serial link to the FPGA

**Memory**

- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**

- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50°C
  - **Storage Temp:** -20° to 90°C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** 0° to 65°C
  - **Storage Temp:** -40° to 100°C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** Half-length PCIe card, 4.38 in. x 7.13 in.
Model 78851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

General Information

Model 78851 is a member of the Jade family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78851 factory-installed functions include two A/D acquisition and a waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 78851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- Ruggedized version available
Model 78851

### A/D Acquisition IP Modules

The 78851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### D/A Waveform Playback IP Module

The Model 78851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

### DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output band-

### Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

### A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.
Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - x8 PCIe

**Specifications**

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 65,536x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **Default Filter Set:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Input Data Rate:** 800 MHz max.
- **Output Sampling Rate:** 2x to 262,144x
- **Interpolation Range:** 2x to 262,144x

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output IF:** 2x to 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x
- **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- **Option -105** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing

**Option -702:** L2 (air cooled)
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** -40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing

**Size:** PCIe card 4.380 in x 7.130 in (111.25 mm x 181.10 mm)
Model 78861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - x8 PCIe

General Information

Model 78861 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**A/D Acquisition IP Modules**

The 78861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a D/A channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \),

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
PCI Express Interface

The Model 78861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters

- Quantity: Four channels
- Decimation Range: 2x to 32,768x in three stages of 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources

- On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers

- External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

- Type: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: Installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
- Option -105: Provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory

- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size: PCIe card, 4.380 in x 7.130 in (111.25 mm x 181.10 mm)
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

General Information

Model 78862 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 78862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and
- 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized version available
The 78862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**XIlinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 78862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - PCIe

- **PCI Express Interface**
  The Model 78862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

- **Specifications**
  - **Front Panel Analog Signal Inputs**
    - **Input Type:** Transformer-coupled, front panel female SSMC connectors
    - **Transformer Type:** Coil Craft WBC4-6TLB
    - **Full Scale Input:** 3.3 V
    - **Passband:** 300 kHz to 700 MHz
  - **A/D Converters**
    - **Type:** Texas Instruments ADS5485
    - **Sampling Rate:** 10 MHz to 200 MHz
    - **Resolution:** 16 bits
  - **Wideband Digital Downconverters**
    - **Quantity:** Four channels
    - **Decimation Range:** 2x to 32x
    - **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
    - **LO SFDR:** >120 dB
    - **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
    - **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
    - **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
  - **Multiband Digital Downconverters**
    - **Quantity:** Four banks, 8 channels per bank
    - **Decimation Range:** 2x to 1024x
    - **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s, independent tuning for each channel
    - **LO SFDR:** >120 dB
    - **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
    - **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
    - **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
  - **Sample Clock Sources:** On-board clock synthesizer
  - **Clock Synthesizer**
    - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
    - **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
    - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
  - **External Clock**
    - **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
    - **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
  - **Field Programmable Gate Array**
    - **Standard:** Xilinx Kintex UltraScale XCKU035-2
    - **Option -084:** Xilinx Kintex UltraScale XCKU060-2
    - **Option -087:** Xilinx Kintex UltraScale XCKU115-2
  - **Custom I/O**
    - **Option -104:** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
    - **Option -105:** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.
  - **Memory**
    - **Type:** DDR4 SDRAM
    - **Size:** 5 GB
    - **Speed:** 1200 MHz (2400 MHz DDR)
  - **PCI-Express Interface**
    - **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
  - **Environmental**
    - **Standard:** L0 (air cooled)
    - **Operating Temp:** 0° to 50°C
    - **Storage Temp:** -20° to 90°C
    - **Relative Humidity:** 0 to 95%, non-condensing
    - **Option -702:** L2 (air cooled)
    - **Operating Temp:** -20° to 65°C
    - **Storage Temp:** -40° to 100°C
    - **Relative Humidity:** 0 to 95%, non-condensing
    - **Size:** PCIe card, 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78862</td>
<td>4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

Options:
- 084: XCKU060-2 FPGA
- 087: XCKU115-2 FPGA
- 104: LVDS FPGA I/O through 68-pin ribbon cable connector
- 105: Gigabit serial FPGA I/O through serial connector
- 702: Air cooled, Level L2
Model 78800 is a member of the Jade family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

### The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The 78800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

### Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

### Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides an 8X gigabit link between the FPGA and a serial connector to support serial protocols.

### Front Panel Digital I/O Interface

The 78800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path. ➤
Kintex UltraScale FPGA Coprocessor- x8 PCIe

► PCI Express Interface

The Model 78800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 78800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Specifications

Front Panel Digital I/O

Connector Type: 80-pin connector, mates to a ribbon cable connector
Signal Quantity: 38 pairs
Signal Type: LVDS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.
Option -105 provides an 8X gigabit link between the FPGA and a serial connector to support serial protocols.

Memory

Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: PCIe card 4.375 in x 8.125 in (111.13 mm x 206.38 mm)

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Ordering Information

Model Description
78800 Kintex UltraScale FPGA Coprocessor - x8 PCIe

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
General Information
The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level
The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options
An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers
The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy

Tuning Accuracy
The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock
In addition to accepting a 10 MHz reference signal on the front panel, the 7820 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output
Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Two-Channel Analog RF Wideband Downconverter - PCIe

Specifications

RF Input
- Connector Type: SSINC
- Input Impedance: 50 ohms
- Input Level Range: –60 dBm to –20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

Phase Noise
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SSINC
- Input/Output Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave
- Reference Output Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance (20 years): ±4.60 ppm

Phase Noise
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 kHz Offset: –148 dBc/Hz
- 10 kHz Offset: –154 dBc/Hz
- 100 kHz Offset: –155 dBc/Hz

IF Output
- Connector Type: SSINC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI-Express Interface
- PCI Express Bus: x4 or x8, power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>7820</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - PCIe</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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</table>
Model 8266
PC Development System for PCIe Cobalt, Onyx and Flexor Boards

General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx®, and Flexor™ PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19” 4U rackmount chassis that is 21” deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19” W x 21” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5% to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model 8266
PC Development System for PCIe Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.
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<th>MODEL</th>
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<td>5308</td>
<td>Front Panel x8 PCI Express Adapter - 3U VPX</td>
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<tr>
<td>Cobalt 53620</td>
<td>3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53624</td>
<td>Dual-Channel, 34-Signal Adaptive IF Relay - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 53640</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53641</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53650</td>
<td>Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53661</td>
<td>4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 53662</td>
<td>4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 53663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 3U VPX</td>
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<tr>
<td>Cobalt 53664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 53670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 53671</td>
<td>4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 53690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53720</td>
<td>3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53721</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53740</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53750</td>
<td>2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 53760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 53761</td>
<td>4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 53791</td>
<td>L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Jade 53130</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX</td>
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<tr>
<td>Jade 53132</td>
<td>8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX</td>
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<tr>
<td>Jade 53141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - 3U VPX</td>
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<tr>
<td>Jade 53821</td>
<td>3-Channel 200 MHz A/D, DDC, DUC 2-Channel 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 53841</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 53851</td>
<td>2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 53861</td>
<td>4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 53862</td>
<td>4-Channel 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 53800</td>
<td>Kintex UltraScale FPGA Coprocessor - 3U VPX Format 1</td>
</tr>
<tr>
<td>8267</td>
<td>3U VPX Development System for Cobalt, Onyx, Flexor, and Jade boards</td>
</tr>
</tbody>
</table>

Customer Information

RADAR & SDR I/O - PMC/XMC
RADAR & SDR I/O - CompactPCI
RADAR & SDR I/O - x8 PCI Express
RADAR & SDR I/O - AMC
RADAR & SDR I/O - 3U VPX - FORMAT 2
RADAR & SDR I/O - 6U VPX
RADAR & SDR I/O - FMC

Last updated March 2018
**General Information**

Model 53800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The 53800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

**Front Panel Digital I/O Interface**

The 53800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

---

**Features**

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
**Model 53800**

**Kintex UltraScale FPGA Coprocessor- 3U VPX**

> **Interfaces and Memory**

The Model 53800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the FPGA. The 53800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

**Crossbar Switch**

The 53800 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable input equalization and output pre-emphasis settings enable optimization.

**SPARK Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53800</td>
<td>Kintex UltraScale FPGA Coprocessor - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

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**Specifications**

**Front Panel Digital I/O**
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

**Field Programmable Gate Array**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104** connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

**Memory**
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**
- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Option -702:** L2 (air cooled)
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Option -713:** L3 (conduction cooled)
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Relative Humidity in all options:** 0 to 95%, non-condensing

**Size:** 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
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<tbody>
<tr>
<td>52xxx</td>
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<tr>
<td>Form Factor</td>
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<td># of XMCs</td>
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<tr>
<td>Crossbar Switch</td>
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<td>PCIe path</td>
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<tr>
<td>Option -104 path</td>
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<td>Option -105 path</td>
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<tr>
<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
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</tbody>
</table>

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**Kintex UltraScale FPGA Resources**

![Kintex UltraScale FPGA Resources](image)

**Kintex UltraScale FPGA Dataflow Detail**

![Kintex UltraScale FPGA Dataflow Detail](image)

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
General Information

Model 5308 is a front panel PCI Express adapter for 3U VPX systems. It provides a convenient interface from a 3U VPX system to an external host computer, to simplify development.

The 5308 features built-in support for PCI Express (PCIe) Gen. 2 over the 3U VPX backplane. A unique fabric-transparent crossbar switch configuration allows selection of the desired VPX-P1 port.

Front Panel Connection

The 5308 provides a front panel interface to the 3U VPX system for connection to a host computer. It supports x4 or x8 PCIe protocol in compliance with PCI-SIG PCI Express® External Cabling 1.0 Specification. It can also be used to connect to an additional VPX system when ordered with Cascade Mode (option -002).

Model 5308 contains built-in PCI Express ReDriver™ circuitry. This circuitry provides signal conditioning that allows the user to correct for signal loss or data errors due to cable length.

PC Connection

The most common use for Model 5308 is for connection to an external host computer. In order to make this connection, the PC requires a PCIe host adapter which is also compliant to PCI-SIGPCI Express External Cabling 1.0 Specification. Adapters supporting either PCIe x8 Gen. 1 or Gen. 2 are available from Pentek under Model 4235.

Fabric-Transparent Crossbar Switch

Two ports from the front panel PCI Express connector are attached to a Fabric-Transparent Crossbar switch. This switch bridges numerous interfaces on the board using gigabit serial data paths with no latency. This allows the user to select the desired port on VPX-P1.

Data paths can be selected as single (x1) lanes, or groups of four lanes (x4). Programmable signal input equalization and output pre-emphasis settings enable optimization. A USB interface is provided for switch programming, and 4 MB onboard FLASH memory allows storage of up to 16 user configurations. Several useful configurations are pre-installed at the factory.

PCI Express Switch

The 5308 includes a multiport PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the fabric-transparent crossbar switch. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Data to or from the panel cable can be selected as x4 or x8 width. Both PCIe Gen. 1 and Gen. 2 are supported.

3U VPX Interface

The 5308 provides full-duplex links to the VPX P1 connector, each capable of peak rates up to 1 gigabyte per sec. Four sets of x4 links support PCI Express.

Features

- Front Panel x8 PCI Express connection to host PC
- 3U VPX form factor provides a compact, rugged platform
- Cascade mode provides connection to an additional VPX system
- Compatible with several VITA standards including:
  - VITA-46 (VPX Baseline Standard)
  - VITA-48 (VPX REDI)
  - VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Ordering Information

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<thead>
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<th>Description</th>
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</thead>
<tbody>
<tr>
<td>5308</td>
<td>Front Panel x8 PCI Express Adapter - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

-001 Host Adapter Mode (for connection to external host computer)
-002 Cascade Mode (for connection to additional VPX system)
-703 Level L3 Conduction-Cooled Version

Accessories:

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>4235</td>
<td>PCI Express x8 Host Card for PC</td>
</tr>
<tr>
<td>2180</td>
<td>PCI Express x8 Cable</td>
</tr>
</tbody>
</table>

*Total of 24 lanes can be configured for x1, x4, x8 or x16 widths
Model 53620

3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-6 FPGA - 3U VPX

General Information
Model 53620 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53620 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board’s analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Three 200 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing within the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53620’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 53620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
PCI Express Interface

The Model 53620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tbody>
<tr>
<td>53620</td>
<td>3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 104 LVDS FPGA I/O to VPX P2
- 105 Gigabit serial FPGA I/O to VPX P1
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +8 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

A/D Converters

- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

D/A Converters

- **Type**: Texas Instruments DAC5688
- **Input Data Rate**: 250 MHz max.
- **Output IF**: DC to 400 MHz max.
- **Output Signal**: 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate**: 800 MHz max. with interpolation
- **Resolution**: 16 bits

Front Panel Analog Signal Outputs

- **Output Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<td>Option -104 path</td>
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<tr>
<td>Option -105 path</td>
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<tr>
<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

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Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

General Information

Model 53621 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53621 includes three A/Ds, one upconverter, two D/A and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/A
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Optional LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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A/D Acquisition IP Modules

The 53621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be program-med from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Core

In addition to the DDCs, the 53621 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53621’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
Model 53621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage
The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.
The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.
When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.
If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.
Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53621’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 53621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.
In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 53621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch
The 53621 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.
Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits ➤

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www.pentek.com
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U XMC</td>
</tr>
</tbody>
</table>

Options:

- 062  XC6VLX240T FPGA
- 064  XC6VXSX315T FPGA
- 104  LVDS FPGA I/O to VPX P2
- 150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Digital Downconverters

- Quantity: Three channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to f<sub>o</sub>
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator

- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer

- Summation: Three channels on-board, multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One channel in and one channel out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs

- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources:

- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus:
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental

- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
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<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td></td>
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<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
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<td>PCIe Path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<td>Two x4 or one x8 on VPX P1</td>
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<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  www.pentek.com
Model 53624 is a member of the Cobalt\textsuperscript{a} family of high-performance 3U OpenVPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 53624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

### Adaptive Relay Input Overview

The Model 53624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) and 34 DUCs (digital upconverters) are independently enabled or disabled, and any signal within each IF band can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. 

Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

### Adaptive Relay Output Overview

The Model 53624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation). The translated DUC outputs are directed to either of two summation blocks,
each associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 53624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to 0.8\( f_s / N \), where \( N \) is the decimation setting and \( f_s \) is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 53624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 53624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.
Model 53624

Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to \( f_s \) where \( f_s \) is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

**Summation Blocks**

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

**D/A Converters**

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to \( x4 \) mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53624’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**PCI Express Interface**

The Model 53624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

**Fabric-Transparent Crossbar Switch**

The 53624 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

**Form Factor Adaptors**

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.

**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Quantity:** Two
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<td>53624</td>
<td>Dual-Channel 34-Signal Adaptive IF Relay - 3U OpenVPX</td>
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</tbody>
</table>

Options:
-064 [XC6VSX315T (required)]
-702 L2 (air cooled)
-712 L2 (conduction cooled)
-730 2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

Development System
See 8267 Datasheet for Options

SPARK Development Systems

Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

- Digital Downconverters
  - Quantity: 34
  - Decimation Range: 512 to 8192, in steps of 8
  - LO Tuning Freq. Resolution: 32 bits, 0 to f_s
  - LO SFDR: >100 dB
  - Phase Offset: 1 bit, 0 or 180 degrees
  - FIR Filter: 18-bit coefficients
  - Output: Complex, 16-bit I + 16-bit Q
  - Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- Input Gain Blocks
  - Quantity: 34
  - Data: Complex, 16-bit I + 16-bit Q
  - Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

- Output Gain Blocks
  - Quantity: 34
  - Data: Complex, 16-bit I + 16-bit Q
  - Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

- Digital Upconverters
  - Quantity: 34
  - Interpolation Range: 512 to 8192, in steps of 8
  - LO Tuning Freq. Resolution: 32 bits, 0 to f_s
  - LO SFDR: >120 dB
  - FIR Filter: 18-bit coefficients, 16-bit output
  - Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- D/A Converters
  - Analog Output Channels: 2
  - Type: Texas Instruments DAC5688
  - Input Data Rate: 200 MHz max.
  - Output Signal: Real
  - Output Sampling Rate: 800 MHz max.
  - with 4x interpolation
  - Resolution: 16 bits

- Front Panel Analog Signal Outputs
  - Output: Transformer-coupled, front panel female SSMC connectors
  - Transformer: Coil Craft WBC4-6TTLB
  - Full Scale Output: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

- Sample Clock Sources
  - On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

- Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

- Clock Dividers
  - External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

- External Clock
  - Type: Front panel female SSMC connector
  - Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- Timing Bus
  - 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate trigger and sync/PPS inputs

- Field Programmable Gate Array
  - Required: Xilinx Virtex-6 XC6VSX315T

- PCI-Express Interface
  - PCI Express Bus: Gen. 1: x4 or x8

- Environmental
  - Standard:
    - Operating Temp: 0° to 50° C
    - Storage Temp: -20° to 90° C
    - Relative Humidity: 0 to 95%, non-cond.
  - Option 702 L2 Extended Temp (air-cooled):
    - Operating Temp: -20° to 65° C
    - Storage Temp: -40° to 100° C
    - Relative Humidity: 0 to 95%, non-cond.
  - Option 712 L2 Extended Temp (conduction-cooled):
    - Operating Temp: -20° to 65° C
    - Storage Temp: -40° to 100° C
    - Relative Humidity: 0 to 95%, non-cond.

- Size: Standard 3U VPX board, 100 x 160 mm (3.937 x 6.299 in.)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
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<tbody>
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<tr>
<td>Crossbar Switch</td>
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<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
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<td>Option 104 path</td>
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<td>Option 105 path</td>
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<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
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Model 53630

**1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX**

### General Information

Model 53630 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

### The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Module

The 53630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Converter Stage

The 53630 features a D/A Converter Stage with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

The 53630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

Memory Resources

The Pentek Model 5392 and Model 9192 Cobalt Synchronizers can drive multiple 53630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX</td>
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<th>Options</th>
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<td>-2 FPGA speed grade</td>
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<td>-062</td>
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<td>-064</td>
<td>XC6VSX315T FPGA</td>
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<td>-104</td>
<td>LVDS FPGA I/O to VPX P1</td>
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<td>-105</td>
<td>Gigabit serial FPGA I/O to</td>
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<td>VPX P1</td>
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<tr>
<td>-150</td>
<td>Two 8 MB QDRII+ SRAM Memory</td>
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<td>Two 512 MB DDR3 SDRAM Memory</td>
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<td></td>
<td>Banks (3 and 4)</td>
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</table>

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267 VPX Development System. See 8267 Datasheet for Options

PCI Express Interface

The Model 53630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53630 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

- **A/D Converter**
  - Type: Texas Instruments ADS5400
  - Sampling Rate: 100 MHz to 1 GHz
  - Resolution: 12 bits
- **D/A Converter**
  - Type: Texas Instruments DAC5681Z
  - Input Rate: 1 GHz max.
  - Interpolation Filter: bypass, 2x or 4x
  - Output Sampling Rate: 1 GHz max.
  - Resolution: 16 bits

Front Panel Analog Signal Outputs

- **Output Type**: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources:

- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- **Clock Source**: Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus:

- 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

- **Type**: Front panel female SSMC connector, LVTTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- **Option -104**: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105**: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

- **Option 150**: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165**: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus**: Gen.1: x4 or x8; Gen 2: x4

Environmental

- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
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</tr>
</tbody>
</table>
Model 53640 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

General Information

Model 53640 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**Clocking and Synchronization**

The 53640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 53640’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

**Memory Resources**

The 53640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 53640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Fabric-Transparent Crossbar Switch**

The 53640 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **A/D Converter**
  - **Type:** Texas Instruments ADC12D1800
  - **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  - **Resolution:** 12 bits
  - **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  - **Full Scale Input:** +2 dBm to +4 dBm, programmable

**Sample Clock Sources:** Front panel SSMC connector

**Sync Bus:** Multi-pin connectors, bus includes gate, reset and in and out reference clock

**External Trigger Input**

- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1or Gen. 2: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
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<td>One XMC</td>
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<td># of XMCs</td>
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<td>Crossbar Switch</td>
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<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<td>PCIe width</td>
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<td>x4</td>
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<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
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</tbody>
</table>

**Ordering Information**

**Model 53640**

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VXSX315T FPGA
- **-104** LVDS FPGA I/O to VPX P2
- **-105** Gigabit serial FPGA I/O to VPX P1
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

**Model 8267**

VCX Development System. See 8267 Datasheet for Options
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

**General Information**

Model 53641 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53641 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources. ➤

**Features**

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programmable one- or two-channel DDC (Digital Downconverter)
- PCI Express (Gen. 1 & 2) interface, up to x8
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX System Specification)
- Ruggedized and conduction-cooled versions available
Model 53641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Clocking and Synchronization

The 53641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 53641’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 53641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

A/D Acquisition IP Module

The 53641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8 f_s / N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s / N.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

PCI Express Interface

The Model 53641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53641 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters

Modes: One or two channels, programmable

Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x

LO Tuning Freq. Resolution: 32 bits, 0 to f_s

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multipin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input

Type: Front panel female SSMC connector, TTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Xilinx Virtex-6 XC6VSX315T-2

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Form Factor</td>
<td>3U VPX</td>
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<td># of XMCs</td>
<td>One XMC</td>
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</tr>
<tr>
<td>Crossbar Switch</td>
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Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
---|---
53641 | 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

Options:
-002* | -2 FPGA speed grade
-064* | XC6VSX315T FPGA
-104 | LVDS FPGA I/O to VPX P2
-155* | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions
Model 53650 COTS (left) and rugged version

**General Information**

Model 53650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53650 includes two A/Ds, one DUC (digital upconverter), two D/A and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤
A/D Acquisition IP Modules

The 53650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.
PCI Express Interface
The Model 53650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tbody>
<tr>
<td>53650</td>
<td>Two 500 MHz A/Ds, one DUC, Two 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
-002*  2 FPGA speed grade
-014  400 MHz, 14-bit A/Ds
-062  XC6VLX240T FPGA
-064  XC6VSX315T FPGA
-104  LVDS FPGA I/O to VPX P1
-105  Gigabit serial FPGA I/O to VPX P1
-150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
*This option is always required

Specifications

Front Panel Analog Signal Outputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz
- Resolution: 16 bits

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option 014)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz, max.
- Output IF: DC to 400 MHz, max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz, max.
- with interpolation
- Resolution: 16 bits

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<td>Form Factor</td>
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<td># of XMCs</td>
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<td>Crossbar Switch</td>
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<td>Option -104 path</td>
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<td>Lowest Power</td>
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General Information

Model 53651 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53651 includes two A/Ds, two D/A and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
A/D Acquisition IP Modules

The 53651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

Beamformer IP Core

In addition to the DDCs, the 53651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53651’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage
The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53651’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 53651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the boards’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 53651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch
The 53651 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>53651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX</td>
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</tbody>
</table>

Options:
- **-002** -2 FPGA speed grade
- **-014** 400 MHz, 14-bit A/Ds
- **-062** XC6VLX240 FPGA
- **-064** XC6VSX315 FPGA
- **-104** LVDS FPGA I/O through the VPX P2 connector
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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<tr>
<th>Model</th>
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<tr>
<td>8267</td>
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A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or imaginary with DDC, DUC with 2x to 65,536x in 16-bit resolution
- **Output Sampling Rate:** 800 MHz max.
- **Gain Coefficients:** 16-bit resolution
- **Phase Coefficients:** 32 bits, 0 to 360 degrees
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Beamformer
- **Summation:** Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One channel in and one channel out link over the VPX P1 connector using Aurora protocol

Clock Synthesizer
- **Clock Source:** Transformer-coupled, front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Clock Dividers:** Externally or independently for the A/D clock and D/A clock

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Option:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- **Option -150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option -155 or -165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 2: x4 or x8

Environmental
- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 53660 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules

The 53660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description

53660 4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Ordering Information

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTT
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Option -105 path</td>
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<td>Lowest Price</td>
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</tr>
</tbody>
</table>

Model Description

Model 827

VPX Development System. See 8267 Datasheet for Options

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 53661

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

**General Information**

Model 53661 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53661 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**Virtex-6 FPGA**

- LX240T or SX315T
- DDR3 or QDRII+ memories
- DDR3 option 155
- SDRAM 512 MB
- FLASH 64 MB
- UART 40
- Gigabit Serial I/O

**VPX-P2 Connector**

- 4X Gbit Serial
- 4X Ext Serial
- 4X Ext Serial
- 4X Ext Serial

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**Model 53661 COTS (left) and rugged version**

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Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
**FPGA DATAFLOW**

known prior to data acquisition; by a link definition need not be capable of a unique Acquisition linked-list DMA engines are PCIe interface. These powerful moving A/D data through the data in transient capture mode. All memory banks are supported data in FIFO mode or for storing associated memory bank for buffering. Each IP module can receive data easily capturing and moving data. Acquisition IP Modules for easy-likely capturing and moving data.

**Beamformer IP Core**

In addition to the DDCs, the 53661 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

**A/D Converter Stage**

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

**Model 53661**

4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX
PCI Express Interface

The Model 53661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building system and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model Description
53661 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VXSX315T FPGA
-104 LVDS FPGA I/O to VPX P2
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Memory Resources

The 53661 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. DDR3 SDRAM banks can each be up to 512 MB deep.

Fabric-Transparent Crossbar Switch

The 53661 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer

Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit Multiboard Summation Expansion: 32-bit
Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, Functions: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCIe Bus: Gen. 1: x4 or x8; Gen. 2: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3,937 in. x 6,717 in. (100 mm x 170.6 mm)

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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General Information

Model 53662 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

The 53662 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 53662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules

The 53662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.
Model 53662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

PCI Express Interface

The Model 53662 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building system integration. Designed to save engineers and system integrators the time and expense associated with building an integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards.

Ordering Information

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<td>4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX</td>
</tr>
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Options:

- 062   | XC6VLX240T FPGA                                                             |
- 064   | XC6VSX315T FPGA                                                             |
- 104   | LVDS FPGA I/O through VPX P 2                                               |
- 105   | Gigabit serial FPGA I/O through VPX P 1                                     |
- 155   | Two 512 MB DDR3 SDRAM Memory Banks                                         |
- 165   | Two 512 MB DDR3 SDRAM Memory Banks                                         |

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T

Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

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New! New! New! New! New!

3U VPX form factor provides
- PCI Express Gen. 2 x8
- LVPECL clock/sync bus for sample clock synchronization to
- Two banks of 175 DDCs for
- Four 180 MHz 16-bit A/Ds
- Complete GSM channelizer

Features
- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8
- 3U VPX form factor provides a compact, rugged platform

General Information
Model 53663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture
The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCI Express interface, gating, and triggering.

The 53663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage
The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores
The 53663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Model 53663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture
The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCI Express interface, gating, and triggering.

The 53663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage
The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores
The 53663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 53663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 53663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

**Channelizer Output Formatting**

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.
**Model 53663**

1100-Channel GSM Channelizer with Quad A/D - VPX

### Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

**Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**GSM Channel Banks**
- **DDCs per bank:** two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank:** 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

**DDC Channels**
- **Channel Spacing:** 200 kHz, fixed
- **DDC Center Freqs:** IF Freq + k * 200 kHz, where k = 0 to 87, or 0 to 187

**DDC Channel Filter Characteristics:**
- < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
- > 18 dB attenuation at ±100 kHz
- > 78 dB attenuation at ±170 kHz
- > 83 dB attenuation at ±600 kHz
- > 93 dB attenuation at ±800 KHz
- > 96 dB attenuation at ±3 MHz

**DDC Output Rate f_s:** Resampled to 180 MHz/13/2160 = 1.0833333 MS/sec

**DDC Data Output Format:**
- 24 bits I + 24 bits Q

**Superchannels**
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: -f_s/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +f_s/4 (+270.8333 kHz)
  - Fourth: +f_s/2 (+541.666 kHz)
- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q

**Number of Superchannels per Bank:**
- 175-Channel banks: 44; 375-Channel banks: 94

**Field Programmable Gate Array:**
- Xilinx Virtex-6 XC6VSX315T

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td><strong>Option -104 path</strong></td>
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**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

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<td>53663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - VPX</td>
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**Contact Pentek for availability of rugged and conduction-cooled versions**

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<th>Model</th>
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General Information

Model 53664 is a member of the Cobalt® family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 53664 PCIe output supports fully the VITA-49.0 Radio Transport (VRT) Standard.

The 53664 includes four A/Ds and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
A/D Acquisition IP Modules

The 53664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8/f_s$, where $N$ is the decimation setting. The rejection of adjacent-band components within the $80\%$ output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Core

In addition to the DDCs, the 53664 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53663’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

➤ VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA-49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 53664 supports fully the VITA 49.0 specification. ➤
A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53664’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53664 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f_s
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Functions:** trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -106:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCIe Bus:** Gen. 1: x4 or x8; Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

### VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<th>VPX Family Comparison</th>
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<th>53xxx</th>
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<tr>
<td><strong># of XMCs</strong></td>
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<td><strong>Crossbar Switch</strong></td>
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<td>Yes</td>
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<tr>
<td><strong>PCIe path</strong></td>
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<td><strong>Option -105 path</strong></td>
<td>20 pairs on VPX P2</td>
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<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
<td><strong>Lowest Price</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

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**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Model 53664**

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

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**Ordering Information**

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<td>53664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - 3U VPX</td>
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</table>

**Options:**
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS FPGA I/O to VPX P2
- -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- -160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 8267 Development Systems**

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**Model Description**

Model 8267 VPX Development System. See 8267 Datasheet for Options

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**Contact Pentek for availability of rugged and conduction-cooled versions**
**General Information**

Model 53670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53670 includes general purpose and gigabit serial connectors for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53670 family of high performance 3U VPX boards includes general purpose and gigabit links between the FPGA and the VPX backplane, the Model 53670 is a member of the Cobalt® line to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

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### Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- User-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**Model 53670 COTS (left) and rugged version**

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**Virtex-6 FPGA**

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<td>VPX-P1</td>
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<tr>
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**4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX**

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**Pentek, Inc.**

One Park Way ● Upper Saddle River ● New Jersey 07458

Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

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**www.pentek.com**
Video Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5392 or 9192 Cobalt Synchronizers can drive multiple 53670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 53670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

D/A Waveform Playback IP Module

The Model 53670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/A channels from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
Model 53670
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

➤ Fabric-Transparent Crossbar Switch
The 53670 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications
D/A Converters
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs
Quantity: Four D/A outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS
Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -04: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -05: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen 2: x4 or x8;

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model Description
53670 4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U VPX

Options:
-002* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model Description
8267 VPX Development System.
See 8267 Datasheet for Options

Model Family Comparison

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
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<tbody>
<tr>
<td><strong>Form Factor</strong></td>
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<td><strong># of XMCs</strong></td>
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<tr>
<td><strong>Crossbar Switch</strong></td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
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<tr>
<td><strong>PCIe width</strong></td>
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<tr>
<td><strong>Option -04 path</strong></td>
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<tr>
<td><strong>Option -05 path</strong></td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
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<tr>
<td><strong>Lowest Price</strong></td>
</tr>
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</table>

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

Model 53671 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all of the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all

General Information

Model 53671 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all of the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all
**Digital Upconverter and D/A Stage**

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 53671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

**Clocking and Synchronization**

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5392 or 9192 Cobalt Synchronizers can drive multiple 53671 µSync connectors enabling large, multi-channel synchronous configurations.

**Memory Resources**

The 53671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

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**D/A Waveform Playback IP Module**

The Model 53671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model Description**

- Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- Gigabit serial FPGA I/O to VPX P2
- LVDS FPGA I/O to VPX P2
- 1.0x-G(x+1)/16 Vp-p, where 4-bit integer G = 0 to 15
- Transformer-coupled, 50 ohms, accepts 10 to 500 MHz sine wave, 0 to +10 dBm, AC-coupled
- Programmable functions: trigger, gate, sync and PPS

**Ordering Information**

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>8267</td>
<td>VPX Development System. See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>

**Options:**

- -104: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
- -105: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- -106: Xilinx Virtex-6 XC6VLX240T-2
- -107: Xilinx Virtex-6 XC6VSX315T-2
- -108: TI DAC3484
- -109: Front panel female SSMC connector

**Specifications**

- **PCI Express Interface**
  - The Model 53671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

- **Fabric-Transparent Crossbar Switch**
  - The 53671 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

- **D/A Converters**
  - Type: TI DAC3484
  - Input Data Rate: 312.5 MHz max.
  - Output Bandwidth: 250 MHz max.
  - Output Sampling Rate: 1.25 GHz max. with interpolation
  - Interpolation: 2x, 4x, 8x or 16x
  - Resolution: 16 bits

- **Digital Interpolator**
  - Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

- **Front Panel Analog Signal Outputs**
  - Quantity: Four D/A outputs
  - Output Type: Transformer-coupled, 50 ohms, accepts 10 to 500 MHz sine wave, 0 to +10 dBm, AC-coupled

- **Clock Synthesizer**
  - Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  - VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
  - Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

- **External Clock**
  - Type: Front panel female SSMC connector
  - Signal: sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

- **Synchronization**
  - VCXO Frequency: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
  - VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

- **External Trigger Input**
  - Type: Front panel female SSMC connector
  - Function: Programmable functions include: trigger, gate, sync and PPS

- **Timing Bus**
  - 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

- **Field Programmable Gate Array**
  - Standard: Xilinx Virtex-6 XC6VLX240T-2
  - Optional: Xilinx Virtex-6 XC6VSX315T-2

- **Custom I/O**
  - Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
  - Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

- **Memory**
  - Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

- **PCI-Express Interface**
  - PCI Express Bus: Gen. 1 or Gen 2: x4 or x8

- **Environmental**
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.

- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 53690 COTS (left) and rugged version

**General Information**

Model 53690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 53690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep.
PCI Express Interface

The Model 53690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

- 062   | XC6VLX240T FPGA                  |
- 064   | XC6VSX315T FPGA                  |
- 104   | LVDS FPGA I/O to VPX P1          |
- 105   | Gigabit serial FPGA I/O to VPX P1|
- 150   | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2) |
- 160   | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4) |
- 155   | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2) |
- 165   | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |

Specifications

Front Panel Analog Signal Input

- Connector: Front panel female SSMC
- Impedance: 50 ohms

L-Band Tuner

- Type: Maxim MAX2112
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- PLL Reference (freqREF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz

LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter

Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps

*Usable Full-Scale Input Range: −50 dBm to +10 dBm

Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL

Field Programmable Gate Array

- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VX315T

Custom I/O

- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector for serial protocols

Memory

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: −20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Family Comparison

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<thead>
<tr>
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<tr>
<td>Form Factor</td>
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<td>Option -105 path</td>
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<tr>
<td>Lowest Power</td>
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<td>Lowest Price</td>
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Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
General Information

Model 53720 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53720 includes three A/Ds, one upconverter, two D/A and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules

The 53720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53720 factory-installed functions include a sophisticated D/A Waveform Playback IP Module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either onboard memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-P PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of SSMC connectors.
Memory Resources
The 53720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 53720 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>53720</td>
<td>3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
<td>-073 XC7VX330T-2 FPGA, -076 XC7VX690T-2 FPGA, -104 LVDS FPGA I/O to VPX P2, -105 Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

Environmental
- **Operating Temp.**: 0° to 50° C
- **Storage Temp.**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<td>Lowest Power</td>
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General Information

Model 53721 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDR3 IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
A/D Acquisition IP Modules

The 53721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Core

In addition to the DDCs, the 53721 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8k samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53721’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 53721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
Memory Resources

The 53721 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53721 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs. The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will be loaded on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF sampling and sync functions across all connected boards.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolarate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53721’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. 

➤
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Three channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
- Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connections between the FPGA and the VPX P2
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
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<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
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<td>Yes</td>
</tr>
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<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>PCIe switch</td>
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<td>x4 or x8</td>
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<tr>
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<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
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<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
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</tr>
</tbody>
</table>
**Model 53730**

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

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### General Information

Model 53730 is a member of the Onyx family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

### The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Module

The 53730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments AD85400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
Memory Resources
The 53730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 53730 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and testing a development system for Pentek Cobalt, Onyx and integrated development system Flexor 3U VPX boards. It was created to save engineers and

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VXCO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VXCO. Either clock source (front panel or VXCO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

Crossbar Switch
The 53730 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VXCO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VXCO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 to support serial protocols

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8;
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 53741 COTS (left) and rugged version

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

General Information
Model 53741 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**A/D Acquisition IP Module**

The 53741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately pre-selects a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.
VPX P1 or P2 on VPX P1 or P2
x4 or x8

The 53741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Crossbar Switch

The 53741 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a development system. It was created to save engineers and system integrators the time and expense associated with building a development system.

8267 VPX Development System

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a development system.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a development system.

Specifications

Front Panel Analog Signal Inputs

<table>
<thead>
<tr>
<th>Input Type</th>
<th>Transformer-coupled, front panel SSMC connectors</th>
</tr>
</thead>
</table>

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

Clocking and Synchronization

The 53741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 53741’s can be synchronized with a simple cable. For larger systems, multiple 53741’s can be synchronized using the Model 5392 high-speed sync board to drive the sync bus.

PCI Express Interface

The Model 53741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>53741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
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<table>
<thead>
<tr>
<th>Options</th>
<th>Description</th>
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<tr>
<td>-073</td>
<td>XC7VX330T-2 FPGA</td>
</tr>
<tr>
<td>-076</td>
<td>XC7VX690T-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
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<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
</tr>
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</table>

Pentek, Inc.  One Park Way  •  Upper Saddle River  •  New Jersey 07458  
Tel: 201-818-5900  •  Fax: 201-818-5904  •  Email: info@pentek.com  
www.pentek.com
Model 53751

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

**General Information**

Model 53751 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 53751 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53751 factory installed functions include two A/D conversion and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
### A/D Acquisition IP Modules

The 53751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### D/A Waveform Playback IP Module

The Model 53751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

### DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \cdot f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

#### GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx IMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course...
of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53751’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 53751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**Fabric-Transparent Crossbar Switch**

The 53751 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

**PCI Express Interface**

The Model 53751 includes an industry-standard interface fully compliant with PCIe Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53751</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

-014 400 MHz, 14-bit A/Ds
-073 XC7VX330T-2 FPGA
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>
General Information

Model 53760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53760 includes four A/Ds and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules

The 53760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user and programmed into the FLASH through Xilinx iMPACT or through the board’s PCIe interface. At power up, the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel.
PCI Express Interface

The Model 53760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53760 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building system integrators the time and testing a development system. It was designed to provide a complete integrated development system for prototyping PCIe links up to x8, the transparencies enable optimization.

The Model 8267 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Bandpass: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Environmental

- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>VPX P1 or P2</td>
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<td>PCIe width</td>
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<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
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<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
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<td>No</td>
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<tr>
<td>Lowest Price</td>
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<td>No</td>
</tr>
</tbody>
</table>
Model 53761 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53761 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 53761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
A/D Acquisition IP Modules

The 53761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

Beamformer IP Core

In addition to the DDCs, the 53761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 53761’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from.
Model 53761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53761 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53761 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.
Model 53761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Resolutions: 32 bits, 0 to ƒs
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to ±10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
--- | ---
53761 | 4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:
- 076 | XC7VX690T-2 FPGA
- 104 | LVDS FPGA I/O to VPX P2

Contact Pentek for availability of rugged and conduction-cooled versions.

Model | Description
--- | ---
8267 | VPX Development System

See 8267 Datasheet for Options

Contact Pentek for availability of rugged and conduction-cooled versions
Model 53791 COTS (left) and rugged version

General Information

Model 53791 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 53791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 53791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 2 PCIe interface.

Thus, the 53791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Accepts RF signals from 925 MHz to 2175 MHz

Programmable LNA handles L-Band input signal levels from –50 dBm to +10 dBm

Programmable analog downconverter provides IF or I/Q baseband signals at frequencies up to 123 MHz

Two 500 MHz 12-bit A/Ds digitize IF or I/Q signals synchronously; optional: 400 MHz 14-bit A/Ds

Two FPGA-based multiband digital downconverters

Xilinx Virtex-7 VX330T or VX690T FPGAs

4 GB of DDR3 SDRAM

Sample clock synchronization to an external system reference

PCI Express (Gen. 1, & 2) interface, up to x8

Clock/sync bus for multiboard synchronization

Optional user-configurable gigabit serial interface

Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Modules

The 53791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converters and DDCs**

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

**A/D Clocking & Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 53791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe. The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

**Fabric-Transparent Crossbar Switch**

The 53791 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Model 53791

➤ PCI Express Interface
The Model 53791 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuner
Type: Maxim MAX2121
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer: \( f_{VCO} = (N.F.) \times f_{REF} \)
where integer \( N \) = 19 to 251 and fractional \( F \) is a 20-bit binary value
PLL Reference (freqREF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
Usable Full-Scale Input Range: -50 dBm to +10 dBm
Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz
A/D Converters
Type: Texas Instruments ADS5463
Sampling Rate: 10 MHz to 500 MHz
Resolution: 12 bits
Option -014: 400 MHz, 14-bit A/Ds
Sample Clock Sources: On-board timing generator/synthesizer
A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs;
TTL signal for gate/trigger and sync/PPS inputs
External Trigger Input
Quantity: 2
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols.
Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<th>Description</th>
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<td>L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX</td>
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<td>LVDS FPGA I/O to VPX P2</td>
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<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P1</td>
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</tbody>
</table>

Options:
-014 400 MHz, 14-bit A/Ds
-076 XC7VX690T-2 FPGA
-100 27 MHz crystal for MAX2121
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8267 VPX Development System
See 8267 Datasheet for Options
8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

General Information

Model 53131 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through

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Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 53131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42L69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 53131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

**Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

**Crossbar Switch**

The 53131 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- 084  XCKU060-2 FPGA
- 087  XCKU115-2 FPGA
- 014  LVDS FPGA I/O
- 015  Gigabit serial FPGA I/O
- 702  Air cooled, Level L2
- 713  Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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**PCI Express Interface**

The Model 53131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

**Digital Downconverters**

- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_c \)
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**

- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus:** 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**

- **Type:** Front panel female MMCX connector, LVTTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Kintex UltraScale XCKU105-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**

- **Option -104:** Connects 20 LVDS pairs between the FPGA and VPX P2
- **Option -105:** Connects eight gigabit serial lanes between the FPGA and VPX P1

**Memory**

- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

**Environmental**

- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -702:** L2 (air cooled)
- **Operating Temp:** -20° to 65°C
- **Storage Temp:** -40° to 100°C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -713:** L3 (conduction cooled)
- **Operating Temp:** -40° to 70°C
- **Storage Temp:** -50° to 100°C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Size:** 3.937 in. x 6.717 in. (100.00 mm x 170.60 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
</tr>
<tr>
<td>52xxx: 3U VPX</td>
</tr>
<tr>
<td>53xxx: 3U VPX</td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
</tr>
<tr>
<td>52xxx: One XMC</td>
</tr>
<tr>
<td>53xxx: Yes</td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
</tr>
<tr>
<td>52xxx: No</td>
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<tr>
<td>53xxx: Yes</td>
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<tr>
<td><strong>PCIe Path</strong></td>
</tr>
<tr>
<td>52xxx: VPX P1</td>
</tr>
<tr>
<td>52xxx: VPX P1 or P2</td>
</tr>
<tr>
<td>53xxx: x4</td>
</tr>
<tr>
<td>53xxx: x4 or x8</td>
</tr>
<tr>
<td><strong>PCIe Width</strong></td>
</tr>
<tr>
<td>52xxx: 24 pairs on VPX P2</td>
</tr>
<tr>
<td>52xxx: 20 pairs on VPX P2</td>
</tr>
<tr>
<td>53xxx: Two x4 or one x8 on VPX P1</td>
</tr>
<tr>
<td>53xxx: Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
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<tr>
<td>52xxx: Yes</td>
</tr>
<tr>
<td>52xxx: No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
</tr>
<tr>
<td>52xxx: Yes</td>
</tr>
<tr>
<td>52xxx: No</td>
</tr>
</tbody>
</table>

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  www.pentek.com
Model 53132 is a member of the Jade family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

**Features**

- **Complete radar and software radio interface solution**
- **Supports Xilinx Kintex UltraScale FPGAs**
- **Eight 250 MHz 16-bit A/Ds**
- **Eight wideband DDCs (digital downconverters)**
- **64 multiband DDCs**
- **5 GB of DDR4 SDRAM**
- **Sample clock synchronization to an external system reference**
- **LVPECL clock/sync bus for multiboard synchronization**
- **PCI Express (Gen. 1, 2 & 3) interface up to x8**
- **Optional LVDS and gigabit serial connections to the FPGA for custom I/O**
- **Ruggedized and conduction-cooled versions available**

**General Information**

Model 53132 for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.
A/D Acquisition IP Modules

The Pentek Model 52862 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \(f_s\), where \(f_s\) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \(f_s\), where \(f_s\) is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 5293 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications.
Model 53132

8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

PCI Express Interface

The Model 53132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Crossbar Switch

The 53132 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model Description
53132 8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

Options:
-084 XCKU060-2 FPGA
-087 XCKU115-2 FPGA
-104 LVDS FPGA I/O through VPX P2
-105 Gigabit serial FPGA I/O through VPX P1 connector
-702 Air cooled, Level L2
-713 Conduction cooled, Level L3

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female MMCX connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Eight paths
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Eight paths, 8 channels per bank
Decimation Range: 16x to 1024x in steps of 8
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female MMCX connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Option -104: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105: Provides one 8x gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>3U VPX Family Comparison</th>
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<td>52xxx</td>
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</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

General Information
Model 53141 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features
- Ideal radar and software radio interface solution
- Supports XilinX Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- μSync clock/sync bus for multinode synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

The Model 53141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 53141 factory installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/A waveforms stored in either on-board memory or offboard host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections between the FPGA and the VPX P2 connector the for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz, or in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 53141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 53141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 53141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201 818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Fabric-Transparent Crossbar Switch
The 53161 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 4X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
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<tbody>
<tr>
<td><strong>52xxx</strong></td>
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<tr>
<td><strong>53xxx</strong></td>
</tr>
<tr>
<td>Form Factor</td>
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<tr>
<td># of XMCs</td>
</tr>
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<td>Crossbar Switch</td>
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<td>PCIe path</td>
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<td>PCIe width</td>
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<tr>
<td>Option -104 path</td>
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<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Ordering Information
Model Description
53141 1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

De
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elopment Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
General Information

Model 53821 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 53821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.
A/D Acquisition IP Modules

The 53821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

D/A Waveform Playback IP Module

The Model 53821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and dual D/A stages.

KINTEX ULTRASCALE FPGA DATAFLOW DETAIL

- The Model 53821 is designed for high-performance data acquisition and processing applications with three A/D and two DUC channels.
- It integrates Kintex UltraScale FPGA technology for powerful signal processing.
- The schematic diagram shows the dataflow details for A/D and D/A acquisition and upconversion.
- Key features include:
  - Three A/D channels at 200 MHz.
  - Two DUC channels at 800 MHz.
  - DMA engines for efficient data movement.
  - Linked-list DMA cores for flexible data handling.
  - METADATA packets for data integrity.
  - Throttle, Meter, and Detect features for monitoring.
  - Waveform Playback and D/A engine for generating waveforms.
  - PCIe Interface for communication.

Pentek, Inc.
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
Model 53821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

- When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

  If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

  Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

  Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

  A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

  Multiple 53821’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

  The 53821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

  The Model 53821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +5 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

A/D Converters

  Type: Texas Instruments ADS5485
  Sampling Rate: 10 MHz to 200 MHz
  Resolution: 16 bits

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**SPARK Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

### Ordering Information

**Model** | **Description**
---|---
53821 | 3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

**Options:**
- **-084** XCKU060-2 FPGA
- **-087** XCKU115-2 FPGA
- **-104** LVDS FPGA I/O through VPX P1
- **-105** Gigabit serial FPGA I/O through VPX P1
- **-702** Air cooled, Level L2
- **-713** Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

**VPX Family Comparison**

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<tr>
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<th>53xxx</th>
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<tbody>
<tr>
<td>Form Factor</td>
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<td>3U VPX</td>
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<td># of XMCs</td>
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<td>Yes</td>
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<td>PCIe Switch</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<td>PCIe width</td>
<td>x4</td>
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<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

**Model 53821**

**3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX**

- **Digital Downconverters**
  - **Quantity:** Two channels
  - **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
  - **LO Tuning Freq. Resolution:** 32 bits, 0 to f<sub>L</sub>
  - **LO SFDR:** >120 dB
  - **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
  - **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
  - **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- **D/A Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Signal:** 2-channel real or 1-channel with frequency translation
  - **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
  - **Resolution:** 16 bits

- **Digital Interpolator Core**
  - **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x
  - **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

- **Front Panel Analog Signal Outputs**
  - **Output:** Transformer-coupled, front panel female SSMC connectors
  - **Transformer:** Coil Craft WBC4-6TLB
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

- **Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

- **External Clock**
  - **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

- **Field Programmable Gate Array**
  - **Standard:** Xilinx Kintex UltraScale XCKU035-2

- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

- **Custom I/O**
  - **Option -104** provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
  - **Option -105** provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

- **Memory**
  - **Type:** DDR4 SDRAM
  - **Size:** 5 GB
  - **Speed:** 1200 MHz (2400 MHz DDR)

- **PCI-Express Interface**
  - **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

- **Environmental**
  - **Standard:** L0 (air cooled)
    - **Operating Temp:** 0° to 50° C
    - **Storage Temp:** -20° to 90° C
    - **Relative Humidity:** 0 to 95%, non-condensing
  - **Option -702:** L2 (air cooled)
    - **Operating Temp:** -20° to 65° C
    - **Storage Temp:** -40° to 100° C
    - **Relative Humidity:** 0 to 95%, non-condensing
  - **Option -713:** L3 (conduction cooled)
    - **Operating Temp:** -40° to 70° C
    - **Storage Temp:** -50° to 100° C
    - **Relative Humidity:** 0 to 95%, non-condensing
  - **Size:** 3U VPX board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)
General Information

Model 53841 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCIe Express Gen. 3 as a native interface, Model 53841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.
A/D Acquisition IP Module

The 53841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has an associated 5 GB memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8×f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

PCI Express Interface

The Model 53841 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Option -104 connects 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

Pentek, Inc.◆ One Park Way◆ Upper Saddle River◆ New Jersey 07458◆ Tel: 201.818.5900◆ Fax: 201.818.5904◆ Email: info@pentek.com◆ www.pentek.com
Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Memory Resources
The 53841 architecture supports an optional 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Crossbar Switch
The 53841 architecture supports a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to fs
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL

Clocking and Synchronization
The 53841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.
A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 53841’s can be synchronized with a simple cable. For larger systems, multiple 53841’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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Model 53851

General Information

Model 53851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/A. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 53851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 53851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own. ➤

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/A
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multinode synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

New! New! New! New! New!

Model 53851 COTS (left) and rugged version

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Pentek Inc. One Park Way, Upper Saddle River, New Jersey 07458
www.pentek.com
Tel: 201 818 5900 Fax: 201 818 5904 Email: info@pentek.com
A/D Acquisition IP Modules

The 53851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output band-widths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

D/A Waveform Playback IP Module

The Model 53851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.
Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 53851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53851 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

| Input Type: | Transformer-coupled, front panel female SSMC connectors |
| Transformer Type: | Coil Craft WBC4-6TLB |
| Full Scale Input: | +5 dBm into 50 ohms |
| 3 dB Passband: | 300 kHz to 700 MHz |


A/D Converters (standard)

| Type: | Texas Instruments ADS5463 |
| Sampling Rate: | 20 MHz to 500 MHz |
| Resolution: | 12 bits |

A/D Converters (option -014)

| Type: | Texas Instruments ADS5474 |
| Sampling Rate: | 20 MHz to 400 MHz |
| Resolution: | 14 bits |
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 65,536 in three stages of 2x to 32x and one fixed stage of 2x
- LO Tuning Freq. Resolution: 32 bits, 0 to f<sub>s</sub>
- LO SFD: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Digital Interpolator Core
- Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
- Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale
- Option -084: Xilinx Kintex UltraScale
- Option -087: Xilinx Kintex UltraScale

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8x gigabit link between the FPGA and the VPX P1 connector to support serial protocols

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-condensing

Ordering Information

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Options:
- 014: 400 MHz, 14-bit A/Ds
- 084: XCKU060-2 FPGA
- 087: XCKU115-2 FPGA
- 087: XCKU115-2 FPGA
- 084: XCKU060-2 FPGA
- 104: LVDS FPGA I/O through VPX P2 connector
- 105: Gigabit serial FPGA I/O through VPX P1 connector
- 702: Air cooled, Level L2
- 713: Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

General Information

Model 53861 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules
The 53861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores
Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage
The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 53861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 53861

4-Channel 200 MHz A/D with DDCs and Xilinx Kintex UltraScale FPGA - 3U VPX

Fabric-Transparent Crossbar Switch

The 53861 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1x) lanes, or groups of four lanes (4x).

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered and tested a development system.

Ordering Information

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<td>- 087</td>
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<td>LVDS FPGA I/O to VPX P2</td>
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<td>Air cooled, Level L2</td>
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<tr>
<td>- 713</td>
<td>Conduction cooled, Level L3</td>
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</table>

Contact Pentek for complete specifications of rugged and conduction-cooled versions

PCI Express Interface

The Model 53861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6T9L8
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters

- Quantity: Four channels
- Decimation Range: 10 x 32,768 x in three stages of 2 x 32
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, 0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
- External Trigger Input Type: Front panel female SSMC connector, LVTL3
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory

- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -104: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -105: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

- Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

3U VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

General Information

Model 53862 is a member of the Jade family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 53862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included.) Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com www.pentek.com
The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8x gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI AD55485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 53862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 53862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

➤ Fabric-Transparent Crossbar Switch
The 53862 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

PCI Express Interface
The Model 53862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

SPARK Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Oxyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53862</td>
<td>4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
- 084: XCKU060-2 FPGA
- 087: XCKU115-2 FPGA
- 104: LVDS FPGA I/O to VPX P1
- 105: Gigabit serial FPGA I/O to VPX P1
- 702: Air cooled, Level L2
- 713: Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: CoilCraft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 5 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments AD55485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Wideband Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to f₀
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- Quantity: Four banks, 8 channels per bank
- Decimation Range: 2x to 1024x
- LO Tuning Freq. Resolution: 32 bits, 0 to f₀ independent tuning for each channel
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50°C
- Storage Temp: −20° to 90°C
- Option -702: L2 (air cooled)
- Operating Temp: −20° to 65°C
- Storage Temp: −40° to 100°C
- Option -713: L3 (conduction cooled)
- Operating Temp: −40° to 70°C
- Storage Temp: −50° to 100°C
- In all Cases Relative Humidity: 0 to 95%, non-condensing
- Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

3U VPX Family Comparison

<table>
<thead>
<tr>
<th></th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td></td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x4 or x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>One x8 on VPX P1 or P2</td>
<td>One x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
General Information

Model 53800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 53800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The 53800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Front Panel Digital I/O Interface

The 53800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
**Model 53800**

► Interfaces and Memory

The Model 53800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The 53800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Crossbar Switch

The 53800 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable input equalization and output pre-emphasis settings enable optimization.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options:</th>
</tr>
</thead>
</table>
| 53800 | Kintex UltraScale FPGA Coprocessor - 3U VPX | -084 XCKU060-2 FPGA  
-087 XCKU115-2 FPGA  
-104 LVDS FPGA I/O  
-105 Gigabit serial FPGA I/O  
-702 Air cooled, Level L2  
-713 Conduction cooled, Level L3 |

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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**Specifications**

Front Panel Digital I/O
- Connector Type: 80-pin connector, mates to a ribbon cable connector
- Signal Quantity: 38 pairs
- Signal Type: LVDS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 100° C
- Option -702: L2 (air cooled)
- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Option -713: L3 (conduction cooled)
- Operating Temp: -40° to 70° C
- Storage Temp: -50° to 100° C

Relative Humidity in all options: 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

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**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
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<tbody>
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<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
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</tbody>
</table>

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**Kintex UltraScale FPGA Resources**

![Kintex UltraScale FPGA Resources Diagram](image-url)

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**Contact Pentek for complete specifications of rugged and conduction-cooled versions**
3U VPX Development System for Cobalt, Onyx and Flexor Boards

General Information
The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19” 4U rackmount chassis that is 12” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options
Available options include high-end multi-core CPUs and extended memory support.

Specifications
Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19” W x 12” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information
Model Description
8267 3U VPX Development System for Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS
-101 Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
### RADAR & SDR I/O - AMC

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<th>DESCRIPTION</th>
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<tr>
<td>Cobalt 56621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 56624</td>
<td>Dual-Channel, 34-Signal Adaptive IF Relay - AMC</td>
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<tr>
<td>Cobalt 56630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - AMC</td>
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<tr>
<td>Cobalt 56640</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 56641</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Wideband DDC, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 56650</td>
<td>Two 500 MHz A/Ds, DUC, 800 MHz D/A, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 56651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, Virtex-6 FPGA - AMC</td>
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<tr>
<td>Cobalt 56661</td>
<td>4-Channel 200 MHz A/D, DUC, Virtex-6 FPGA - AMC</td>
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<td>Cobalt 56662</td>
<td>4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC</td>
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<tr>
<td>Cobalt 56663</td>
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<td>Cobalt 56664</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 56667</td>
<td>4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC</td>
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<tr>
<td>Cobalt 56690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Onyx 56720</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56721</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56751</td>
<td>2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56760</td>
<td>4-Channel 200 MHz A/D, 16-bit A/D, Virtex-7 FPGA - AMC</td>
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<tr>
<td>Onyx 56761</td>
<td>4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - AMC</td>
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<td>Onyx 56791</td>
<td>L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - AMC</td>
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<td>Jade 51131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC</td>
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<tr>
<td>Jade 51132</td>
<td>8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC</td>
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<tr>
<td>Jade 51141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - AMC</td>
</tr>
<tr>
<td>Jade 51821</td>
<td>3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Kintex UltraScale FPGA - AMC</td>
</tr>
<tr>
<td>Jade 51841</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - AMC</td>
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<td>Jade 51851</td>
<td>2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex UltraScale FPGA - AMC</td>
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<tr>
<td>Jade 51861</td>
<td>4-Channel 200 MHz A/D with DDc and Kintex UltraScale FPGA - AMC</td>
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<tr>
<td>Jade 51862</td>
<td>4-Channel 200 MHz A/D with Multiband DDCs, Kintex UltraScale FPGA - AMC</td>
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<td>Jade 56800</td>
<td>Kintex UltraScale FPGA Coprocessor - AMC</td>
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<tr>
<td>Bandit 5620</td>
<td>Two-Channel Analog RF Wideband Downconverter - AMC</td>
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### Customer Information

- [Click for Product Selector](http://www.pentek.com)
The Model 56132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The Model 56132 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female MMCX connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Wideband Digital Downconverters
- Quantity: Eight channels
- Decimation Range: 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- Quantity: Eight banks, 8 channels per bank
- Decimation Range: 16x to 1024x in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \), independent tuning for each channel
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female MMCX connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50° C
- Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
- Operating Temp: -20° to 65° C
- Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
- Operating Temp: -40° to 70° C
- Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

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module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56620 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56620 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

D/A Converters

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference
- **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 x4 or x8; Gen. 2: x4

AMC Interface

- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental

- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

General Information
Model 56621 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56621 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed functions ideally matched to the board’s analog interfaces. The 56621 factory installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules

The 56621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_\omega$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Core

In addition to the DDCs, the 56621 features a complete beamforming subsystem. Each DDC core contains programmable I & Q parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module FIFO for reading over the PCIe. For larger systems, multiple 56621’s can be chained together via a built-in Xilinx Aurora gigabit serial interface which allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 56621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
**A/D Converter Stage**

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56621’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 56621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**AMC Interface**

The Model 56621 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56621 includes an industry-standard interface fully compliant with PCIe Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤
3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Three channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer
- **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Summation Expansion:** 32-bit

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC</td>
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Options:
- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS FPGA I/O through front panel connector
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- **-160** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 56624 is a member of the Cobalt® family of high-performance AMC boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 56624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

Adaptive Relay Input Overview

The Model 56624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) and two DUCs (digital upconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

Adaptive Relay Output Overview

The Model 56624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation). The translated DUC outputs are directed to either of two summation blocks, each

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**Features**
- Modifies 34 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two 200 MHz 16-bit A/Ds
- Two 800 MHz 16-bit D/A
- 34 DDCs and 34 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCIe Express Gen. 1: x4 or x8

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**Diagram**

[Diagram of the Model 56624 board showing input and output channels, DDCs, DUCs, and summation blocks.]

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associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

Xilinx Virtex-6 FPGA

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 56624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

A/D Converters

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

Digital Downconverters

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8f_s/N$, where $N$ is the decimation setting and $f_s$ is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Input Gain Blocks

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Receive DMA Controller

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 56624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

Transmit DMA Controller

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 56624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

Output Gain Blocks

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

Digital Upconverters

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.
Model 56624

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to $f_s$ where $f_s$ is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

**Summation Blocks**

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

**D/A Converters**

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56624’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**AMC Interface**

The Model 56624 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56624 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

**Form Factor Adaptors**

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.
Dual-Channel, 34-Signal Adaptive IF Relay - AMC

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Quantity: 2
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: 34
- Decimation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >100 dB
- Phase Offset: 1 bit, 0 or 180 degrees
- FIR Filter: 18-bit coefficients
- Output: Complex, 16-bit I + 16-bit Q
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Output Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/- 48 dB

Digital Upconverters
- Quantity: 34
- Interpolation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- FIR Filter: 18-bit coefficients, 16-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Required: Xilinx Virtex-6 XC6VSX315T

AMC Interface
- Type: AMC.1
- Module Management: IPMI Version 2.0

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Standard:
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.

Option 702 L2 Extended Temp (air-cooled):
- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-cond.

Option 712 L2 Extended Temp (conduction-cooled):
- Operating Temp: -20° to 65° C
- Storage Temp: -40° to 100° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions
Model 56630
1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

General Information

Model 56630 is a member of the Cobalt® family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56630 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSnc clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
- Memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Converter Stage
The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage
The 56630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Memory Resources
The 56630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Model 56630
1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

➤ AMC Interface
The Model 56630 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen.1: x4 or x8; Gen 2: x4

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions
Model 56640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

General Information

Model 56640 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56640 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz, or in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 56640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**Clocking and Synchronization**

The 56640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 56640’s can be synchronized using the Cobalt high speed sync module to drive the sync bus.

**Memory Resources**

The 56640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**AMC Interface**

The Model 56640 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

**PCI Express Interface**

The Model 56640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converter**

- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

**Sample Clock Sources:** Front panel SSMC connector

**Sync Bus:** Multi-pin connectors, bus includes gate, reset and in and out ref clock

**External Trigger Input**

- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

**Custom I/O**

- **Option -002:** -2 FPGA speed grade
- **-062:** XC6VLX240T
- **-064:** XC6VSX315T
- **-104:** LVDS FPGA I/O through front panel connector
- **-155:** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165:** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Ordering Information**

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**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS FPGA I/O through front panel connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions.
Model 56641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

General Information

Model 56641 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56641 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Features

- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Acquisition IP Module**

The 56641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**Clocking and Synchronization**

The 56641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The sync bus includes gate, reset, and in and out reference clock signals. Two 56641’s can be synchronized with a simple cable. For larger systems, multiple 56641’s can be synchronized using the Cobalt 7192 high-speed sync module to drive the sync bus.

**Memory Resources**

The 56641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.
**Model 56641**

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - AMC

- **AMC Interface**
  - The Model 56641 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

- **PCI Express Interface**
  - The Model 56641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converter**
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

**Digital Downconverters**
- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x; two-channel mode: 4x, 8x, or 16x

**LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
**LO SFDR:** >120 dB
**Phase Offset Resolution:** 32 bits, 0 to 360 degrees
**FIR Filter:** User-programmable 18-bit coefficients
**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources:** Front panel SSMC connector
**Sync Bus:** Multipin front panel connector, includes gate, reset, and in and out ref clock

**External Trigger Input**
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include trigger and gate

**Field Programmable Gate Array**
- **Type:** Xilinx Virtex-6 XC6VSX315T-2

**Custom I/O**
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**
- **Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR**

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4 or x8

**AMC Interface**
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>56641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

**Options:**

- **-002***: -2 FPGA speed grade
- **-064***: XC6VSX315T
- **-104**: LVDS FPGA I/O through front panel connector
- **-155***: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165***: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

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*Contact Pentek for availability of rugged and conduction-cooled versions*
Model 56650

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - AMC

General Information
Model 56650 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, one DUC (Digital Upconverter), two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56650 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Converter Stage**

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/ Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 56650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the.
Front Panel Analog Signal Outputs
- **Output Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

Sample Clock Sources:
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers:
- External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus:
- 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type**: Front panel female SSMC connector, LVTTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104**: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- **Option 150 or 160**: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165**: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus**: Gen.1 or Gen.2, x4 or x8

AMC Interface
- **Type**: AMC.1
- **Module Management**: IPMI Version 2.0

Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>56650</td>
<td>Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

**Options:**
- -002* -2 FPGA speed grade
- -014 400 MHz, 14-bit A/Ds
- -062 XC6VLX240 FPGA
- -064 XC6VFX315 FPGA
- -104 LVDS FPGA I/O through front panel connector
- -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- -160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

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Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 56651 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnaround solution.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56651 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56651 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules
The 56651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Beamformer IP Core
In addition to the DDCs, the 56651 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56651’s can be chained together via a built-in Xilinx Aurora gigabit serial interface to allow summation across channels on multiple boards.

D/A Waveform Playback IP Module
The Model 56651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56651’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56651 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56651 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option -014)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Beamformer
- Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VXCO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Clock Dividers
- External clock or VXCO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

Ordering Information

Model Description
56651 2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - AMC

Options:
- -002* -2 FPGA speed grade
- -014 400 MHz, 14-bit A/Ds
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS FPGA I/O through front panel connector
- -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 56660 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56660 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed documents as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56660 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

- **PCI Express Interface**
  The Model 56660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

- **Specifications**
  - **Front Panel Analog Signal Inputs**
    - **Input Type:** Transformer-coupled, front panel female SSMC connectors
    - **Transformer Type:** Coil Craft WBC4-6TLB
    - **Full Scale Input:** +8 dBm into 50 ohms
    - **3 dB Passband:** 300 kHz to 700 MHz
  - **A/D Converters**
    - **Type:** Texas Instruments ADS5485
    - **Sampling Rate:** 10 MHz to 200 MHz
    - **Resolution:** 16 bits
  - **Sample Clock Sources:** On-board clock synthesizer
  - **Clock Synthesizer**
    - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
    - **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
    - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
  - **External Clock**
    - **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
  - **Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

- **External Trigger Input**
  - **Type:** Front panel female SSMC connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS

- **Field Programmable Gate Array**
  - **Standard:** Xilinx Virtex-6 XC6VLX130T
  - **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

- **Custom I/O**
  - **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

- **Memory**
  - **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  - **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

- **PCI-Express Interface**
  - **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

- **AMC Interface**
  - **Type:** AMC.1
  - **Module Management:** IPMI Version 2.0

- **Environmental**
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-cond.

- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>56660</td>
<td>4-Channel 200 MHz A/D with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

**Options:**
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through front panel connector
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-160** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*Contact Pentek for availability of rugged and conduction-cooled versions*
4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC

General Information

Model 56661 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multifunction, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56661 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

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Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SX FPGA families
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \(0.8f_s/N\), where \(N\) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

**Beamformer IP Core**

In addition to the DDCs, the 56661 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this case, the clock is distributed to each module via the backplane.

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**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \(f_s\), where \(f_s\) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.
Model 56661
4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - AMC

AMC Interface
The Model 56661 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or μTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Ordering Information

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Options:
- 062  XC6VLX240T
- 064  XC6VSX315T
- 104  LVDS FPGA I/O through front panel connector
- 150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to 32
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: 1 & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/sync and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
- Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
- Type: AMC.1
- Module Management: IPMI Version 2.0

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
General Information

Model 56662 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56662 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 56662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multibank DDCs
- Up to 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Modules

The 56662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation ratio is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s \)/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.00 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of \( f_s \)/N. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interlever that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Virtex-6 FPGA Dataflow Detail

-The 56662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.
Model 56662

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56662 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56662 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four 8-channel banks, one per acquisition module
- Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

Environmental
- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model      Description
56662  4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - AMC

Options:
-062      XC6VLX240T
-064      XC6VSX315T
-104      LVDS FPGA I/O through front panel connector
-155      Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165      Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
## General Information

Model 56663 is a member of the Cobalt family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

### The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 56663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

### A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

### Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

### GSM Channelizer Cores

The 56663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 56663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 56663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

### Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

### Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

### PCI Express Interface

The Model 56663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 56663 and host.

### AMC Interface

The Model 56663 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
1100-Channel GSM Channelizer with Quad A/D - AMC

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
- Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
- IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
- Channel Spacing: 200 kHz, fixed
- DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
- < 0.1 dB pass band flatness across ±80 kHz from center (160 kHz BW)
- > 18 dB attenuation at ±100 kHz
- > 78 dB attenuation at ±170 kHz
- > 83 dB attenuation at ±600 kHz
- > 93 dB attenuation at ±800 kHz
- > 96 dB attenuation at > ±3 MHz

DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.083333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
- Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:
- First: -f_s/4 (-270.8333 kHz)
- Second: 0 Hz
- Third: +f_s/4 (+270.8333 kHz)
- Fourth: +f_s/2 (+541.666 kHz)

Superchannel Sample Rate: f_s

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- PCI Express Bus: Gen. 2 x8

AMC Interface
- Type: AMC.1
- Module Management: IPMI Version 2.0

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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Contact Pentek for availability of rugged and conduction-cooled versions
Model 56664 is a member of the Cobalt family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with programmable DDCs (digital downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 56664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56664 includes a front panel general-purpose connector for application-specific I/O.

### The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (Digital Downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LX7 FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**Beamformer IP Core**

In addition to the DDCs, the 56664 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56664's can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

**VITA 49.0**

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 56664 supports fully the VITA 49.0 specification.
A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments AD5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56664’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56664 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or μTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments AD5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Four channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs, TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model | Description
--- | ---
56664 | 4-Channel 200 MHz A/D with DDCs, VITA 49.0 and Virtex-6 FPGA - AMC

Options:
-062 | XC6VLX240T
-064 | XC6VSX315T
-104 | LVDS FPGA I/O through front panel connector
-150 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions
**General Information**

Model 56670 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5692 or 9192 Cobalt Synchronizers can drive multiple 56670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 56670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56670 complies with the AMC1.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

D/A Waveform Playback IP Module

The Model 56670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
### 4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

#### PCI Express Interface

The Model 56670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

#### Specifications

**D/A Converters**
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Input**
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus**
- **Type:** 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**
- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**
- **Type:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

**AMC Interface**
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Ordering Information**

<table>
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<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>56670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

**Options:**
- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through front panel connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions
Model 56671

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC

General Information

Model 56671 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56671 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX3 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multichannel synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMI 2.0 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital up converter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 56671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5692 or 9192 Cobalt Synchronizers can drive multiple 56671 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 56671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC

**AMC Interface**

The Model 56671 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**D/A Converters**

- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

**Digital Interpolator**

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

**Front Panel Analog Signal Outputs**

- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** \(1.0 \times (G+1)/16\) Vp-p, where 4-bit integer \(G = 0\) to 15

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Input**

- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus**

- **Type:** 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

**Field Programmable Gate Array**

- **Type:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**

- **Type:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8

**AMC Interface**

- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Ordering Information**

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<th>Model</th>
<th>Description</th>
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<tr>
<td>56671</td>
<td>4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through front panel connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**
General Information

Model 56690 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56690 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LX3 FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
**L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - AMC**

**RF Tuner Stage**
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**
The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**A/D Clocking and Synchronization**
An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**
The 56690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

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**A/D Acquisition IP Modules**
The 56690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA.

### AMC Interface

The Model 56690 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or μTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

### PCI Express Interface

The Model 56690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

### Specifications

#### Front Panel Analog Signal Input
- **Connector**: Front panel female SSMC
- **Impedance**: 50 ohms

#### L-Band Tuner
- **Type**: Maxim MAX2112
- **Input Frequency Range**: 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise**: -97 dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer**:
  - \( f_{\text{vco}} = (N.F) \times f_{\text{ref}} \)
  - where integer \( N \) = 19 to 251 and fractional \( F \) is a 20-bit binary value
- **PLL Reference** (\( f_{\text{ref}} \)): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain**: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- **Baseband Amplifier Gain**: 0 to 15 dB, in 1 dB steps*
- **Usable Full-Scale Input Range**: -50 dBm to +10 dBm
- **Baseband Low Pass Filter**: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

#### A/D Converters
- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

#### Sample Clock Sources
- **On-board timing generator/synthesizer

#### A/D Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

#### Timing Generator External Clock Input
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

#### Timing Generator Bus
- **Type**: Front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input
- **Quantity**: 2
- **Type**: Front panel female SSMC connector, LVTTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

#### Field Programmable Gate Array
- **Standard**: Xilinx Virtex-6 XC6VLX130T
- **Optional**: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

#### Custom I/O
- **Option -104**: Installs a front panel connector with 20 LVDS pairs to the FPGA

#### Memory
- **Option 150 or 160**: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165**: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

#### PCI-Express Interface
- **PCI Express Bus**: Gen. 1 x4 or x8; Gen. 2 x4

#### AMC Interface
- **Type**: AMC.1
- **Module Management**: IPMI Version 2.0

#### Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.

#### Size
- **Single-width, full-height AMC module, 2.89 in. x 7.11 in.
**General Information**

Model 56720 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As, and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56720 includes a front panel general-purpose connector for application-specific I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56760 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56720 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
D/A Waveform Playback IP Module

The 56720 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56720 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.
Model 56720
3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - AMC

Memory Resources
The 56720 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface
The Model 56720 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56720 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56720’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max.
- with interpolation
- Resolution: 16 bits

Front Panel Analog Signal Outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronizer: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX690T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI-Express Bus: Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

AMC Interface
- Type: AMC.1
- Module Management: IPMI Version 2.0

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
Model 56721 is a member of the Onyx family of high performance AMC boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for Gen. 1 and 2 PCI Express.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
A/D Acquisition IP Modules

The 56721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Core

In addition to the DDCs, the 56721 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56721’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 56721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56721’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

AMC Interface

The Model 56721 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
Memory Resources
The 56721 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.
In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 56721 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
Input: Transformer-coupled, front panel female SSMC connectors
Transformer: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters
Quantity: Three channels
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Signal: 2-channel real or 1-channel with frequency translation
Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
Resolution: 16 bits
Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Beamformer
Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit
Multiboard Summation Expansion: 32-bit
Front Panel Analog Signal Outputs
Output: Transformer-coupled, front panel female SSMC connectors
Transformers: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/sync/PPS inputs
Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
General Information

Model 56730 is a member of the Onyx® family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen.3 as a native interface, the Model 56730 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Module

The 56730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer is defined by a link definition in the IP module. The link is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 56730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The 56730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 56730 includes a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSps, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.
**Model 56730**

**1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - AMC**

### AMC Interface
The Model 56730 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

### PCI Express Interface
The Model 56730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

### Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals. The Pentek Model 5692 and Model 9192 Cobalt Synchronizers can drive multiple 56730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

### Memory Resources
The 56730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

### Specifications
**Front Panel Analog Signal Inputs**
- Input Type: Transformer-coupled, front panel female SSMC connectors
- A/D Converter Type: Texas Instruments ADS5400
  - Sampling Rate: 100 MHz to 1 GHz
  - Resolution: 12 bits
- D/A Converter Type: Texas Instruments DAC5681Z
  - Input Data Rate: 1 GHz max.
  - Interpolation Filter: bypass, 2x or 4x
  - Output Sampling Rate: 1 GHz max.
  - Resolution: 16 bits

**Front Panel Analog Signal Outputs**
- Output Type: Transformer-coupled, front panel female SSMC connectors

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
- **Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVDTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

**Memory**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

**AMC Interface**
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**Environmental**
- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Contact Pentek for availability of rugged and conduction-cooled versions**

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Tel: 201.818.5900 ● Fax: 201.818.5904 ● Email: info@pentek.com

[www.pentek.com](http://www.pentek.com)
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

General Information
Model 56741 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

- It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory.
- In addition to supporting PCI Express Gen. 3 as a native interface, Model 56741 includes an optional front-panel connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

- Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter.

Features
- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O. ➤
A/D Acquisition IP Module

The 56741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_a \), where \( f_a \) is the A/D sampling frequency. In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
Memory Resources

The 56741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

AMC Interface

The Model 56741 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

Model Description
56741 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - AMC

Options:
- 073 XC7VX330T-2 FPGA
- 076 XC7VX690T-2 FPGA
- 104 LVDS FPGA I/O to front panel connector

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Clocking and Synchronization

Supported Clock Sources: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
Model 56751

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC

General Information

Model 56751 is a member of the Onyx® family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56751 includes a general-purpose front-panel connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option-104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules

The 56751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

D/A Waveform Playback IP Module

The Model 56751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Oryx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course...

Model 56751
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Memory Resources

The 56751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 5650 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56751 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.
## Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters (standard)**
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

**A/D Converters (option -014)**
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

**Digital Downconverters**
- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

**Digital Interpolator**
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x
- **Total Interpolation Range (D/A and Digital combined):** 2x to 524,288x

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus**
- **Unique:** 26-pin connector LVPECL bus includes clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

**Memory**
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen.1 or Gen.2, x4 or x8

**AMC Interface**
- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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### Ordering Information

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<th>Model</th>
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<td>56751</td>
<td>2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and a Virtex-7 FPGA - AMC</td>
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**Options:**
- **-014:** 400 MHz, 14-bit A/Ds
- **-076:** XC7VX690T-2 FPGA
- **-104:** LVDS FPGA I/O through P14 connector
- **-105:** Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions.

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Pentek, Inc.  One Park Way ◆ Upper Saddle River ◆ New Jersey 07458  Tel: 201.818.5900 ◆ Fax: 201.818.5904 ◆ Email: info@pentek.com  www.pentek.com
General Information

Model 56760 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCIe Express Gen. 3 as a native interface, the Model 56760 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multinode synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-7 FPGA for custom I/O
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-Pcie configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a Pcie target for the host computer. In this mode, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts four full-scale analog HF or IF inputs on front panel SMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives...
4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - AMC

- an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56760’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56760 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 or 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: ±8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -073: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 56761 is a member of the Onyx® family of high-performance AMC boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. It features built-in support for Gen. 1 and 2 PCI Express.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 56761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.
A/D Acquisition IP Modules

The 56761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Beamformer IP Core

In addition to the DDCs, the 56761 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8k samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 56761’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from...
Model 56761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - AMC

➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

AMC Interface

The Model 56761 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Memory Resources

The 56761 architecture supports up to four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56761 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
Specifications

Front Panel Analog Signal Inputs
- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +8 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

A/D Converters
- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

Digital Downconverters
- **Quantity**: Four channels
- **Decimation Range**: 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution**: 32 bits
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation**: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain**: One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients**: I & Q with 16-bit resolution
- **Gain Coefficients**: 16-bit resolution
- **Channel Summation**: 24-bit
- **Multiboard Summation Expansion**: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus**: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type**: Front panel female SSMC connector, LVTTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard**: Xilinx Virtex-7 XC7VX330T-2
- **Optional**: Xilinx Virtex-7 XC7VX690T-2

Memory
- **Type**: DDR3 SDRAM
- **Size**: Four banks, 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus**: Gen. 1 or 2: x4 or x8

Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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<th>Model</th>
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<tr>
<td>56761</td>
<td>4-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - AMC</td>
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**Options:**
- 076  XC7VX690T-2 FPGA

*Contact Pentek for availability of rugged and conduction-cooled versions*
General Information

Model 56791 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board’s data and control paths are accessible by the FPGA, so to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 56791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 56791 can operate as a complete turnkey solution with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP within the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I-Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I-Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Modules

The 56791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.

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**A/D Acquisition IP Modules**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

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For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, the LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe. The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

AMC Interface

The Model 56791 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
## Specifications

### Front Panel Analog Signal Input
- **Connector:** Front panel female SSMC
- **Impedance:** 50 ohms

### L-Band Tuner
- **Type:** Maxim MAX2121
- **Input Frequency Range:** 925 MHz to 2175 MHz
- **Monolithic VCO Phase Noise:** $-97$ dBc/Hz at 10 kHz
- **Fractional-N PLL Synthesizer:**
  - $\text{freq}_{\text{VCO}} = (\text{N.F.}) \times \text{freq}_{\text{REF}}$
  - where integer $N = 19$ to 251 and fractional $F$ is a 20-bit binary value
- **PLL Reference ($\text{freq}_{\text{REF}}$):**
  - Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- **LNA Gain:** 60 dB range, controlled by a programmable 12-bit D/A converter
- **Usable Full-Scale Input Range:** $-50$ dBm to $+10$ dBm
- **Baseband Low Pass Filter:**
  - 3 dB cutoff frequency: 123.75 MHz

### A/D Converters
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 10 MHz to 500 MHz
- **Resolution:** 12 bits
- **Option -014:** 400 MHz, 14-bit A/Ds

### Sample Clock Sources:
- On-board timing generator/synthesizer

### A/D Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

### Timing Generator External Clock Input
- **Type:** Front panel female SSMC connector, sine wave, 0 to $+10$ dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

### Timing Generator Bus
- 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### External Trigger Input
- **Quantity:** 2
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

### Custom I/O
- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

### Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

### PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3*: x4 or x8

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

### Size:
- Standard XMC module, 2.91 in. x 5.87 in.

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### Ordering Information

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<td>L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - AMC</td>
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<tr>
<th>Options</th>
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<td>-076</td>
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<td>-100</td>
<td>27 MHz crystal for MAX2121</td>
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<tr>
<td>-104</td>
<td>LVDS FPGA I/O through front-panel connector</td>
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* Gen 3 requires a compatible backplane and SBC
General Information

Model 56131 is a member of the Jade family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through

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Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

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Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com

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Model 56131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC
A/D Acquisition IP Modules

The 56131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

> KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 56131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 56131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

PCI Express Interface

The Model 56131 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56131 complies with the AMC 1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters

- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >108 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **Timing Bus:** 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- **Option -104:** Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory

- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental

- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp:** -40° to 70° C
  - **Storage Temp:** -50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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<td>56131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC</td>
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</table>

Options:

- **-084:** XCKU060-2 FPGA
- **-087:** XCKU115-2 FPGA
- **-104:** LVDS FPGA I/O
- **-702:** Air cooled, Level L2
- **-713:** Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
General Information

Model 56132 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115.
8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

A/D Acquisition IP Modules

The 566862 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times \frac{f_s}{N} \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( \frac{f_s}{N} \).

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 5693 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications.
# Model 56132

## 8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

### PCI Express Interface

The Model 56132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### AMC Interface

The Model 56132 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

### Specifications

#### Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female MMCX connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

#### A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

#### Wideband Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

#### Multiband Digital Downconverters
- **Quantity:** Eight banks, 8 channels per bank
- **Decimation Range:** 16x to 1024x in steps of 8
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$, independent tuning for each channel
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

#### Sample Clock Sources
- **On-board clock synthesizer**

### Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

### External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

### Timing Bus
- **12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### External Trigger Input
- **Type:** Front panel female MMCX connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

### Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O

### Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

### PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

### Environmental
- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp:** -40° to 70° C
  - **Storage Temp:** -50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

### Ordering Information

<table>
<thead>
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<th>Model</th>
<th>Description</th>
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<td>56132</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC</td>
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**Options:**
- **-084** XCKU060-2 FPGA
- **-087** XCKU115-2 FPGA
- **-104** LVDS FPGA I/O through front-panel connector
- **-702** Air cooled, Level L2
- **-713** Conduction cooled, Level L3

*Contact Pentek for complete specifications of rugged and conduction-cooled versions*
Model 56141

General Information

Model 56141 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to RF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/A and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices ➤

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit DAs
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. • One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Module

The 56141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 56141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12J3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, inter-ppolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 56141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 56141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 56141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel μSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The μSync bus includes gate, reset, and in and out reference clock signals. The Model 5692 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Khansales@pentek.com
www.pentek.com

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201.818.5900 • Fax: 201.818.5904 • Email: info@pentek.com
Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A,
Kintex UltraScale FPGA - AMC

➤ AMC Interface
The Model 56141 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Ordering Information
Model Description
56141 1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

Pentek, Inc., One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

General Information

Model 56821 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 56821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 56821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 56821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_{os}$, where $f_{os}$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8\times f_{os}/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_{os}/N$.

D/A Waveform Playback IP Module

The Model 56821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

The 56821 supports user installed IP.
Model 56821

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 56821’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

AMC Interface

The Model 56821 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
## Specifications

### Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

### Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max.
- **Resolution:** 16 bits

### Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x
- **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

### Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

### Sample Clock Sources
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

### Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

### Synchronization
- VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

### Clock Dividers
- External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

### External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input or PLL system reference

### Timing Bus
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

### Custom I/O
- **Option -104** provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

### Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

### PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

### Environmental
- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp:** –40° to 70° C
  - **Storage Temp:** –50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

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**Contact Pentek for complete specifications of rugged and conduction-cooled versions**
Model 56841

**New!**

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - AMC

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### General Information

Model 56841 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

### The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

### Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

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**Pentek, Inc.**

One Park Way • Upper Saddle River • New Jersey 07458

Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 56841

**A/D Acquisition IP Module**

The 56841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \(0.8 \times f_s/N\), where \(N\) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \(f_s/N\).

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

**KINTEX ULTRASCALE FPGA DATAFLOW DETAIL**

*Two-Channel mode shown. Programmable decimation of 4, or 8 to 256 in steps of 8 available.*

**Notes:**

- and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

**Pentek, Inc.**

One Park Way • Upper Saddle River • New Jersey 07458

Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 56841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - AMC

Clocking and Synchronization

The 56841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync. A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 56841’s can be synchronized with a simple cable. For larger systems, multiple 56841’s can be synchronized using the Model 5692 high-speed sync board to drive the sync bus.

PCI Express Interface

The Model 56841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to S12 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$

LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104: Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for complete specifications of rugged and conduction-cooled versions.
Model 56851 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 56851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 56851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.
Model 56851

A/D Acquisition IP Modules

The 56851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

D/A Waveform Playback IP Module

The Model 56851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back the dual D/As waveforms stored in either on-board memory or off-board host memory.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463. The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

➡ Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 71851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

AMC Interface

The Model 56851 complies with the AMC1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - AMC

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)
- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)
- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters
- **Quantity:** Two channels
- **Decimation Range:** 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator Core
- **Interpolation Range:** 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
- **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

Front Panel Analog Signal Outputs
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

Sample Clock Sources:
- On-board clock
- D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Clock Dividers
- External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

Environmental
- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
- **Operating Temp:** -20° to 65° C
- **Storage Temp:** -40° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
- **Operating Temp:** -50° to 70° C
- **Storage Temp:** -50° to 100° C
- **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

Ordering Information

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<th>Model</th>
<th>Description</th>
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<td>56851</td>
<td>2-Channel 500 MHz A/D with DDCs, DUC, 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - AMC</td>
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Options:
- -014 400 MHz, 14-bit A/Ds
- -084 XCKU060-2 FPGA
- -087 XCKU115-2 FPGA
- -104 LVDS FPGA I/O to front-panel connector
- -702 Air cooled, Level L2
- -713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

General Information

Model 56861 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

New! New! New! New! New!
A/D Acquisition IP Modules

The 56861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
Model 56861

4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface

The Model 56861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface

The Model 56861 complies with the AMC1.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 32,768x in three stages of 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale XCKU035-2
  - Option -084: Xilinx Kintex UltraScale XCKU060-2
  - Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50°C
  - Storage Temp: −20° to 90°C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: −20° to 65°C
  - Storage Temp: −40° to 100°C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: −40° to 70°C
  - Storage Temp: −50° to 100°C
  - Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

Ordering Information

Model 56861
4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - AMC

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O to front-panel connector
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Ruggedized and conduction-cooled versions available

■ IPMI 2.0 compliant MMC
■ AMC 1 compliant
■ Optional LVDS connections
PCI Express (Gen. 1, 2 & 3)
LVPECL clock/sync bus for sample clock synchronization
5 GB of DDR4 SDRAM
32 multiband DDCs
Four wideband DDCs and four 200 MHz 16-bit A/Ds
Supports Xilinx Kintex
Complete radar and software test signal
controller (Module Management Controller)
Three clock synchronization functions; a test signal generator; and a PCIe interface. These functions enable the 56862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Model 56862 4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

General Information
Model 56862 is a member of the Jade family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 56862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

The 56862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 56862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other board resources.

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 56862

4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - AMC

➤ PCI Express Interface
The Model 56862 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface
The Model 56862 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Wideband Digital Downconverters
Quantity: Four channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Multiband Digital Downconverters
Quantity: Four banks, 8 channels per bank
Decimation Range: 2x to 1024x
LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$, independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Sources: On-board clock synthesizer
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2
Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.
Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: ~20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: ~20° to 65° C
Storage Temp: ~40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: ~40° to 70° C
Storage Temp: ~50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: Single-width, full-height AMC module 2.890 in x 7.110 in 73.40 mm x 180.60 mm

Ordering Information
Model Description
56862 4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - AMC
Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
-104 LVDS FPGA I/O to front-panel connector
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions
Model 56800 is a member of the Jade™ family of high-performance AMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today.

Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's interfaces. The 56800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Features

- Hi-performance coprocessor platform
- Supports Xilinx Kintex UltraScale FPGAs
- Front panel digital I/O can be used as a status and control or data interface
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS to the FPGA for custom I/O
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Front Panel Digital I/O Interface

The 56800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.
Memory Resources
The 56800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface
The Model 56800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

AMC Interface
The Model 56862 complies with the AMC.1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications
Front Panel Digital I/O
Connector Type: 80-pin connector, mates to a ribbon cable connector
Signal Quantity: 38 pairs
Signal Type: LVDS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.6 mm)

Ordering Information
56800 Kintex UltraScale FPGA Coprocessor - AMC

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions
General Information

The Bandit® Model 5620 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded AMC board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5620 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5620 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5620 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5620 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5620 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families. ➤
Bandit Two-Channel Analog RF Wideband Downconverter - AMC

**Specifications**

**RF Input**
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz

**RF Attenuator**: Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms

**Reference Input Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**Reference Output Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**OCXO Reference**
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm

**Aging**
- Daily: ±10 ppb/day
- First Year: ±300 ppb

**Total Frequency Tolerance**
- (20 years): ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 KH Offset: –148 dBc/Hz
- 10 KH Offset: –154 dBc/Hz
- 100 KH Offset: –155 dBc/Hz

**IF Output**
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12 VDC
- Current: 1.5 A

**PCI-Express Interface**
- PCI Express Bus: Gen. 1 x4 or x8, power only

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

**Size**: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>5620</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - AMC</td>
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<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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</table>
## MODEL DESCRIPTION

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>Cobalt 52620</td>
<td>3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Cobalt 52621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, 3U VPX</td>
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<tr>
<td>Cobalt 52624</td>
<td>Dual-Channel, 34-Signal Adaptive IF Relay - 3U VPX</td>
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<tr>
<td>Cobalt 52630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52640</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52641</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52650</td>
<td>Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52661</td>
<td>4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52662</td>
<td>4-Channel 200 MHz A/D with 32-Channel DDC and Virtex-6 FPGA - 3U VPX</td>
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<td>Cobalt 52663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 3U VPX</td>
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<td>Cobalt 52664</td>
<td>4-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 3U VPX</td>
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<td>Cobalt 52670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52671</td>
<td>4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Cobalt 52690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 52720</td>
<td>3-Channel 200 MHz A/D, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td>Onyx 52721</td>
<td>3-Channel 200 MHz A/D with DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 52730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 52741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 52751</td>
<td>2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA - 3U VPX</td>
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<td>Onyx 52760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Onyx 52761</td>
<td>4-Channel 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 3U VPX</td>
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<td>Onyx 52791</td>
<td>L-Band RF Tuner, 2-Channel 500 MHz A/D, Virtex-7 FPGA - 3U VPX</td>
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<tr>
<td>Jade 52131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 52132</td>
<td>8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 52141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 52821</td>
<td>3-Channel 200 MHz A/D, DDC, DUC 2-Channel 800 MHz D/A, Kintex UltraScale FPGA - 3U VPX</td>
</tr>
<tr>
<td>Jade 52841</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA - 3U VPX</td>
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<tr>
<td>Jade 52851</td>
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**Customer Information**

**RADAR & SDR I/O - PMC/XMC**

**RADAR & SDR I/O - CompactPCI**

**RADAR & SDR I/O - x8 PCI Express**

**RADAR & SDR I/O - AMC**

**RADAR & SDR I/O - 3U VPX - FORMAT 1**

**RADAR & SDR I/O - 6U VPX**

**RADAR & SDR I/O - FMC**

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*Last updated: March 2018*
General Information

Model 52620 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52620 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52620 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules, ideally matched to the board’s analog interfaces. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52620 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules
The 52620 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module
The Model 52620 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either onboard memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage
The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesize circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52620’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 52620 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the Virtex-6 FPGA.
Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model 8267
- 3U VPX Development System. See 8267 Datasheet for Options

Options:
- XC6VLX240T FPGA
- XC6VFX315T FPGA
- LVDS FPGA I/O to VPX P2
- Gigabit serial FPGA I/O to VPX P1
- Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 52621 is a member of the Cobalt\textsuperscript{®} family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

### The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52621 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52621 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

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**General Information**

Model 52621 is based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

### Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Optional LVPECL clock/sync bus for multiboard synchronization
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**General Information**

Model 52621 is based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52621 includes three A/Ds, one upconverter, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

### Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
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**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
A/D Acquisition IP Modules

The 52621 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board.

Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Core

In addition to the DDCs, the 52621 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52621’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VXI P1 connector. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 52621 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
Model 52621

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

A/D Converter Stage
The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to crate a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52621’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 52621 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 52621 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

- Digital Downconverters
  - Quantity: Three channels
  - Decimation Range: 2x to 65,536x in two stages of 2x to 256x
  - LO Tuning Freq. Resolution: 32 bits, 0 to 0.13 MHz
  - LO SFDR: >120 dB
  - Phase Offset Resolution: 32 bits, 0 to 360 degrees
  - FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
  - Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- D/A Converters
  - Type: Texas Instruments DAC5688
  - Input Data Rate: 250 MHz max.
  - Output IF: DC to 400 MHz max.
  - Output Signal: 2-channel real or 1-channel with frequency translation
  - Output Sampling Rate: 800 MHz max.
  - with 2x, 4x or 8x interpolation
  - Resolution: 16 bits

- Digital Interpolator
  - Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

- Beamformer
  - Summation: Three channels on-board; multiple boards can be summed via Summation Expansion Chain
  - Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
  - Phase Shift Coefficients: I & Q with 16-bit resolution
  - Gain Coefficients: 16-bit resolution
  - Channel Summation: 24-bit
  - Multiboard Summation Expansion: 32-bit

- Front Panel Analog Signal Outputs
  - Output: Transformer-coupled, front panel female SSMC connectors
  - Transformer: Coil Craft WBC4-6TLB
  - Full Scale Output: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

- Sample Clock Sources
  - On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

- Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus
  - 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
  - Standard: Xilinx Virtex-6 XC6VLX240T
  - Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
  - Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
  - Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  - Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
  - PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
  - Operating Temp: 0° to 95° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.
  - Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

VPX Development System. See 8267 Datasheet for Options
Model 52624 is a member of the Cobalt® family of high-performance 3U OpenVPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the module.

The 52624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen 1 system interface supports control, status and data transfers.

**Adaptive Relay Input Overview**

The Model 52624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted, or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

**Adaptive Relay Output Overview**

The Model 52624 output stage consists of 34 DUCs (digital upconverters) and two 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q signals from either the local DDCs or from system memory. DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stage. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation). The translated DUC outputs are directed to either of two summation blocks, each
associated with one of the two D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 DUCs.

**Xilinx Virtex-6 FPGA**

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the Model 52624 adaptive relay. Because of the complexity and proprietary nature of these functions, the FPGA cannot be extended or modified by the user.

**A/D Converters**

The front-end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for the data capture and all of the remaining adaptive relay signal processing operations.

**Digital Downconverters**

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to $0.8f_s/N$, where $N$ is the decimation setting and $f_s$ is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

**Input Gain Blocks**

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

**Receive DMA Controller**

Two output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2.

When a target memory buffer is filled, the 52624 issues an interrupt to the system processor and then begins filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

**Transmit DMA Controller**

Each of the FPGA-based 34 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, the 52624 signals the processor with an interrupt and moves to the next assigned buffer to continue fetching data.

**Output Gain Blocks**

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

**Digital Upconverters**

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.
Model 52624

Dual-Channel, 34-Signal Adaptive IF Relay - 3U OpenVPX

➤ A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to \( f_s \) where \( f_s \) is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

Summation Blocks

Two summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

D/A Converters

A TI DAC5688 dual-channel D/A accepts two summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to \( x4 \) mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two transformer-coupled analog IF outputs are delivered through a pair of front panel SSMC connectors.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52624’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

The Model 5264 includes an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

Form Factor Adaptors

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Quantity: Two
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits ➤
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Digital Downconverters
- Quantity: 34
- Decimation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >100 dB
- Phase Offset: 1 bit, 0 or 180 degrees
- FIR Filter: 18-bit coefficients
- Output: Complex, 16-bit I + 16-bit Q
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/-48 dB

Output Gain Blocks
- Quantity: 34
- Data: Complex, 16-bit I + 16-bit Q
- Gain Range: 16-bit Q8.8 format, approximately +/-48 dB

Digital Upconverters
- Quantity: 34
- Interpolation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- FIR Filter: 18-bit coefficients, 16-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Analog Output Channels: 2
- Type: Texas Instruments DAC5688
- Input Data Rate: 200 MHz max.
- Output Signal: Real
- Output Sampling Rate: 800 MHz max. with 4x interpolation
- Resolution: 16 bits

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock
- Clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Sources
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td># of XMCs</td>
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<td>Crossbar Switch</td>
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<td>VPX P1 or P2</td>
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<td>PCIe width</td>
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<td>x8</td>
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General Information

Model 52630 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ➤
A/D Acquisition IP Module

The 52630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 52630 features a Tl DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GS/s, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 5292 and Model 9192 Cobalt Synchronizers can drive multiple 52630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 52630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

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A/D Converter Stage

- The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.
- The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

- The 52630 features a Tl DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GS/s, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

- Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.
- Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Memory Resources

- The 52630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

- In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

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Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

PCI Express Interface
The Model 52630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock
External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen 2: x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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Model 52640

General Information

Model 52640 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Conversion Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 52640 accepts an 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals.

Multiple 52640’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 52640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s data transfer and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- **Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input
- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** −20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm).

Ordering Information

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<tr>
<td>52640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O to VPX P2
- **-105** Gigabit serial FPGA I/O to VPX P1
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

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</tbody>
</table>
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

General Information
Model 52641 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 52641 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52641 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52641 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

For applications that require additional control and status signals, option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Features
- Ideal radar and software radio interface solution
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Programmable one- or two-channel DDC (Digital Downconverter)
- PCI Express (Gen. 1 & 2) interface, up to x4
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

The 52641 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Clocking and Synchronization

The 52641 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 52641’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 52641 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.
# Model 52641

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D w/ Wideband DDC, Virtex-6 FPGA - 3U VPX

## PCI Express Interface
The Model 52641 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

## Specifications

### Front Panel Analog Signal Inputs
- **Input Type**: Transformer-coupled, front panel female SSMC connectors

### A/D Converter
- **Type**: Texas Instruments ADC12D1800
- **Sampling Rate**: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution**: 12 bits
- **Input Bandwidth**: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input**: +2 dBm to +4 dBm, programmable

### Digital Downconverters
- **Modes**: One or two channels, programmable
- **Supported Sample Rate**: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range**: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \)
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: User-programmable 18-bit coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

### Sample Clock Sources
- Front panel SSMC connector

### Sync Bus
- Multipin connectors, bus includes gate, reset and in and out reference clock

### External Trigger Input
- **Type**: Front panel female SSMC connector, TTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array
- **Xilinx Virtex-6 XC6VSX315T-2**

## Custom I/O
**Option -104**: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

**Memory**: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus**: Gen. 1 or Gen. 2: x4

## Environmental
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

## VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

### VPX Family Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>VPX P1 or P2</td>
<td>VPX P2</td>
</tr>
<tr>
<td>PCIe path</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td>Two x4 or one x8 on VPX P1</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

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**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
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<tr>
<td>52641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-002*</td>
<td>-2 FPGA speed grade</td>
</tr>
<tr>
<td>-064*</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td>-155*</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>-165*</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

*These options are always required

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**Contact Pentek for availability of rugged and conduction-cooled versions**

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<tbody>
<tr>
<td>8267</td>
<td>VPX Development System. See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>
Model 52650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52650 includes two A/Ds, one DUC (digital upconverter), two D/A and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52650 factory-installed functions include two A/D acquisition and one D/A waveform playback IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52650 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

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**General Information**

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 FPGA
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Two 500 MHz 12-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
The Model 52650 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfers, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate timestamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 52650 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**A/D Converter Stage**

The front end accepts two full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 52650 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the...
**PCI Express Interface**

The Model 52650 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

**Model** | **Description** |
---|---|
52650 | Two 500 MHz A/Ds, one DUC, Two 800 MHz D/As, Virtex-6 FPGA - 3U VPX |

**Options:**

- **-002** | -2 FPGA speed grade |
- **-014** | 400 MHz, 14-bit A/Ds |
- **-062** | XC6VLX240T FPGA |
- **-064** | XC6VSX315T FPGA |
- **-104** | LVDS FPGA I/O to VPX P2 |
- **-105** | Gigabit serial FPGA I/O to VPX P1 |
- **-150** | Two 8 MB QDR II+ SRAM Memory Banks (Banks 1 and 2) |
- **-160** | Two 8 MB QDR II+ SRAM Memory Banks (Banks 3 and 4) |
- **-155** | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2) |
- **-165** | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |

*This option is always required|

**Contact Pentek for availability of rugged and conduction-cooled versions**

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<tbody>
<tr>
<td>8267</td>
<td>VPX Development System. See 8267 Datasheet for Options</td>
</tr>
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</table>

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**Model 52650**

Two 500 MHz A/Ds, DUC, 800 MHz D/As, Virtex-6 FPGA - 3U VPX

- board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

- In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memory for many other purposes.

### Specifications

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

**A/D Converters (standard)**

- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

**D/A Converters**

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz, max.
- **Output IF:** DC to 400 MHz, max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz, max.
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**

- **Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

**Sample Clock Sources**

- **Type:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization**

- **VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz**

**Clock Dividers**

- **External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock**

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**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus**

- **26-pin front panel connector**
- **LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs**

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory**

- **Option 150 or 160:** Two 8 MB QDR II+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

**Environmental**

- **Operating Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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**VPX Families**

- Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<th>52xxx</th>
<th>53xxx</th>
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<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>3U VPX</td>
<td>3U VPX</td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
<td>x4</td>
<td>x8</td>
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<tr>
<td><strong>Option -104 path</strong></td>
<td>20 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
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<td>No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
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<td>No</td>
</tr>
</tbody>
</table>

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Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
Model 52651

2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

General Information

Model 52651 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52651 includes two A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52651 factory installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52651 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX31ST. The SX7 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVP ECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com

www.pentek.com
The 52651 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Each DDC core contains programable I & Q coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

In addition to the DDCs, the 52651 features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the two DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52651’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

The 52651 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**A/D Acquisition IP Modules**

**Beamformer IP Core**

**D/A Waveform Playback IP Module**
A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52651’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52651 architecture supports up to three independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52651 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (standard)
Type: Texas Instruments ADS5463
Sampling Rate: 20 MHz to 500 MHz
Resolution: 12 bits
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>52651</td>
<td>2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

- **-002** -2 FPGA speed grade
- **-014** 400 MHz, 14-bit A/Ds
- **-062** XC6VLX240 FPGA
- **-064** XC6VSX315 FPGA
- **-104** LVDS FPGA I/O through the VPX P2 connector
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

VPX Development System. See 8267 Datasheet for Options

A/D Converters (option -014)

- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits

Digital Downconverters

- **Quantity:** Two channels
- **Decimation Range:** 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- **LO Tuning Freq. Resolution:** 32 bits, 0 to f<sub>s</sub>
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution:** 16 bits

Digital Interpolator

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

Beamformer

- **Summation:** Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link over the FPGA and a Virtex-6 FPGA - 3U VPX

Option -104 path

- **Option -105 path**

Clock Sources

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

- **26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX240T-2
- **Optional:** Xilinx Virtex-6 XC6VSX315T-2

Custom I/O

- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory

- **Option -150:** Two 8 MB DDR3 SDRAM memory banks, 400 MHz DDR
- **Option -155 or -165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
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<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>3U VPX</td>
<td>One XMC</td>
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<tr>
<td><strong># of XMCs</strong></td>
<td>One XMC</td>
<td></td>
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<tr>
<td><strong>Crossbar Switch</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
General Information

Model 52660 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 52660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SX315T part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 52660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An onboard clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.
4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information

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<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>52660</td>
<td>4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
- 062 XC6VLX240T FPGA
- 064 XC6VXSX315T FPGA
- 104 LVDS FPGA I/O to VPX P2
- 105 Gigabit serial FPGA I/O to VPX P1
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
**General Information**

Model 52661 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter with a programmable DDC, it is suitable for connections to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52661 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52661 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52661 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**Model 52661 COTS (left) and rugged version**

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**Model 52661 4-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 3U VPX**
A/D Acquisition IP Modules

The 52661 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Core

In addition to the DDCs, the 52661 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The average constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage.

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Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458 Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com www.pentek.com
PCI Express Interface

The Model 52661 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe link up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a development system. The system is created to save engineers and system integrators the time and expense associated with building a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments AD55485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: $>$ 120 dB

FIR Filter
- Resolution: 18-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, $<$0.3 dB passband ripple, $>$100 dB stopband attenuation

Beamformer
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Sum Expansion: 32-bit

Sample Clock Sources
- On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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General Information

Model 52662 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed data converter with programmable DDCs (digital downconverters) is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution.

The 52662 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52662 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, a test signal generator, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable the 52662 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

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Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Modules

The 52662 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of the gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful 8-channel DDC bank. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all 32 DDC channels or each of the four A/Ds driving its own DDC bank.

Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to $f_{s}/8$, where $f_{s}$ is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192. The decimation range is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_{s}/N$, where $N$ is the decimation setting.

The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. For example, with a sampling rate of 200 MHz, the available output bandwidth range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of $f_{s}/N$. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleave that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52662 architecture supports up to four independent memory banks which can be configured with DDR3 SDRAM.
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

4-Ch 200 MHz A/D with 32-Ch DDC and Virtex-6 FPGA - 3U VPX

Model 82662

➤ Each DDR3 SDRAM bank can be up to 512 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory and capture space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52662 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters

Quantity: Four 8-channel banks, one per acquisition module
Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
LO Tuning Freq. Resolution: 32 bits, 0 to fs
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user-programmable coefficients
Default Filter Set: 80% bandwidth, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P1 connector to support serial and parallel protocols
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Crossbar Switch</td>
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<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<tr>
<td>PCIe width</td>
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<td>x8</td>
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<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td>Two x4 or x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
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General Information

Model 52663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 2 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 52663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 52663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x4
- 3U VPX form factor provides a compact, rugged platform
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 52663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 52663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

### Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 2 GB/sec peak rate of PCIe Gen 2 x4 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is slightly above the capability of the PCIe Gen 2 x4 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

### Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

### PCI Express Interface

The Model 52663 includes an industry-standard interface fully compliant with PCIe Express Gen. 2 bus specifications. Supporting PCIe links up to x4, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 52663 and host.
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank:** two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank:** 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing:** 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics:**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 kHz
  - > 96 dB attenuation at > ±3 MHz

DDC Output Rate f_s: Resampled to 180 MHz/13/2160 = 1.0833333 MS/sec

DDC Data Output Format:
- 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: -f_s/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +f_s/4 (+270.8333 kHz)
  - Fourth: +f_s/2 (+541.6666 kHz)

- **Superchannel Sample Rate:** f_s
- **Superchannel Output Format:** 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size:
- 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

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Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 52663

1100-Channel GSM Channelizer with Quad A/D - VPX

Ordering Information

Model 52663 | 1100-Channel GSM Channelizer with Quad A/D - VPX

Model 8267 | VPX Development System. See 8267 Datasheet for Options

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 52664 is a member of the Cobalt™ family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 52664 PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

The 52664 includes four A/Ds and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52664 factory-installed functions include four A/D acquisition IP modules.

Each of the four acquisition IP modules contains a powerful, programmable DDC (digital downconverter) IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52664 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Complete radar and software radio interface solution
- PCIe output supports VITA 49.0 Radio Transport (VRT) Standard
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs (digital downconverters)
- Multiboard programmable beamformer
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458 Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
A/D Acquisition IP Modules

The 52664 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to 8/f s where f s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f s/N.

Beamformer IP Core

In addition to the DDCs, the 52664 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52664s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the VPX P1 connector. This allows summation across channels on multiple boards.

VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA-49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

The 52664 supports fully the VITA 49.0 specification.
Model 52664

4-Ch. 200 MHz A/D w. DDCs, VITA 49.0, Virtex-6 FPGA - 3U VPX

➤ A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52664’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52664 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52664 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Four channels
- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- **Summation:** Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution
- **Channel Summation:** 24-bit
- **Multiboard Sum Expansion:** 32-bit

Sample Clock Sources
- **On-board clock synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), external clock or LVPECL timing bus

Clock Synthesizer
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus
- **26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX240T
- **Optional:** Xilinx Virtex-6 XC6VSX315T

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
General Information

Model 52670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 52670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
D/A Waveform Playback IP Module

The Model 52670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channels 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5292 or 9192 Cobalt Synchronizers can drive multiple 52670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 52670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x4 lane interface includes multiple DMA controllers for efficient transfers to and from the board.
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Specifications

D/A Converters
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs
Quantity: Four D/A outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Trigger Input
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS
Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
</tr>
</tbody>
</table>

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
--- | ---
52670 | 4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U VPX

Options:
-002* | -2 FPGA speed grade
-062 | XC6VLX240T FPGA
-064 | XC6VSX315T FPGA
-104 | LVDS FPGA I/O to VPX P2
-105 | Gigabit serial FPGA I/O to VPX P1
-155* | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions
4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

General Information

Model 52671 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As with a wide range of programmable interpolation factors, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 52671 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52671 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52671 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**Digital Upconverter and D/A Stage**

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 52671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. Analog output is through four front panel SSMC connectors.

**Clocking and Synchronization**

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5292 or 9192 Cobalt Synchronizers can drive multiple 52671 µSync connectors enabling large, multi-channel synchronous configurations.

**Memory Resources**

The 52671 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
4-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 3U VPX

PCI Express Interface
The Model 52671 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x4 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
D/A Converters
- Type: TI DAC3484
- Input Data Rate: 312.5 MHz max.
- Output Bandwidth: 250 MHz max.
- Output Sampling Rate: 1.25 GHz max. with interpolation
- Interpolation: 2x, 4x, 8x or 16x
- Resolution: 16 bits
Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Front Panel Analog Signal Outputs
- Quantity: Four D/A outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15
Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO or front panel external clock
- VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock
External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- Type: Front panel female SSMC connector
- Function: Programmable functions include: trigger, gate, sync and PPS
Timing Bus: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML
Field Programmable Gate Array:
- Standard: Xilinx Virtex-6 XC6VLX240T-2
- Optional: Xilinx Virtex-6 XC6VSX315T-2
Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Memory:
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
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<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
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<tr>
<td># of XMCs</td>
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<td>Crossbar Switch</td>
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<td>PCIe path</td>
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<td>PCIe width</td>
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<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
<td>Lowest Power</td>
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<td>No</td>
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<tr>
<td>Lowest Price</td>
<td>Yes</td>
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</table>
General Information

Model 52690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 52690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**A/D Clocking and Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 52690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

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**A/D Acquisition IP Modules**

The 52690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or from a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
PCI Express Interface

The Model 52690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building system and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model  Description
52690  L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX

Options:
-062  XC6VLX240T FPGA
-064  XC6VSX315T FPGA
-104  LVDS FPGA I/O to VPX P2
-105  Gigabit serial FPGA I/O to VPX P1
-150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuner
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:

PLL Reference (fref): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*

*Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Option -105 path</td>
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<tr>
<td>Lowest Power</td>
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<tr>
<td>Lowest Price</td>
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Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
General Information

Model 52720 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52720 includes three A/Ds, one upconverter, two D/A and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52720 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts three full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband...
3-Ch. 200 MHz A/D, 2-Ch. 800 MHz D/A, Virtex-7 FPGA - 3U VPX

Memory Resources
The Model 52720 supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

PCi Express Interface
The Model 52720 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards.

Ordering Information

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<td>3-Ch 200 MHz A/D and 2-Ch 800 MHz D/A with Virtex-7 FPGA - 3U VPX</td>
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<td></td>
<td>Options:</td>
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<tr>
<td>-073</td>
<td>XC7VX330T-2 FPGA</td>
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<tr>
<td>-076</td>
<td>XC7VX690T-2 FPGA</td>
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<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
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<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +9 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with interpolation
- Resolution: 16 bits

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.
- Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable VCXO. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the VCXO.

Memory Resources
- One XMC
- Memory: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

Environmental
- PCI-Express Interface: Gen. 1 or Gen. 2: x4

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<td>Lowest Price</td>
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</table>
Model 52721

3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX

General Information

Model 52721 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes three A/Ds, two D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52721 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an intrepolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52721 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs
- Two 800 MHz 16-bit D/As
- One DUC (digital upconverter)
- Multiboard programmable beamformer
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 52721 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Core

In addition to the DDCs, the 52721 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52721’s can be chained together via a built-in Xilinx Aurora giga-bit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The Model 52721 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.
Memory Resources

The 52721 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52721 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52721’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.
### Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-7 FPGA - 3U VPX</td>
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</table>

**Options:**
- -076 XC7VX690T-2 FPGA
- -104 LVDS FPGA I/O to VPX P2

**Contact Pentek for availability of rugged and conduction-cooled versions**

### Specifications

- **Front Panel Analog Signal Inputs**
  - **Input:** Transformer-coupled, front panel female SSMC connectors
  - **Transformer:** Coil Craft WBC4-6TLB
  - **Full Scale Input:** +8 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

- **A/D Converters**
  - **Type:** Texas Instruments ADS5485
  - **Sampling Rate:** 10 MHz to 200 MHz
  - **Resolution:** 16 bits

- **Digital Downconverters**
  - **Quantity:** Three channels
  - **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
  - **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
  - **LO SFDR:** >120 dB
  - **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
  - **FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients
  - **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- **D/A Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Signal:** 2-channel real or 1-channel with frequency translation
  - **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation
  - **Resolution:** 16 bits

- **Digital Interpolator**
  - **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x

- **Beamformer**
  - **Summation:** Three channels on-board; multiple boards can be summed via Summation Expansion Chain
  - **Summation Expansion Chain:** One chain in and one chain out link via XMC connector using Aurora protocol
  - **Phase Shift Coefficients:** I & Q with 16-bit resolution
  - **Gain Coefficients:** 16-bit resolution
  - **Channel Summation:** 24-bit Multibank Summation Expansion: 32-bit

- **Front Panel Analog Signal Outputs**
  - **Output:** Transformer-coupled, front panel female SSMC connectors
  - **Transformer:** Coil Craft WBC4-6TLB
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

- **Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

### Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

### External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

### Timing Bus

- **Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### Field Programmable Gate Array

- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

### Custom I/O

- **Option -104:** Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

### Memory

- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

### PCI-Express Interface

- **PCI Express Bus:** Gen. 1, 2 or 3: x4

### Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

### VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<th>VPX Family Comparison</th>
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<th>53xxx</th>
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<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
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<tr>
<td># of XMCs</td>
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<td>Crossbar Switch</td>
<td>No</td>
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<td>x4</td>
<td>x4 or x8</td>
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<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
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</table>
1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Model 52730

General Information
Model 52730 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Model 52730 COTS (left) and rugged version
**A/D Acquisition IP Module**

The 52730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 52730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The 52730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
Memory Resources

The 52730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface

The Model 52730 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<th>Description</th>
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<tbody>
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<td>52730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:

- 073   | XC7VX330T-2 FPGA                                 |
- 076   | XC7VX690T-2 FPGA                                 |
- 104   | LVDS FPGA I/O to VPX P1                         |
- 105   | Gigabit serial FPGA I/O to VPX P1               |

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phaselocked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX690T-2
Optional: Xilinx Virtex-7 XC7VX330T-2

Custom I/O

Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>53xxx</td>
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<td>Form Factor</td>
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<td>Option -105 path</td>
</tr>
<tr>
<td>Lower Cost</td>
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<tr>
<td>Lower Price</td>
</tr>
</tbody>
</table>

Pentek, Inc.

One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

General Information
Model 52741 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Module

The 52741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8*f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation, simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply...
Model 52741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Memory Resources
The 52741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FPGA memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface
The Model 52741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
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<td>XC7VX330T-2 FPGA</td>
</tr>
<tr>
<td>-076</td>
<td>XC7VX690T-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to fs
LO SFDR: >120 dB

Clocking and Synchronization
The 52741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

Environment
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 52751
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

General Information
Model 52751 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A two-channel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

The 52751 includes two A/Ds, two D/A channels and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52751 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O and Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/A channels
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the FPGA for custom I/O
- Optional 400 MHz 14-bit A/Ds
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
A/D Acquisition IP Modules
The 52751 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module
The Model 52751 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration
The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course 

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**Pentek, Inc.** One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-9900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters. Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be installed.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Memory Resources

The 52751 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52751 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3* bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.
2-Channel 500 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A and a Virtex-7 FPGA - 3U VPX

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (standard)
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

A/D Converters (option -014)
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

Digital Downconverters
- Quantity: Two channels
- Decimation Range: 2x to 131,072x in two programmable stages of 2x to 256x and one fixed 2x stage
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: >120 dB
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation
- Resolution: 16 bits

Digital Interpolator
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
- Total Interpolation Range (D/A and Digital combined): 2x to 524,288x

Front Panel Analog Signal Outputs
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -014: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -015: Provides one 8x or two 4x gigabit links between the FPGA and VPX P1 connector to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3*: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
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<tbody>
<tr>
<td>Form Factor</td>
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<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
<td>Lowest Price</td>
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* Gen 3 requires a compatible backplane and SBC

Contact Pentek for availability of rugged and conduction-cooled versions
Model 52760 COTS (left) and rugged version

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

General Information

Model 52760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52760 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules
The 52760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration
The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important in applications where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage
The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel.
PCI Express Interface

The Model 52760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options</th>
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<tbody>
<tr>
<td>52760</td>
<td>4-Channel 200 MHz A/D with Virtex-7 FPGA - 3U VPX</td>
<td>-073, -076, -104, -105</td>
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<td>Options:</td>
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<td>-073: XC7VX330T-2 FPGA -104: LVDS FPGA I/O to VPX P2 -105: Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267 Description

VPX Development System See 8267 Datasheet for Options

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz
- A/D Converters: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits
- Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus

- Type: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
<td># of XMCs</td>
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General Information

Model 52761 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter with programmable DDCs (Digital Downconverters), it is suitable for connection to HF or IF ports of a communications or radar system. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52761 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52761 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, a programmable beamforming IP core, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable the 52761 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
The 52761 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8\*fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit 1 + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of fs/N.

**Beamformer IP Core**

In addition to the DDCs, the 52761 features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 52761’s can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from GateXpress for FPGA Configuration.
Model 52761

4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX

➤ FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52761 architecture supports up to four independent DDR3 SDRAM memory banks.

Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52761 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformer
- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via XMC connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2
- Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
**Model 52791**

**L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX**

**General Information**

Model 52791 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52791 includes general purpose and gigabit serial connectors for application-specific I/O.

**The Onyx Architecture**

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 52791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

Thus, the 52791 can operate as a complete turnkey solution with no need to develop FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

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**Features**

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA handles L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverter provides IF or I+Q baseband signals at frequencies up to 123 MHz
- Two 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x4
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

---

**Model 52791 COTS (left) and rugged version**

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**Pentek, Inc.**, One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

The 52791 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Both memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters and DDCs

The two analog tuner outputs are digitized by two Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two independent A/D and DDC channels are now available for digitizing and downconverting two signals with different center frequencies and bandwidths.

A/D Clocking & Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front-panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52791 architecture supports four independent 1 GB DDR3 SDRAM for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 and 2. Banks 3 and 4 can be used to support custom user-installed IP within the FPGA.

PCI Express Interface

The Model 52791 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.
L-Band RF Tuner, 2-Chan. 500 MHz A/D, Virtex-7 FPGA - 3U VPX

Specifications

Front Panel Analog Signal Input
- Connector: Front panel female SSMC
- Impedance: 50 ohms

L-Band Tuner
- Type: Maxim MAX2121
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer:
  \[ \text{freqVCO} = (N\text{.F}) \times \text{freqREF} \]
  where integer \( N = 19 \) to 251 and fractional \( F \) is a 20-bit binary value
- PLL Reference (freqREF):
  - Front panel SSMC connector or on-board 27 MHz crystal (Option -100)
  - 12 to 30 MHz
- LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
- Usable Full-Scale Input Range: -50 dBm to +10 dBm
- Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

A/D Converters
- Type: Texas Instruments ADS5463
- Sampling Rate: 10 MHz to 500 MHz
- Resolution: 12 bits
- Option -014: 400 MHz, 14-bit A/Ds
- Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Quantity: 2
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and VPX P1 connector to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3*: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td></td>
</tr>
<tr>
<td># of XMCs</td>
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<td>1</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x4 or x8</td>
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<tr>
<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

* Gen 3 requires a compatible backplane and SBC

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:
- -014 400 MHz, 14-bit A/Ds
- -076 XC7VX690T-2 FPGA
- -100 27 MHz crystal for MAX2121
- -104 LVDS FPGA I/O to VPX P2
- -105 Gigabit serial FPGA I/O to VPX P1

Ordering Information

Model | Description
--- | ---
52791 | L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:
- -014 400 MHz, 14-bit A/Ds
- -076 XC7VX690T-2 FPGA
- -100 27 MHz crystal for MAX2121
- -104 LVDS FPGA I/O to VPX P2
- -105 Gigabit serial FPGA I/O to VPX P1

8267 | VPX Development System
- See 8267 Datasheet for Options

VPX Family Comparison

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<td># of XMCs</td>
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<td>1</td>
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<td>Crossbar Switch</td>
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<td>Yes</td>
</tr>
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<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

* Gen 3 requires a compatible backplane and SBC
General Information

Model 52131 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52131 is a multichannel, high-speed data converter with multiband DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, multiband DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52131 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through...
A/D Acquisition IP Modules

The 52131 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_o \) where \( f_o \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_o/N \), where \( N \) is the decimation setting. The rejection of adjacent band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_o/N \).

KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects one 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front panel MMCX connectors with transformer-coupling into four Texas Instruments ADS42L69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal-processing or routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The 52131 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

![Diagram of Model 52131](image-url)
Model 52131

8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

**Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type**: Transformer-coupled, front panel female MMCX connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters**

- **Type**: Texas Instruments ADS42LB69
- **Sampling Rate**: 10 MHz to 250 MHz
- **Resolution**: 16 bits

**Digital Downconverters**

- **Quantity**: Eight channels
- **Decimation Range**: 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to f_s
- **LO SFDR**: >108 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources**

- **On-board clock synthesizer**

**Clock Synthesizer**

- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization**

- VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers**

- **External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock**

**External Clock**

- **Type**: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus**

- **12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs**

**External Trigger Input**

- **Type**: Front panel female MMCX connector, LVTTL

**Field Programmable Gate Array**

- **Standard**: Xilinx Kintex UltraScale
- **Option -084**: Xilinx Kintex UltraScale
- **Option -087**: Xilinx Kintex UltraScale

**Custom I/O**

- **Option -104**: Connects 24 LVDS pairs between the FPGA and VPX P2
- **Option -105**: Connects eight gigabit serial lanes between the FPGA and VPX P1

**VPX Families**

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52131</td>
<td>8-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Options</th>
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</thead>
<tbody>
<tr>
<td>-084</td>
<td>XCKU060-2 FPGA</td>
</tr>
<tr>
<td>-087</td>
<td>XCKU115-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O</td>
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<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O</td>
</tr>
<tr>
<td>-702</td>
<td>Air cooled, Level 2</td>
</tr>
<tr>
<td>-713</td>
<td>Conduction cooled, Level 3</td>
</tr>
</tbody>
</table>

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

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*Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458 • Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com • www.pentek.com*
General Information
Model 52132 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52132 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52132 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52132 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52132 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA
The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU115.
A/D Acquisition IP Modules

The 52132 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each acquisition module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC has its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 5293 System Synchronizer supports additional boards in increments of eight.

Memory Resources

The architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of it for custom applications.
8-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 3U VPX

PCI Express Interface

The Model 52132 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped for optimum performance.

Ordering Information

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<tr>
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<th>Options:</th>
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<td>52132</td>
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<td></td>
</tr>
<tr>
<td>-084</td>
<td>XCKU060-2 FPGA</td>
<td>x8, x16</td>
</tr>
<tr>
<td>-087</td>
<td>XCKU115-2 FPGA</td>
<td>x4, x8, x16</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O through VPX P2</td>
<td>x1, x2, x4</td>
</tr>
<tr>
<td>-105</td>
<td>Gigabit serial I/O through VPX P1 connector</td>
<td>x1, x2, x4</td>
</tr>
<tr>
<td>-702</td>
<td>Air cooled, Level L2</td>
<td>x2, x4</td>
</tr>
<tr>
<td>-713</td>
<td>Conduction cooled, Level L3</td>
<td>x1, x2, x4</td>
</tr>
</tbody>
</table>

Specifications

Front Panel Analog Signal Inputs
- **Input Type**: Transformer-coupled, front panel female MMCX connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

A/D Converters
- **Type**: Texas Instruments ADS42LB69
- **Sampling Rate**: 10 MHz to 250 MHz
- **Resolution**: 16 bits

Wideband Digital Downconverters
- **Quantity**: Eight channels
- **Decimation Range**: 2x to 32x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \)
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
- **Quantity**: Eight banks, 8 channels per bank
- **Decimation Range**: 2x to 1024x in steps of 8
- **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \) independent tuning for each channel
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source**: Selectable from on-board programmable VXCO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VXCO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VXCO can be divided by 1, 2, 4, 8, or 16 for the \( A/D \) clock

External Clock
- **Type**: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type**: Front panel female MMCX connector, LVTTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Option -084**: Xilinx Kintex UltraScale XCKU060-2
- **Option -087**: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104**: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105**: Provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- **Type**: DDR4 SDRAM
- **Size**: 5 GB
- **Speed**: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus**: Gen. 1, 2 or 3: x4

Environmental
- **Standard**: L0 (air cooled)
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Option -702**: L2 (air cooled)
- **Operating Temp**: -20° to 65° C
- **Storage Temp**: -40° to 100° C
- **Option -713**: L3 (conduction cooled)
- **Operating Temp**: -40° to 70° C
- **Storage Temp**: -50° to 100° C
- **Relative Humidity in all cases**: 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>3U VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
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<tr>
<td>Form Factor</td>
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<tr>
<td># of XMCs</td>
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<tr>
<td>Crossbar Switch</td>
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<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
General Information

Model 52141 is a member of the Jade™ family of high-performance PCIe modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.
D/A Waveform Generator IP Module

The 52141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 52141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

A/D Acquisition IP Module

The 52141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

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For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

Memory Resources

The 52141 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 52141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information

Model  Description
52141  1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:
- 084  XCKU060-2 FPGA
- 087  XCKU115-2 FPGA
- 104  LVDS FPGA I/O
- 105  Gigabit serial FPGA I/O
- 702  Air cooled, Level L2
- 713  Convection cooled, Level L3

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz
Resolution: 14 bits

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale
Option -084: Xilinx Kintex UltraScale
Option -087: Xilinx Kintex UltraScale

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

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<td>6U VPX</td>
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<td># of XMCs</td>
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<td>VPX P1</td>
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<td>PCIe width</td>
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<td>x8</td>
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<td>Two x4 or one x8 on VPX P1</td>
<td>24 pairs on VPX P2</td>
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<td>No</td>
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<tr>
<td>Lowest Price</td>
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<td>No</td>
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General Information

Model 52821 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a stream-lined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52821 is a 3-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three 200 MHz 16-bit A/Ds
- Three multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 52821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52821 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.
A/D Acquisition IP Modules

The 52821 features three A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage

The front end accepts three analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

D/A Waveform Playback IP Module

The Model 52821 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.
When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52821’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 52821 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface
The Model 52821 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits
3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

**Digital Downconverters**
- **Quantity:** Two channels
- **Decimation Range:** 2x to 32,768x in three stages of 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters**
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Signal:** 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate:** 800 MHz max.
- **Resolution:** 16 bits

**Digital Interpolator Core**
- **Interpolation Range:** 2x to 32,768x in three stages of 2x to 32x
- **Total Interpolation Range (D/A and interpolator core combined):** 2x to 262,144x

**Front Panel Analog Signal Outputs**
- **Output:** Transformer-coupled, front panel female SSMC connectors
- **Transformer:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:** On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Array**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2

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**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

### 3U VPX Family Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x4 or x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>24 pairs</td>
<td>24 pairs or VPX P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>One x1 on VPX P1</td>
<td>One x1 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

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**Contact Pentek for complete specifications of rugged and conduction-cooled versions**
Model 52841 COTS (left) and rugged version

General Information

Model 52841 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52841 is a high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including:
  - VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

New! New! New! New! New!
**A/D Acquisition IP Module**

The 52841 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has an associated 5 GB memory bank for buffer data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8.

In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-channel components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

**PCI Express Interface**

The Model 52841 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module. ➤
Model 52841

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a 4U rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Memory Resources

The 52861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Ordering Information

Model  Description
52841  1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Kintex UltraScale FPGA - 3U VPX

Options:
- 084  XCKU060-2 FPGA
- 087  XCKU115-2 FPGA
- 104  LVDS FPGA I/O
- 105  Gigabit serial FPGA I/O
- 204  XCKU035-2 FPGA
- 102  Air cooled, Level L2
- 713  Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Clocking and Synchronization

The 52841 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync. A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 52841’s can be synchronized with a simple cable. For larger systems, multiple 52841’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
- Type: Texas Instruments ADC12D1800
- Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- Resolution: 12 bits
- Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer

Digital Downconverters
- Modes: One or two channels, programmable
- Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- Single-channel mode: decimation can be programmed to 8 to 16 to 512 in steps of 16
- Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value

Either mode: the DDC can be bypassed completely
- LO Tuning Freq.
  - Resolution: 32 bits, 0 to \( f_s \)
  - LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- Type: Front panel female SSMC connector, LV TTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale
- Option -084: Xilinx Kintex UltraScale
- Option -087: Xilinx Kintex UltraScale

Custom I/O
- Option -104: Connects 24 LVDS pairs between the FPGA and VPX P2
- Option -105: Connects eight gigabit serial lanes between the FPGA and VPX P1

Memory
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4
- Subject to speed limitations of backplane and SBC

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -713: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>53xxx</td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>Yes</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<tr>
<td>Option -105 path</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
Model 52851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52851 is a 2-channel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The 52851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52851 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Two 500 MHz 12-bit A/Ds
- Two multiband DDCs (digital downconverters)
- One DUC (digital upconverter)
- Two 800 MHz 16-bit D/As
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Optional 400 MHz 14-bit A/Ds
- Ruggedized and conduction-cooled versions available

New! New! New! New! New!

Model 52851 COTS (left) and rugged version
Model 52851

A/D Acquisition IP Modules

The 52851 features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output band-widths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

A/D Converter Stage

The front end accepts two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, a Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.

D/A Waveform Playback IP Module

The Model 71851 factory-installed functions include a sophisticated D/A Waveform Playback IP module. It allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.
Model 52851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52851 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52851 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +5 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters (standard)

- **Type:** Texas Instruments ADS5463
- **Sampling Rate:** 20 MHz to 500 MHz
- **Resolution:** 12 bits

A/D Converters (option -014)

- **Type:** Texas Instruments ADS5474
- **Sampling Rate:** 20 MHz to 400 MHz
- **Resolution:** 14 bits ➤
2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Model 52851

2-Channel 500 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A and Kintex UltraScale FPGA - 3U VPX

- Digital Downconverters
  - Quantity: Two channels
  - Decimation Range: 2x to 65,536x in three stages of 2x to 32x and one fixed stage of 2x
  - LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
  - LO SFD: >120 dB
  - Phase Offset Resolution: 32 bits, 0 to 360 degrees
  - FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
  - Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

- Digital Interpolator Core
  - Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x
  - Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x

- Front Panel Analog Signal Outputs
  - Output: Transformer-coupled, front panel female SSMC connectors
  - Transformer: Coil Craft WBC4-6TLB
  - Full Scale Output: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

- Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

- Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

- Clock Dividers
  - External clock or VCXO can be divided or reconfigured for the A/D clock and D/A clock

- External Clock
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

- Option -104: Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols

Memory

- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -713: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

- Size: 3U VPX board 3.937 in x 6.717 in (100.00 mm x 170.61 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<tr>
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Contact Pentek for complete specifications of rugged and conduction-cooled versions.

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201.818.5900 ● Fax: 201.818.5904 ● Email: info@pentek.com  www.pentek.com
4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

General Information

Model 52861 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52861 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multiboard clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52861 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52861 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52861 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four multiband DDCs
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 52861 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52861 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 3U VPX

PCI Express Interface
The Model 52861 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters
- Quantity: Four channels
- Decimation Range: 2x to 32,768x in three stages of 2x to 32x
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources
- On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale
- XCKU035-2
- Option -084: Xilinx Kintex UltraScale
- XCKU060-2
- Option -087: Xilinx Kintex UltraScale
- XCKU115-2

Custom I/O
- Option -0104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- Option -0105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
- Type: DDR4 SDRAM
- Size: 3 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4

Environmental
- Standard: L0 (air cooled)
- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-condensing
- Option -0702: L2 (air cooled)
- Operating Temp: -20° to 65°C
- Storage Temp: -40° to 100°C
- Relative Humidity: 0 to 95%, non-condensing
- Option -0713: L3 (conduction cooled)
- Operating Temp: -40° to 70°C
- Storage Temp: -50° to 100°C
- Relative Humidity: 0 to 95%, non-condensing

Size: Board 3.937 in. x 6.717 in. (100.0 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
General Information

Model 52862 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52862 is a multichannel, high-speed data converter with programmable DDCs (digital downconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes four A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52862 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52862 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and transfer.

Each of the four acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 52862 to operate as a complete turnkey solution for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four 200 MHz 16-bit A/Ds
- Four wideband DDCs and 32 multiband DDCs (digital downconverters)
- 5 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x4
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

**A/D Acquisition IP Modules**

The 52862 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module are two powerful DDC cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filters for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit 1 + 16-bit Q samples at a rate of \( f_s/N \).

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

**A/D Converter Stage**

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGA for signal processing or routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 52862 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
4-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - XMC

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
5 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments AD5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Wideband Digital Downconverters
Quantity: Four channels
Decimation Range: 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Multiband Digital Downconverters
Quantity: Four banks, 8 channels per bank
Decimation Range: 2x to 1024x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s independent tuning for each channel
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50°C
Storage Temp: -20° to 90°C
Option -702: L2 (air cooled)
Operating Temp: -20° to 65°C
Storage Temp: -40° to 100°C
Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70°C
Storage Temp: -50° to 100°C
Relative Humidity in all cases: 0 to 95%, non-condensing
Size: Board 3.937 in. x 6.717 in.
(100.0 mm x 170.6 mm

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, refer to its datasheet. The table below provides a comparison of their main features.

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Model 52800 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA based boards, simplifying the design to reduce power and cost, while still providing some of the highest performance FPGA resources available today.

Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data processing IP.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 52800 includes optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The 52800 factory-installed functions include a test signal generator, a metadata generator, a DDR4 SDRAM controller, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocalls.

Front Panel Digital I/O Interface

The 52800 includes an 80-pin front panel connector that provides 38 LVDS pairs connected to the FPGA. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.
**Model 52800**

**Kintex UltraScale FPGA Coprocessor-3U VPX**

**Specifications**

**Front Panel Digital I/O**
- **Connector Type:** 80-pin connector, mates to a ribbon cable connector
- **Signal Quantity:** 38 pairs
- **Signal Type:** LVDS

**Field Programmable Gate Array**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104** connects 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105** connects an 8X gigabit serial link from the FPGA to the VPX P1 connector to support serial protocols.

**Memory**
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

**Environmental**
- **Standard:** L0 (air cooled)
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Option -702:** L2 (air cooled)
- **Operating Temp:** –20° to 65° C
- **Storage Temp:** –40° to 100° C
- **Option -713:** L3 (conduction cooled)
- **Operating Temp:** –40° to 70° C
- **Storage Temp:** –50° to 100° C
- **Relative Humidity in all options:** 0 to 95%, non-condensing

**Size:** 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

**Memory Resources**

The 52800 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

**SPARK Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8264), or a 6U VPX chassis (Model 8267), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>52800</td>
<td>Kintex UltraScale FPGA Coprocessor-3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- **-084** XCKU060-2 FPGA
- **-087** XCKU115-2 FPGA
- **-104** LVDS FPGA I/O
- **-105** Gigabit serial FPGA I/O
- **-702** Air cooled, Level L2
- **-713** Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

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New!

**PCI Express Interface**

The Model 52800 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

---

**Memory**

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

**Environmental**

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: –20° to 90° C

Option -702: L2 (air cooled)

Operating Temp: –20° to 65° C

Storage Temp: –40° to 100° C

Option -713: L3 (conduction cooled)

Operating Temp: –40° to 70° C

Storage Temp: –50° to 100° C

Relative Humidity in all options: 0 to 95%, non-condensing

Size: 3U VPX card 3.937 in x 6.717 in (100.00 mm x 149.00 mm)
Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

General Information

The Bandit® Model 5220 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded 3U VPX board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5220 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5220 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5220 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5220 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5220 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
## Specifications

### RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** -60 dBm to -20 dBm
- **Flatness:** ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- **RF Attenuator:** Programmable from 0 to 63 dB in 0.5 dB steps

### LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz

### Phase Noise
- **1 kHz Offset:** −90 dBc/Hz
- **100 kHz Offset:** −110 dBc/Hz
- **1 MHz Offset:** −130 dBc/Hz

### Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

### Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

### Reference Input/Output
- **Connector Type:** SSMC
- **Input/Output Impedance:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave
- **Reference Output Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

### OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm

### Aging
- **Daily:** ±10 ppb/day
- **First Year:** ±300 ppb
- **Total Frequency Tolerance (20 years):** ±4.60 ppm

### Phase Noise
- **1 Hz Offset:** −67 dBc/Hz
- **10 Hz Offset:** −100 dBc/Hz
- **100 Hz Offset:** −130 dBc/Hz
- **1 KHz Offset:** −148 dBc/Hz
- **10 KHz Offset:** −154 dBc/Hz
- **100 KHz Offset:** −155 dBc/Hz

### IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

### Programming
- **Functions:** RF Atten, IF Atten, Int/Ext
- **Reference Select, LO Synthesizer Frequency Interface:** USB
- **Connector Type:** MicroUSB

### Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

### PCI Express Interface
- **PCIe Bus:** x4, power only

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** −20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

## Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>5220</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

General Information
The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19” 4U rackmount chassis that is 12” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options
Available options include high-end multi-core CPUs and extended memory support.

Specifications
- Operating System: 64-bit Windows 7 Professional or Linux
- Processor: Intel Core i7 processor
- Clock Speed: 3.6 GHz
- SDRAM: 16 GB standard
- Dimensions: 4U Chassis, 19" W x 12" D x 7" H
- Weight: 35 lb, approx.
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>8267</td>
<td>3U VPX Development System for Cobalt, Onyx and Flexor Boards</td>
</tr>
</tbody>
</table>

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS
-101 Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458  www.pentek.com
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
# Radar & SDR I/O - 6U VPX

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cobalt 57620 &amp; 58620</td>
<td>3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57621 &amp; 58621</td>
<td>3/6-Ch 200 MHz A/D, DDCs, DUC, 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57624 &amp; 58624</td>
<td>2- or 4-Channel, 34- or 68-Signal Adaptive IF Relay - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57630 &amp; 58630</td>
<td>1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57640 &amp; 58640</td>
<td>1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57641 &amp; 58641</td>
<td>1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, DDC, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57650 &amp; 58650</td>
<td>2/4 500 MHz A/Ds, 1/2 DUCs, 2/4 800 MHz D/A, Virtex-6 FPGA - 6U VPX</td>
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<tr>
<td>Cobalt 57651 &amp; 58651</td>
<td>2/4-Ch 500 MHz A/D w. DDC, DUC w. 2/4-Ch 800 MHz D/A, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57660 &amp; 58660</td>
<td>4/8-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57661 &amp; 58661</td>
<td>4/8-Ch 200 MHz A/D with DDCs, Beamformer and Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57662 &amp; 58662</td>
<td>8-Ch 200 MHz A/D with 32/64-Ch DDC and Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57663 &amp; 58663</td>
<td>1100/2200-Channel GSM Channelizer with Quad or Octal A/D - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57664 &amp; 58664</td>
<td>4/8-Channel 200 MHz A/D with DDCs, VITA-49, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57667 &amp; 58667</td>
<td>4/8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57671 &amp; 58671</td>
<td>4/8-Ch 1.25 GHz D/A with DUC, Extend. Interpol. and Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57672 &amp; 58672</td>
<td>1/2-Ch L-Band RF Tuner, 2/4-Ch 200 MHz A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 57673 &amp; 58673</td>
<td>3/6-Ch 200 MHz A/D, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57720 &amp; 58720</td>
<td>3/6-Ch 200 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57721 &amp; 58721</td>
<td>1/2-Ch 1 GHz A/D and 1/2-Ch 1 GHz D/A, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57730 &amp; 58730</td>
<td>1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57741 &amp; 58741</td>
<td>1/2-Ch 3.6 GHz or 2/4-Ch 1.8 GHz 12-bit A/D, DDC, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57751 &amp; 58751</td>
<td>2/4-Ch 500 MHz A/D, DDC, DUC, 2/4-Ch 800 MHz D/A, Virtex-7 FPGA - 6U VPX</td>
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<tr>
<td>Onyx 57760 &amp; 58760</td>
<td>4/8-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57761 &amp; 58761</td>
<td>4-Channels 200 MHz, 16-bit A/D with DDCs and Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57791 &amp; 58791</td>
<td>2-Channel 500 MHz A/D, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57131 &amp; 58131</td>
<td>8-Channels 250 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57132 &amp; 58132</td>
<td>8-Channels 250 MHz A/D with Multiband DDCs and Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57141 &amp; 58141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, and Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57821 &amp; 58821</td>
<td>3-Channels 200 MHz A/D, DDC, DUC and Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57841 &amp; 58841</td>
<td>3-Channels 200 MHz A/D, DDC, 2-Channel 800 MHz D/A, Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57851 &amp; 58851</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57861 &amp; 58861</td>
<td>2-Ch. 500 MHz A/D, DDC, DUC, 2-Ch. 800 MHz D/A, Kintex FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57862 &amp; 58862</td>
<td>4-Channels 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 57800 &amp; 58800</td>
<td>4-Channels 200 MHz A/D with Multiband DDCs, Kintex Ultrascale FPGA - 6U VPX</td>
</tr>
<tr>
<td>Jade 8264</td>
<td>Development System for 6U VPX Cobalt, Onyx, Jade, Flexor, and Jade boards</td>
</tr>
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Customer Information

RADAR & SDR I/O - PMC/XMC
RADAR & SDR I/O - CompactPCI
RADAR & SDR I/O - x8 PCI Express
RADAR & SDR I/O - 3U VPX - FORMAT 1
RADAR & SDR I/O - AMC
RADAR & SDR I/O - 3U VPX - FORMAT 2
RADAR & SDR I/O - FMC

Last updated: March 2018
General Information

Models 57620 and 58620 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71620 XMC modules mounted on a VPX carrier board.

Model 57620 is a 6U board with one Model 71620 module while the Model 58620 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, one or two DUCs, two or four D/A and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocks and synchronization functions, a test signal generator, and an PCIe interface complete the factory-installed functions and enable these models to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SXT315T. The XRT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57620; P3 and P5, Model 58620.

Option -105 supports serial protocols by providing a 4x gigabit link between the FPGA and VPX P2, Model 57620; or one 4x link from each FPGA to P2 and an additional 4x link between the FPGAs, Model 58620. 

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Three or six 200 MHz 16-bit A/Ds
- One or two DUCs (Digital Upconverters)
- Two or four 800 MHz 16-bit D/A
- 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64 MB of QDRII+ SRAM
- PCIe Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the three A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes, the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

![Virtex-6 FPGA Dataflow Detail](image-url)
Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tr>
<td>57620</td>
<td>3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58620</td>
<td>6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
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Options:
- 062  
  XC6VLX240T FPGA
- 064  
  XC6VSX315T FPGA
- 104  
  LVDS I/O between the FPGA and P3 connector, Model 57620; P3 and P5 connectors, Model 58620
- 105  
  Gigabit link between the FPGA and P2 connector, Model 57620; gigabit links from each FPGA to P2 connector, Model 78620
- 150  
  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160  
  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155  
  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165  
  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

- Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.
- In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

- These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Sample Clock Sources (2 or 4)
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference
- Timing Bus (1 or 2): 26-pin connector
- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57620; P3 and P5, Model 58620
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57620; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58620

Memory Banks (1 or 2)
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks. 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1 or 2: x4 or x8
- Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**General Information**

Models 57621 and 58621 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71621 XMC modules mounted on a VPX carrier board.

Model 57621 is a 6U board with one Model 71621 module while the Model 58621 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, three or six multiband DDCs, one or two DUCs, two or four D/As and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, one or two programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57621; P3 and P5, Model 58621.
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the three DCC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via the built-in Xilinx Aurora gigabit serial interfaces through the VPX P2 connectors. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Modules

The factory-installed functions include sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.
3 or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, with Virtex-6 FPGA - 6U OpenVPX

**A/D Converter Stage**

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture and for routing to other module resources.

**Digital Upconverter and D/A Stage**

One or two TI DAC5688 DUCs (digital upconverters) and D/A s accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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### Ordering Information

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<th>Model</th>
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<tr>
<td>57621</td>
<td>3-Channel 200 MHz A/D with DDC, DUC with 2-Channel 800 MHz D/A, and a Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58621</td>
<td>6-Channel 200 MHz A/D with DDCs, DUCs with 4-Channel 800 MHz D/A, and two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57621; P3 and P5 connectors, Model 58621
- **-150** Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-160** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

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**Specifications**

**Model 57621:** 3 A/Ds, 3 DDCs, 1 DUC, 2 D/As  
**Model 58621:** 6 A/Ds, 6 DDCs, 2 DUCs, 4 D/As  

**Front Panel Analog Signal Inputs (3 or 6)**  
*Input Type:* Transformer-coupled, front panel female SSMC connectors  
*Transformer Type:* Coil Craft WBC4-6TLB  
*Full Scale Input:* +8 dBm into 50 ohms  
*3 dB Passband:* 300 kHz to 700 MHz  

**A/D Converters (3 or 6)**  
*Type:* Texas Instruments ADS5485  
*Sampling Rate:* 10 MHz to 200 MHz  
*Resolution:* 16 bits  

**Digital Downconverters (3 or 6)**  
*Decimation Range:* 2x to 65,536x in two stages of 2x to 256x  
*LO Tuning Freq. Resolution:* 32 bits, 0 to $f_s$  
*LO SFDR:* >120 dB  
*Phase Offset Resolution:* 32 bits, 0 to 360 degrees  

**FIR Filter:** 18-bit coefficients, 24-bit output, with user programmable coefficients  
**Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation  

**Multiboard Summation Expansion Chain**  
*Summation Expansion Chain:* Multiple boards can be summed via two stages of 2x to 256x  
*Gain Coefficients:* 16-bit resolution  
*Phase Shift Coefficients:* 1 and Q with 16-bit resolution  
*Gain Coefficients:* 16-bit resolution  
*Channel Summation:* 24-bit  
*Multiboard Summation Expansion:* 32-bit  

**External Clocks (1 or 2)**  
*Type:* Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference  

**Timing Bus (1 or 2):** 26-pin connector  
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs  

**Field Programmable Gate Arrays (1 or 2)**  
*Standard:* Xilinx Virtex-6 XC6VLX240T  
*Optional:* Xilinx Virtex-6 XC6VSX315T

**Custom I/O**  
*Option -104:* Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57621; P3 and P5, Model 58621  

**Memory Banks (1 or 2)**  
*Option 150 or 165:* Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR  
*Option 155 or 165:* Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**  
*PCI Express Bus:* Gen. 1 or 2: x4 or x8  
*Environmental:* Level L1 & L2 air-cooled;  
Level L3 ruggedized, conduction-cooled  
*Size:* 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57800 and 58800 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a VPX carrier board. Model 57800 is a 6U board with one Model 71800 module while the Model 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57800 and Model 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.
Kintex UltraScale FPGA Coprocessor - 6U VPX

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Specifications

Front Panel Digital I/O Interface
These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Options:
- -084 XCKU060-2 FPGA
- -087 XCKU115-2 FPGA
- -104 LVDS FPGA I/O
- -105 Gigabit serial FPGA I/O
- -702 Air cooled, Level L2
- -713 Conduction cooled, Level L3

Memory (1 or 2)
- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: −20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: −40° to 70° C
  - Storage Temp: −50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size:
- 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Ordering Information

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<td>Kintex UltraScale FPGA Coprocessor - 6U VPX</td>
<td>-084 XCKU060-2 FPGA, -087 XCKU115-2 FPGA, -104 LVDS FPGA I/O, -105 Gigabit serial FPGA I/O, -702 Air cooled, Level L2, -713 Conduction cooled, Level L3</td>
</tr>
<tr>
<td>58800</td>
<td>Double Kintex UltraScale FPGA Coprocessors - 6U VPX</td>
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Contact Pentek for complete specifications of rugged and conduction-cooled versions.
**General Information**

Models 57624 and 58624 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71624 XMC modules mounted on a VPX carrier board. Model 57624 is a 6U board with one Model 71624 module while the Model 58624 is a 6U board with two XMC modules rather than one.

As IF relays, they accept two or four IF analog input channels, modify up to 34 or 68 signals, and then deliver them to two or four analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

These models support many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board’s data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

A PCIe Gen. 1 system interface supports control, status and data transfers.

### Features
- Modifies 34 or 68 IF signals between input and output
- Up to 80 MHz IF bandwidth
- Two/four 200 MHz 16-bit A/Ds
- Two/four 800 MHz 16-bit D/A
- 34/68 DDCs and 34/68 DUCs (digital downconverters and digital upconverters)
- Signal drop/add/replace
- Frequency shifting and hopping
- Amplitude boost and attenuation
- PCI Express Gen. 1: x4 or x8

### Adaptive Relay Input Overview

These models digitize two or four analog IF inputs using 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 or 68 DDCs (digital downconverters) can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of two A/Ds.

Baseband I+Q DDC outputs are scaled in a programmable gain/attenuation block before being delivered across the PCIe system interface to target memory, typically associated with a system processor. Here, the signals can be analyzed, classified, demodulated, decrypted or decoded, depending on the application.

Samples from each A/D converter can also be delivered across PCIe to system memory so that the processor can access wideband IF data. By performing an FFT, the processor can identify signals and then tune the DDCs accordingly.

### Adaptive Relay Output Overview

The output stage of these models consists of two or four 800 MHz 16-bit D/A converters. Each DUC accepts baseband I+Q.
➤ signals from either the local DDCs or from system memory.

DUC inputs are scaled in programmable gain/attenuation blocks similar to those in the input stages. Each DUC is independently programmable for data source selection (DDC or memory), upconvert tuning frequency and bandwidth (interpolation).

The translated DUC outputs are directed to either of two or four summation blocks, each associated with one of the two or four D/A converters using a final interpolation factor of x4. After conversion, the IF analog outputs of each D/A can contain signals from any combination of the 34 or 68 DUCs.

**Xilinx Virtex-6 FPGA**

The SX315T Virtex-6 FPGA with 1344 DSP48E engines is well suited for the demanding signal processing tasks required by the adaptive relay of these models. Because of the complexity and proprietary nature of these functions, the FPGAs cannot be extended or modified by the user.

**A/D Converters**

The front-end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into one or two Virtex-6 FPGAs for the data capture and all of the remaining adaptive relay signal processing operations.

**Digital Downconverters**

Each of the FPGA-based DDCs has an independent mixer and local oscillator with a 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency, nominally 200 MHz. An IF input signal can be downconverted to a complex (I+Q) signal centered at 0 Hz by setting the DDC tuning frequency to its center frequency.

The DDC output bandwidth is determined by its decimation setting, which is programmable from 512 to 8192 in steps of 8. Each DDC can have a different decimation, thereby supporting up to 34 or 68 different signal bandwidths.

The fixed 80% decimating output filters deliver an output bandwidth equal to \( 0.8 f_s / N \), where \( N \) is the decimation setting and \( f_s \) is the A/D sample rate. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

**Input Gain Blocks**

Each DDC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated. Each input gain block, which is a complex digital multiplier, accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB.

**Receive DMA Controllers**

Two or four output DMA engines deliver data across the PCIe interface into user-specified memory locations in PCIe target memory. DMA engine #1 can deliver either raw samples from A/D Ch 1 or channel-interleaved 24-bit I and Q baseband samples from the 34 DDCs of the first XMC module. Data samples from each DDC can be independently enabled/disabled for output. DMA engine #2 can deliver raw samples from A/D Ch 2. This sequence repeats for the second XMC module of Model 58624.

When a target memory buffer is filled, these models issue an interrupt to the system processor and then begin filling an alternate buffer. In this way, the processor is always informed when and where data is available for retrieval. Packet headers identify the DDC and show the number of subsequent data samples.

**Transmit DMA Controllers**

Each of the FPGA-based 34 or 68 DUCs interpolates complex (I+Q) baseband signals and translates them to the desired IF output center frequency.

The data source for each DUC can be independently selected from its corresponding DDC output, or from PCIe target memory buffers fetched by the transmit DMA controller, where header information steers the memory data to the appropriate DUC channel.

Like the receive DMA controllers, once a data buffer is emptied, these models signal the processor with an interrupt and move to the next assigned buffer to continue fetching data.

**Output Gain Blocks**

The complex baseband input for each DUC complex output is delivered through a complex gain stage where the baseband signal can be amplified or attenuated.

Each of the output gain blocks accepts a unique 16-bit binary gain coefficient in Q8.8 format (8 bits integer + 8 bits fractional). This results in gain values ranging from approximately +48 dB to –48 dB. ➤
**Digital Upconverters**

The interpolation filter increases the baseband input sample rate by an interpolation factor typically equal to the decimation factor of the corresponding DDC. This interpolation factor is programmable from 512 to 8192 in steps of 8. Using this strategy, the interpolation sample rate equals the A/D sample rate, nominally 200 MHz.

A complex digital mixer upconverts the interpolated baseband signal to the desired IF output center frequency. This frequency is determined by a local oscillator programmable with a 32-bit integer from DC to $f_i$, where $f_i$ is the interpolator output frequency, nominally 200 MHz.

Each of the DUCs can have an independent interpolation factor and tuning frequency. However, all DUC outputs sharing a common summation block must have the same sample rate.

**Summation Blocks**

Two or four summation blocks accept any combination of the upconverted DUC signals by setting an enable bit for each DUC’s contribution. Each DUC output can be enabled for none, one or both of the summation blocks.

The summation blocks deliver only real output samples to the subsequent D/A converter stage.

**D/A Converters**

A TI DAC5688 dual-channel D/A accepts the summed upconverted data streams, one from each summation block, and operates in its non-translating dual, real baseband mode. Its built-in interpolation filter is typically set to x4 mode, boosting the summation output sample rate from a nominal 200 MHz to 800 MHz. This simplifies the output low pass reconstruction filtering requirements.

Two or four transformer-coupled analog IF outputs are delivered through one or two pairs of front panel SSMC connectors.

**Clocking and Synchronization**

Two or four internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks.

In an alternate mode, the sample clock can be sourced from one or two on-board programmable VCXOs (voltage-controlled crystal oscillators). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the internal oscillator.

One or two front panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCIe Gen. 1 x8 bus specifications. The interface automatically adjusts to accommodate fewer lanes, and includes dual DMA controllers for efficient transfers to and from the board.

**Form Factor Adaptors**

All Pentek Cobalt XMC modules can be adapted to other standard embedded system form factors through the use of adaptor boards. Available versions include PCIe, 3U and 6U OpenVPX, 3U and 6U cPCI, and AMC. For more information and the Pentek’s Product Selector Tool visit our website at: www.pentek.com.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Model 57624: 2 A/Ds, 34 DDCs, 34 DUCs, 2 D/As
Model 58624: 4 A/Ds, 68 DDCs, 68 DUCs, 4 D/As

Front Panel Analog Signal Inputs (2 or 4)

- Transformer-coupled, front panel female SSMC connectors
- PLL System Reference: Xilinx Virtex-6 XC6VSX315T (required)

A/D Converters

- Quantity: 2 or 4
- Type: Texas Instruments ADS5485
- Resolution: 16 bits

Digital Downconverters

- Quantity: 34 or 68
- Decimation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >100 dB
- Phase Offset: 1 bit, 0 or 180 degrees
- FIR Filter: 18-bit coefficients
- Output: Complex, 16-bit I + 16-bit Q
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Input Gain Blocks

- Quantity: 34 or 68
- Data: Complex, 16-bit I + 16-bit Q
- Gain: 16-bit Q8.8 format, approximately +/−48 dB

Output Gain Blocks

- Quantity: 34 or 68
- Data: Complex, 16-bit I + 16-bit Q
- Gain: 16-bit Q8.8 format, approximately +/−48 dB

Digital Upconverters

- Quantity: 34 or 68
- Interpolation Range: 512 to 8192, in steps of 8
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- FIR Filter: 18-bit coefficients, 16-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

D/A Converters

- Analog Output Channels: 2 or 4
- Type: Texas Instruments DAC5688
- Input Data Rate: 200 MHz max.
- Output Signal: Real
- Output Sampling Rate: 80 MHz max. with 4x interpolation
- Resolution: 16 bits

Front Panel Analog Signal Outputs (2 or 4)

- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: (1 or 2)

- On-board clock synthesizers generate two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

- Type: Front panel female SSMC connectors, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accept 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Arrays (1 or 2)

- Required: Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface

- PCI Express Bus: Gen. 1: x4 or x8;

Environmental

- Standard:
  - Operating Temp: 0° to 50° C
  - Storage Temp: −20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.

- Option 702 L2 Extended Temp (air-cooled):
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-cond.

- Option 712 L2 Extended Temp (conduction-cooled):
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-cond.

- Size: Standard 6U VPX board, 233 x 160 mm (9.173 x 6.299 in.)

Ordering Information

Model | Description | Options
--- | --- | ---
57624 | Dual-Channel 34-Signal Adaptive IF Relay - 6U VPX | -064: XC6VSX315T (required)
58624 | Quad-Channel 68-Signal Adaptive IF Relay - 6U VPX | -070: L2 (air cooled), environmental level
 | | -712: L2 (conduction cooled), environmental level
 | -730: 2-slot heatsink

Contact Pentek for availability of rugged and conduction-cooled versions.

Model | Description | Options
--- | --- | ---
8264 | VPX Development System. See 8264 Datasheet for Options

Pentek, Inc. | One Park Way • Upper Saddle River • New Jersey 07458 | Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com | www.pentek.com
**General Information**

Models 57630 and 58630 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a VPX carrier board.

Model 57630 is a 6U board with one Model 71630 module while the Model 58630 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630.

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**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggerized and conduction-cooled versions available

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**Block Diagram, Model 57630**

Model 58630 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5.
**A/D Acquisition IP Module**

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Modules**

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

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**A/D Converter Stage**

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSps, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

**Memory Resources**

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>57630</td>
<td>1 GHz A/D and D/A with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58630</td>
<td>Two 1 GHz A/D and D/A, with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57630; P3 and P5 connectors, Model 58630
- **-105** Gigabit link between the FPGA and P2 connector, Model 57630; gigabit links from each FPGA to P2 connector, Model 78630
- **-160** Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8264

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen.1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57630: 1 A/D, 1 D/A
Model 58630: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

- **Type:** Texas Instruments ADS5400
  - **Sampling Rate:** 100 MHz to 1 GHz
  - **Resolution:** 12 bits

D/A Converters (1 or 2)

- **Type:** Texas Instruments DAC5681Z
  - **Input Data Rate:** 1 GHz max.
  - **Interpolation Filter:** bypass, 2x or 4x
  - **Output Sampling Rate:** 1 GHz max.
  - **Resolution:** 16 bits

Front Panel Analog Signal Outputs (1 or 2)

- **Output Type:** Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)

- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
  - **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus (1 or 2)

- **Type:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)

- **Type:** Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
  - **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630

Memory Banks (1 or 2)

- **Option 150:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

Environmental

- **Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled**
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8264

Development Systems
General Information

Models 57640 and 58640 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a VPX carrier board.

Model 57640 is a 6U board with one Model 71640 module while the Model 58640 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57640; P3 and P5, Model 58640.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57640; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58640.
1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX

➤ A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s data and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX

Model 57640: One A/D
Model 58640: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)
Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources (1 or 2)
Front panel SSMC connector

Sync Bus (1 or 2)
Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -002: -2 FPGA speed grade
-062: XC6VLX240T
-064: XC6VSX315T

-104: LVDS I/O between the FPGA and P3 connector, Model 57640; P3 and P5 connectors, Model 58640
-105: Gigabit link between the FPGA and P2 connector, Model 57640; gigabit links from each FPGA to P2, Model 78640

-155: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Options:

Model 8264
VPX Development System.
See 8264 Datasheet for Options

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57640</td>
<td>1-Ch. 3.6 GHz or 2-Ch.</td>
</tr>
<tr>
<td></td>
<td>1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58640</td>
<td>2-Ch. 3.6 GHz or 4-Ch.</td>
</tr>
<tr>
<td></td>
<td>1.8 GHz, 12-bit A/D with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Memory Banks (1 or 2)
Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57641 and 58641 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71641 XMC modules mounted on a VPX carrier board.

Model 57641 is a 6U board with one Model 71641 module while the Model 58641 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, one- or two-channel programmable digital downconverters, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71641 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Features

- Ideal radar and software radio interface solution
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 2 or 4 GB of DDR3 SDRAM
- PCIe Express (Gen. 1 & 2) interface up to x8
- µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX Models 57641 & 58641
**1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX**

### A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

### Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

### Memory Resources

The Cobalt architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

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**VRTEX-6 FPGA DATAFLOW DETAIL**

*Two channel mode shown. Programmable decimation of 8, 16 or 32 available in one channel mode.*
1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-6 FPGA - 6U OpenVPX

**Models 57641 & 58641**

**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
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<tbody>
<tr>
<td>57641</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58641</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
- **-105** Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

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**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Model 57641: One A/D**

**Model 58641: Two A/Ds**

**Front Panel Analog Signal Inputs (2 or 4)**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converters (1 or 2)**

- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:** Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

**Digital Downconverters (2 or 4)**

- **Modes:** One or two channels, programmable
- **Supported Sample Rate:** One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- **Decimation Range:** One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** User-programmable 18-bit coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**Sample Clock Sources (1 or 2)**

- **Front panel SSMC connector**

**Sync Bus (1 or 2)**

- **Multi-pin connectors, bus includes gate, reset and in and out ref clock**

**External Trigger Input (1 or 2)**

- **Type:** Front panel female SSMC connector, TTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

- **Xilinx Virtex-6 XC6VSX315T-2**

**Custom I/O**

- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57641; P3 and P5, Model 58641
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57641; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58641

**Memory Banks (1 or 2)**

- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1 or 2: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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<tr>
<td>58641</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX</td>
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</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
- **-105** Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Model 8264**

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<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX</td>
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**Options:**

- **-002** -2 FPGA speed grade
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
- **-105** Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

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<td>58641</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57641; P3 and P5 connectors, Model 58641
- **-105** Gigabit link between the FPGA and P2 connector, Model 57641; gigabit links from each FPGA to P2 connector, Model 78641
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

2- or 4-Channel 500 MHz A/D, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA - 6U OpenVPX

General Information
Models 57650 and 58650 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71650 XMC modules mounted on a VPX carrier board.

Model 57650 is a 6U board with one Model 71650 module while the Model 58650 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, one or two DUCs, two or four D/A and four or eight banks of memory.

The Cobalt Architecture
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57650; P3 and P5, Model 58650.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57650; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58650.

Features
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Two or four 500 MHz 12-bit A/Ds
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or 32 MB or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

These models include one or two factory-installed sophisticated D/A Waveform Playback IP modules. Linked-list controllers allow users to easily play back waveforms stored in either on-board memory or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stages

The front end accepts two or four full scale analog HF or IF inputs on front panel SSMC connectors at +5 dBm into 50 ohms with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs and D/A accept baseband real or complex data streams from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tbody>
<tr>
<td>57650</td>
<td>Two 500 MHz A/Ds, One DUC, Two 800 MHz D/As with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58650</td>
<td>Four 500 MHz A/Ds, Two DUCs, Four 800 MHz D/As with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:
- 002* -2 FPGA speed grade
- 014 400 MHz, 14-bit A/Ds
- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 104 LVDS I/O between the FPGA and P3 connector, Model 57650; P3 and P5 connectors, Model 58650
- 105 Gigabit link between the FPGA and P2 connector, Model 57650; gigabit links from each FPGA to P2 connector, Model 78650
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications

- board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include A/D data transient capture mode and D/A waveform playback mode.

- In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

- PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

- Clock Synthesizers (1 or 2)
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

- External Clocks (1 or 2)
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
  - Timing Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

- External Trigger Inputs (1 or 2)
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX130T-2
- Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- Option -014: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57650; P3 and P5, Model 58650
- Option -015: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57650; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58650

Memory Banks (1 or 2)

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1 or 2: x4 or x8
- Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57651 and 58651 are members of the Cobalt family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a VPX carrier board.

Model 57651 is a 6U board with one Model 71651 module while the Model 58651 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As, one or two beamformers and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beam-forming IP cores, an Aurora and a PCIe interfaces complete the factory-installed functions and enable these models to operate without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57651; P3 and P5, Model 58651.
**A/D Acquisition IP Modules**

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s \)/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s \)/N.

**Beamformer IP Cores**

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is program-manageable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple models can be chained together via a built-in Xilinx Aurora gigabit serial interface through the dual 4X serial connector. This allows summation across channels on multiple boards.

**D/A Waveform Playback IP Modules**

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/A wavesforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.
A/D Converter Stages
The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two or four Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other module resources.

Digital Upconverter and D/A Stages
One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The Cobalt architecture supports up to three or six independent memory banks which can be configured with QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
These models include an industry-standard interface fully compliant with PCI Express Gen.1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Specifications**

Model 57651: 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As
Model 58651: 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As

**Front Panel Analog Signal Inputs (2 or 4)**
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +5 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

**A/D Converters (standard) (2 or 4)**
- Type: Texas Instruments ADS5463
- Sampling Rate: 20 MHz to 500 MHz
- Resolution: 12 bits

**A/D Converters (Option -014) (2 or 4)**
- Type: Texas Instruments ADS5474
- Sampling Rate: 20 MHz to 400 MHz
- Resolution: 14 bits

**Digital Downconverters (2 or 4)**
- Decimation Range: 2x to 131,072x
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters (2 or 4)**
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or one-channel with frequency translation
- Output Sampling Range: 800 MHz max.
- with 2x, 4x or 8x interpolation
- Resolution: 16 bits

**Digital Interpolators (1 or 2)**
- Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

**Beamformers (1 or 2)**
- Summation: Two channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via a dual 4X connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Channel Summation: 24-bit
- Multiboard Summation Expansion: 32-bit

**Front Panel Analog Signal Outputs (2 or 4)**
- Output: Transformer-coupled, front panel female SSMC connectors
- Transformer: Coil Craft WBC4-6TLB
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

**Sample Clock Sources (2 or 4)**
- On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
- Clock Synthesizers (1 or 2)
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clocks (1 or 2)**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus (1 or 2)**
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Arrays (1 or 2)**
- Standard: Xilinx Virtex-6 XC6VLX240T-2
- Optional: Xilinx Virtex-6 XC6VSX315T-2

**Custom I/O**
- Option -014: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57651; P3 and P5, Model 58651

**Memory (1 or 2)**
- Option -150 or -160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option -155 or -165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- PCI Express Bus: Gen. 1 or 2: x4 or x8

**Environmental**
- Level L1 & L2 air-cooled;
- Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57660 and 58660 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a VPX carrier board.

Model 57660 is a 6U board with one Model 71660 module while the Model 58660 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDR II+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
FPGA

A/D Acquisition IP Modules

The exact length of that gate is not known prior to data acquisition; rather, it is governed by the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stages

The front end accepts four or eight full-scale analog HF or LF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments AD85485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
## Models 57660 & 58660

### 4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U OpenVPX

#### Specifications
- **Model 57660**: 4 A/Ds
- **Model 58660**: 8 A/Ds
- **Front Panel Analog Signal Inputs (4 or 8)**
  - **Input Type**: Transformer-coupled, front panel female SSMS connectors
  - **Transformer Type**: Coil Craft WBC4-6TLB
  - **Full Scale Input**: +8 dBm into 50 ohms
  - **3 dB Passband**: 300 kHz to 700 MHz
- **A/D Converters (4 or 8)**
  - **Type**: Texas Instruments ADS5485
  - **Sampling Rate**: 10 MHz to 200 MHz
  - **Resolution**: 16 bits
- **Sample Clock Sources (1 or 2)**
  - On-board clock synthesizers
- **Clock Synthesizers (1 or 2)**
  - **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
- **External Clocks (1 or 2)**
  - **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

### Ordering Information

#### Model Description
- **Model 57660**: 4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U VPX
- **Model 58660**: 8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U VPX

#### Options:
- **-062**: XC6VLX240T FPGA
- **-064**: XC6VSX315T FPGA
- **-104**: LVDS I/O between the FPGA and P3 connector, Model 57660; P3 and P5 connectors, Model 58660
- **-105**: Gigabit link between the FPGA and P2 connector, Model 57660; gigabit links from each FPGA to P2 connector, Model 58660
- **-150**: Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- **-160**: Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- **-155**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165**: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

### Custom I/O
- **Option -104**: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660
- **Option -105**: Supports serial protocols by providing a 4x gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660

#### Memory Banks (1 or 2)
- **Option 150 or 160**: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165**: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

### PCI-Express Interface
- **PCI Express Bus**: Gen. 1 or 2: x4 or x8
- **Environmental**: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

### Contact Pentek for availability of rugged and conduction-cooled versions

**Model 8264**
- **Description**: VPX Development System. See 8264 Datasheet for Options
General Information

Models 57661 and 58661 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71661 XMC modules mounted on a VPX carrier board.

Model 57661 is a 6U board with one Model 71661 module while the Model 58661 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, four or eight multiband DDCs, one or two programmable beamformers, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. PentekGateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57661; P3 and P5, Model 58661.

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**Features**

- Supports Xilinx Virtex-6 LXT and SX7 FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs (digital downconverters)
- One or two multiboard programmable beamformers
- Up to 2 or 4 GB of DDR3 SDRAM; or; 32 MB or 64 MB of QDRII+ SRAM
- PCIe Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

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**Models 57661 & 58661**

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U OpenVPX
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold. A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple 71661’s can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 PCIe connector. This allows summation across channels on multiple boards.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage.
4- or 8-Channel 200 MHz A/D with DDCs and Virtex-6 FPGA - 6U OpenVPX

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Options:

- 064 XC6VSX315T
- 104 LVDS I/O between the FPGA and P3 connector, Model 57661; P3 and P5 connectors, Model 58661
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 57661: 4 A/Ds
Model 58660: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)

- Input Type: Transformer-coupled, front panel female SSMB connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Digital Downconverters (4 or 8)

- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)

- Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
- Summation Expansion Chain: One chain in and one chain out link via VPX P2 connector using Aurora protocol
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution
- Multiboard Summation Expansion: 32-bit

Sample Clock Sources (1 or 2)

- On-board clock synthesizer

Clock Synthesizers (1 or 2)

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)

- Type: Front panel female SSMB connector
- Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Timing Bus (1 or 2): 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)

- Type: Front panel female SSMB connector
- LVTTL

Field Programmable Gate Arrays (1 or 2)

- Standard: Xilinx Virtex-6 XC6VLX240T
- Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O

- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57661; P3 and P5, Model 58661

Memory Banks (1 or 2)

- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCI Express Bus: Gen. 1 or 2: x4 or x8
- Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57662 and 58662 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71662 XMC modules mounted on a VPX carrier board.

Model 57662 is a 6U board with one Model 71662 module while the Model 58662 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, 32 or 64 multiband DDCs and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, and triggering. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for control of all data clocking, synchronization, gate and trigger functions, test signal generators, voltage and temperature monitoring, DDR3 SDRAM memory controllers, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662.

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- 32 or 64 channels of multiband DDCs (digital downconverters)
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

 Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

is programmable in steps of 8 from 16 to 1024 and steps of 64 from 1024 to 8192. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of $f_s / N$. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with DDR3 SDRAM.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model 57662: 4 A/Ds, 32 DDCs
Model 58660: 8 A/Ds, 64 DDCs
Front Panel Analog Signal Inputs (4 or 8)
  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: 28AWG, 0.100" female SSMC connector, 50 ohms, accepts 10 to +10 dBm
  Full Scale Input: 150 mV
  Resolution: 12 bits

Digital Downconverters (32 or 64)
  Quantity: Four 8-channel banks, one per acquisition module
  Decimation Range: 16 to 1024 in steps of 8 and 1024 to 8192 in steps of 64
  LO Tuning Freq.: Resolution: 32 bits, 0 to f<sub>L0</sub>
  Phase Offset Resolution: 32 bits, 0 to 360 degrees
  FIR Filter: 18-bit coefficients, 24-bit output, with up to 100 dB stopband attenuation

Sample Clock Sources (1 or 2)
  On-board clock synthesizer

Clock Synthesizers (1 or 2)
  Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL
  Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
  Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm
  AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock, or PLL system reference

Timing Bus (1 or 2): 26-pin connector, clock/sync/gate/PPS inputs and outputs

External Trigger Inputs (1 or 2)
  Type: Front panel female SSMC connector
  Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
  Standard: Xilinx Virtex-6 XC6VLX240T
  Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
  Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57662; P3 and P5, Model 58662
  Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPPX P2, Model 57662; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58662

Memory Banks (1 or 2)
  Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
  PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled;

Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57663 and 58663 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a VPX carrier board.

Model 57663 is a 6U board with one Model 71663 module while the Model 58663 is a 6U board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Features

- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- PCIe Express (Gen. 1 & 2) interface up to x4
- LVPECL clock/sync bus for multiboard synchronization
- Ruggedized and conduction-cooled versions available
GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, carefult filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once completed, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The PCIe interface is also used as the programming interface for all status and control between these models and host.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Model 57663: 4 A/Ds, 1100 Channels
Model 58663: 8 A/Ds, 2200 Channels

Front Panel Analog Signal Inputs (4 or 8)

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)

On-board clock synthesizer
Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks (1 or 2)

DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels

Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 kHz
> 96 dB attenuation at > ±3 MHz

DDC Output Rate $f_s$: Resampled to 180 MHz x 13 / 2160 = 1.0833333 MS/sec

DDC Data Output Format:
24 bits I + 24 bits Q

Superchannels

Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
Frequency Offsets for each DDC:
First: $-f_s / 4$ (-270.8333 kHz)
Second: 0 Hz
Third: $+f_s / 4$ (+270.8333 kHz)
Fourth: $+f_s / 2$ (+541.666 kHz)

Superchannel Sample Rate: $f_s$

Superchannel Output Format:
26 bits I + 26 bits Q

Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Arrays (1 or 2)

Xilinx Virtex-6 XC6VSX315T

PCI-Express Interface

PCI Express Bus: Gen. 1 or 2: x4

Environmental: Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

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<tr>
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<th>Description</th>
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<td>1100-Channel GSM Channelizer with Quad A/D - 6U VPX</td>
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<tr>
<td>58663</td>
<td>2200-Channel GSM Channelizer with Octal A/D - 6U VPX</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>8264</td>
<td>VPX Development System. See 8264 Datasheet for Options</td>
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</tbody>
</table>
General Information

Models 57664 and 58664 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71664 XMC modules mounted on a VPX carrier board.

Model 57664 is a 6U board with one Model 71664 module while the Model 58664 is a 6U board with two XMC modules rather than one. Their PCIe output supports fully the VITA 49.0 Radio Transport (VRT) Standard.

These models include four or eight A/Ds, four or eight multiband DDCs, one or two programmable beamformers, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, programmable beamforming IP cores, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SX part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57664; P3 and P5, Model 58664. ▶
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drive acquires and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Beamformer IP Cores

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector. This allows summation across channels on multiple boards.

VITA 49.0

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software Defined Radio (SDR) systems. Specifically each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver.

These models support fully the VITA 49.0 specification.

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**Pentek, Inc.**
One Park Way  ●  Upper Saddle River  ●  New Jersey 07458
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com

www.pentek.com
A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture and for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Models 57664 & 58664

4- or 8-Channel 200 MHz A/D with DDCs, VITA 49.0, Virtex-6 FPGA - 6U VPX

Specifications
Model 57664: 4 A/Ds
Model 58664: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Digital Downconverters (4 or 8)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, with user programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Beamformers (1 or 2)
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via VPX P2 connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit Multiboard Summation Expansion: 32-bit
Sample Clock Sources (1 or 2)
On-board clock synthesizer

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T
Optional: Xilinx Virtex-6 XC6VSX315T

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57664; P3 and P5, Model 58664

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental
Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information
Model Description
57664 4-Channel 200 MHz A/D with DDCs, VITA 49.0, one Virtex-6 FPGA - 6U VPX
58664 8-Channel 200 MHz A/D with DDCs, VITA 49.0, two Virtex-6 FPGAs - 6U VPX

Options:
- 064 XC6VSX315T
- 104 LVDS I/O between the FPGA and P3 connector, Model 57664; P3 and P5 connectors, Model 58664
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8264 VPX Development System. See 8264 Datasheet for Options
4- or 8-Channel 1.25 GHz D/A with DUC and Virtex-6 FPGA - 6U OpenVPX

General Information

Models 57670 and 58670 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a VPX carrier board.

Model 57670 is a 6U board with one Model 71670 module while the Model 58670 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As, four or eight DUCs, and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57670; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58670.

Features

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/ sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  www.pentek.com
FPGA DATAFLOW

Module D/A Waveform Playback IP

- A minimum of programming.
- Create complex waveforms with a minimum of programming.
- Can be chained together to create complex waveforms with a minimum of programming.

- The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 58670.
- Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.
- Up to 64 or 128 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four or eight front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

———
4- or 8-Channel 1.25 GHz D/A with DUC and Virtex-6 FPGA - 6U OpenVPX

**Specifications**

**Model 57670: 4-Channel DUC, 4-channel D/A**
- **Input Data Rate**: 312.5 MHz max.
- **Output Bandwidth**: 250 MHz max.
- **Output Sampling Rate**: 1.25 GHz max. with interpolation
- **Interpolation**: 2x, 4x, 8x or 16x
- **Resolution**: 16 bits

**Model 58670: 8-Channel DUC, 8-channel D/A**
- **Input Data Rate**: 312.5 MHz max.
- **Output Bandwidth**: 250 MHz max.
- **Output Sampling Rate**: 1.25 GHz max. with interpolation
- **Interpolation**: 2x, 4x, 8x or 16x
- **Resolution**: 16 bits

**D/A Converters (4 or 8)**

- **Type**: TI DAC3484
- **Output Sampling Rate**: 1.25 GHz max. with interpolation
- **Interpolation**: 2x, 4x, 8x or 16x
- **Resolution**: 16 bits

**Front Panel Analog Signal Outputs (4 or 8)**

- **Type**: Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output**: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming**: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

**Clock Synthesizers (1 or 2)**

- **Clock Source**: Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clocks (1 or 2)**

- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Inputs (1 or 2)**

- **Type**: Front panel female SSMC connector
- **Function**: Programmable functions include: trigger, gate, sync and PPS

**Timing Bus (1 or 2)**: 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

**Field Programmable Gate Arrays (1 or 2)**

- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

- **Option -104**: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670
- **Option -105**: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57670; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58670

**Memory Banks (1 or 2)**

- Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus**: Gen. 1 or 2: x4 or x8

**Environmental**

- **Level L1 & L2 air-cooled**: Level 3 ruggedized, conduction-cooled
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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**Ordering Information**

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>57670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58670</td>
<td>8-Channel 1.25 GHz D/A with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57670; P3 and P5 connectors, Model 58670
- **-105** Gigabit link between the FPGA and P2 connector, Model 57670; gigabit links from each FPGA to P2 connector, Model 58670
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

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Contact Pentek for availability of rugged and conduction-cooled versions

**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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Pentek, Inc. One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

**General Information**

Models 57671 and 58671 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71671 XMC modules mounted on a VPX carrier board.

Model 57671 is a 6U board with one Model 71671 module while the Model 58671 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As with a wide range of programmable interpolation factors, four or eight DUCs, and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671.

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**Features**

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Extended interpolation range from 2x to 1,048,576x
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCIe Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad μSync clock/ sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

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**Block Diagram, Model 57671.**

Model 57671 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5.
D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. Four or eight linked-list controllers support waveform generation to the four or eight D/A s from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4, as well as to the other four channels of Model 58671.

Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 or 128 individual link entries for each D/A can be chained together to create complex waveforms with a minimum of programming.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board's sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board's DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
4- or 8-Channel 1.25 GHz D/A with DUC, Extended Interpolation and Virtex-6 FPGA - 6U OpenVPX

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57671: 4-Channel DUC, 4-channel D/A
Model 58671: 8-Channel DUC, 8-channel D/A

D/A Converters (4 or 8)
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x

Front Panel Analog Signal Outputs (4 or 8)
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from −20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX240T-2
Optional: Xilinx Virtex-6 XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57671; P3 and P5, Model 58671
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57671; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58671

Memory Banks (1 or 2)
Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
New! New! New! New! New!

Ruggedized and conduction-cooled versions available

Optional LVDS connections
Optional user-configurable PCIe interface
PCI Express (Gen. 1 & 2)
Up to 2 or 4 GB of DDR3
Supports Xilinx Virtex-6 LXT
Two or four 200 MHz 16-bit A/Ds
One or two programmable L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SX315T part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690.

General Information

Models 57690 and 58690 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a VPX carrier board.

Model 57690 is a 6U board with one Model 71690 module while the Model 58690 is a 6U board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

Features

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or, 32 MB or 64 MB of QDRII+ SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
## RF Tuner Stages

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LN Bs (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters. The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNAs offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

## A/D Converter Stages

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

## A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

## Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

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### A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

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### A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

## Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<td>57690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX</td>
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<tr>
<td>58690</td>
<td>Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX</td>
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Options:

- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 104 LVDS I/O between the FPGA and P3 connector, Model 57690; P3 and P5 connectors, Model 58690
- 105 Gigabit link between the FPGA and P2 connector, Model 57690; gigabit links from each FPGA to P2 connector, Model 58690
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Model 57690: One RF tuner, two A/Ds
Model 58690: Two RF tuners, four A/Ds

Front Panel Analog Signal Inputs (1 or 2)
- Connector: Front panel female SSMC
- Impedance: 50 ohms

L-Band Tuners (1 or 2)
- Type: Maxim MAX2112
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer:
  - freqVCO = (N.F) x freqREF where integer N = 19 to 251 and fractional F is a 20-bit binary value
- PLL Reference (freqREF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz, typical 10 MHz
- LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter
- Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps
  - *Usable Full-Range Input: 0 to +10 dBm
  - Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

Sample Clock Sources (1 or 2)
- On-board timing generator/synthesizer
- A/D Clock Synthesizers (1 or 2)
  - Clock Source: Selectable from on-board programmable LMCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: LMCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or LMCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Inputs (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

External Trigger Inputs (2 or 4)
- Type: Front panel female SSMC connector, LV TTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690

Memory Banks (1 or 2)
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1 or 2: x4 or x8
- Environmental: Level L1 & L2 air-cooled;
- Level L3 ruggedized, conduction-cooled

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
General Information

Models 57720 and 58720 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71720 XMC modules mounted on a VPX carrier board. Model 57720 is a 6U board with one Model 71720 module while the Model 58720 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, one or two D/As, two or four D/As and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include three or six A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 58720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts three or six full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Digital Upconverter and D/A Stages

One or two TI DAC5688 DUCs (digital upconverters) and D/As accept baseband real or complex data streams from the FPGA and provide that input to the upconvert, interpolate and dual D/A stages.
Memory Resources
The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, including FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>57720</td>
<td>3-Channel 200 MHz A/D and 2-Channel 800 MHz D/A with Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58720</td>
<td>6-Channel 200 MHz A/D and 4-Channel 800 MHz D/A with two Virtex-7 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:
- -076  XC7VX690T-2 FPGA
- -104  LVDS I/O between the FPGA and P3 connector, Model 57720; P3 and P5 connectors, Model 58720
- -105  Gigabit link between the FPGA and P2 connector, Model 57720; gigabit links from each FPGA to P2 connector, Model 78720

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications
Model 57620: 3 A/Ds, 1 DUC, 2 DAs
Model 58620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

D/A Converters (2 or 4)
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with interpolation
- Resolution: 16 bits

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

PCI Express Interface
These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

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</tr>
</tbody>
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Options:
- -076  XC7VX690T-2 FPGA
- -104  LVDS I/O between the FPGA and P3 connector, Model 57720; P3 and P5 connectors, Model 58720
- -105  Gigabit link between the FPGA and P2 connector, Model 57720; gigabit links from each FPGA to P2 connector, Model 78720

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications
Model 57620: 3 A/Ds, 1 DUC, 2 DAs
Model 58620: 6 A/Ds, 2 DUCs, 4 D/As

Front Panel Analog Signal Inputs (3 or 6)
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (3 or 6)
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

D/A Converters (2 or 4)
- Type: Texas Instruments DAC5688
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz max.
- Output Signal: 2-channel real or 1-channel with frequency translation
- Output Sampling Rate: 800 MHz max. with interpolation
- Resolution: 16 bits

Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or PLL system reference

Timing Bus (1 or 2): 26-pin connector
- LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57720; P3 and P5, Model 58720
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57720; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58720.

Memory Banks (4 or 8)
- Type: DDR3 SDRAM
- Size: 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Environmental: Level L1 & L2 air-cooled;
- Level L3 ruggedized, conduction-cooled
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
3- or 6-Channel 200 MHz A/D with DDC, DUC with 2- or 4-Channel 800 MHz D/A, Virtex-7 FPGAs - 6U OpenVPX

**General Information**

Models 57721 and 58721 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71721 XMC modules mounted on a VPX carrier board.

Model 58721 is a 6U board with one Model 71721 module while the Model 58721 is a 6U board with two XMC modules rather than one.

These models include three or six A/Ds, programmable DDCs, one or two DUCs, two or four D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful programmable DDC IP core. The waveform playback IP module contains one or two interpolation IP cores, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX-P3 connector, Model 57721; P3 and P5, Model 58721.

**Features**

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs
- One or two DUCs
- Two or four 800 MHz 16-bit D/As
- Multiboard programmable beamformer
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

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**Block Diagram, Model 57721.** Model 58721 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

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**Contact Information**

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications. The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the $80\%$ output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Beamformer IP Cores

In addition to the DDCs, these models feature one or two beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the three DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture and for routing to other board resources.

Digital Upconverter and D/A Stage

One or two TI DAC5688 DUC (digital upconverters) and D/As accept baseband real or complex data stream from the FPGAs and provide that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 65,536x. The two interpolators can be combined to create a total range from 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
### Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Memory Resources
The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

### Specifications
**Model 57721**: 3 A/Ds, 1 DUC, 2 D/As
**Model 58721**: 6 A/Ds, 2 DUCs, 4 D/As

**Front Panel Analog Signal Inputs (3 or 6)**
- **Input**: Transformer-coupled, front panel female SSMC connectors
- **Transformer**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +8 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters (3 or 6)**
- **Type**: Texas Instruments ADS5485
- **Sampling Rate**: 10 MHz to 200 MHz
- **Resolution**: 16 bits

**Digital Downconverters (3 or 6)**
- **Decimation Range**: 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \)
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees

**FIR Filter**: 18-bit coefficients, 24-bit output, with user programmable coefficients

**Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

**D/A Converters (2 or 4)**
- **Type**: Texas Instruments DAC5688
- **Input Data Rate**: 250 MHz max.
- **Output IF**: DC to 400 MHz max.
- **Output Signal**: 2-channel real or 1-channel with frequency translation
- **Output Sampling Rate**: 800 MHz max. with 2x, 4x or 8x interpolation
- **Resolution**: 16 bits

**Digital Interpolators (1 or 2)**
- **Interpolation Range**: 2x to 65,536x in two stages of 2x to 256x

**Beamformers (1 or 2)**
- **Summation**: Three channels on-board; multiple boards can be summed via Summation Expansion Chain

**Summation Expansion Chain**: One chain in and one chain out link via VPX P2 connector using Aurora protocol

**Phase Shift Coefficients**: I & Q with 16-bit resolution

**Gain Coefficients**: 16-bit resolution

**Channel Summation**: 24-bit

**Multiboard Summation Expansion**: 32-bit

**Front Panel Analog Signal Outputs (2 or 4)**
- **Output**: Transformer-coupled, front panel female SSMC connectors

**Transformer**: Coil Craft WBC4-6TLB

**Full Scale Output**: +4 dBm into 50 ohms

**3 dB Passband**: 300 kHz to 700 MHz

**Sample Clock Sources (2 or 4)**
- **On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

**Clock Synthesizers (1 or 2)**
- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

**Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**External Clocks (1 or 2)**
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus (1 or 2)**: 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**Field Programmable Gate Arrays (1 or 2)**
- **Standard**: Xilinx Virtex-7 XC7VX330T-2
- **Optional**: Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- **Option -104**: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57721; P3 and P5 connectors, Model 58721

**Memory Banks (4 or 8)**
- **Type**: DDR3 SDRAM
- **Size**: 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8
- **Environmental**: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57730 and 58730 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a VPX carrier board. Model 57730 is a 6U board with one Model 71730 module while the Model 58730 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Dual-μSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

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**Pentek, Inc.**
One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc., can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reconfiguring the FPGA. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100usec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx IMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx IMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.

D/A Converter Stages

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2- or 1/4-rate input data. Analog output is through front panel SSMC connectors.

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

Pentek, Inc. One Park Way ∙ Upper Saddle River ∙ New Jersey 07458
Tel: 201-818-5900 ∙ Fax: 201-818-5904 ∙ Email: info@pentek.com

Tel: 201-818-5900 ∙ Fax: 201-818-5904 ∙ Email: info@pentek.com

www.pentek.com
1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 9192 Cobalt or Onyx Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LV TTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memory for many other purposes.

Specifications

Model 58730: 1 A/D, 1 D/A
Model 58730: 2 A/Ds, 2 D/As
Front Panel Analog Signal Inputs (1 or 2)
  Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
  Type: Texas Instruments ADS5400
  Sampling Rate: 100 MHz to 1 GHz
  Resolution: 12 bits
D/A Converters (1 or 2)
  Type: Texas Instruments DAC5681Z
  Input Data Rate: 1 GHz max.
  Interpolation Filter: bypass, 2x or 4x
  Output Sampling Rate: 1 GHz max.
  Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)
  Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)
  On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
  Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
  Type: Front panel female SSMC connector, LV TTL
  Function: Programmable functions include: trigger, gate, sync and PPS
  Field Programmable Gate Arrays (1 or 2)
  Standard: Xilinx Virtex-7 XC7VX330T-2
  Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O (1 or 2)
  Option -04: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730
  Option -05: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730

Memory Banks (4 or 8)
  Type: DDR3 SDRAM
  Size: 1 GB each
  Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
  Environmental: Level L1 & L2 air-cooled;
  Level L3 ruggedized, conduction-cooled
  Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
New! New! New! New! New!

■ Optional LVDS connections
■ Optional user-configurable
■ PCIe Express (Gen. 1, 2 & 3)
■ 4 or 8 GB of DDR3 SDRAM
■ Programmable one- or two-channel DDCs (Digital Downconverters)
■ 4 or 8 GB of DDR3 SDRAM
■ μSync clock/sync bus for multiboard synchronization
■ PCI Express (Gen. 1, 2 & 3) interface up to x8
■ Optional user-configurable gigabit serial interface
■ Optional LVDS connections to the Virtex-7 FPGA for custom I/O
■ Ruggedized and conduction-cooled versions available

Features
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- μSync clock/sync bus for multiboard synchronization
- PCIe Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

General Information
Models 57741 and 58741 are members of the Onyx family of high-performance 6U OpenVPX boards based on the Xilinix Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a VPX carrier board.

Model 57741 is a 6U board with one Model 71741 module while the Model 58741 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741.

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, four banks are used to store the single-channel of input data. In dual-channel mode, two memory banks store data from input channel 1 and two memory banks store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor's job of identifying and executing on the data.

DDC IP Core

Within each FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation.

In single-channel mode, the DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s where f_s is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s/N.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it's programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.
Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>57741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58741</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, with Wideband DDC, two Virtex-7 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:
- -076 XC7VX690T-2 FPGA
- -104 LVDS I/O between the FPGA and P3 connector, Model 57741; P3 and P5 connectors, Model 58741
- -105 Gigabit link between the FPGA and P2 connector, Model 57741; gigabit links from each FPGA to P2 connector, Model 78741

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converters (1 or 2)

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters (2 or 4)

Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)

- Front panel SSMC connector
- Timing Bus (1 or 2)
- 19-pin μSync bus connector includes sync and gate/trigger inputs, CML
- External Trigger Input (1 or 2)
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57741; P3 and P5, Model 58741
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57741; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58741

Memory Banks (4 or 8)

Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**General Information**

Models 57751 and 58751 are members of the Onyx® family of high-performance 6 U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a VPX carrier board.

Model 57751 is a 6U board with one Model 71751 module while the Model 58751 is a 6U board with two XMC modules rather than one.

These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/A and four or eight banks of memory.

**The Onyx Architecture**

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition and one or two D/A waveform playback IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57751; P3 and P5, Model 58751. Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57751; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58751.

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<td>GateXpress supports dynamic FPGA reconfiguration across PCIe</td>
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<td>Two or four 500 MHz 12-bit A/Ds</td>
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<td>Two or four multiband DDCs (digital downconverters)</td>
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<tr>
<td>One or two DUCs (digital upconverters)</td>
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<tr>
<td>Two or four 800 MHz 16-bit D/A</td>
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<tr>
<td>4 or 8 GB of DDR3 SDRAM</td>
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<td>Sample clock synchronization to an external system reference</td>
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<td>PCI Express (Gen. 1, 2 &amp; 3) interface up to x8</td>
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<td>LVPECL clock/sync bus for multiboard synchronization</td>
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<td>Optional LVDS connections to the Virtex-7 FPGA for custom I/O</td>
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<td>Ruggedized and conduction-cooled versions available</td>
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**Features**

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A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP Module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the dual D/A waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed.

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Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-9900 • Fax: 201-818-5904 • Email: info@pentek.com
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Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
### Specifications

**Model 57751:** 2 A/Ds, 2 DDCs, 1 DUC, 2 D/As  
**Model 58751:** 4 A/Ds, 4 DDCs, 2 DUCs, 4 D/As  

**Front Panel Analog Signal Inputs (2 or 4):**  
- **Input Type:** Transformer-coupled, front panel female SSMC connectors  
- **Transformer Type:** Texas Instruments ADS5463  
- **Sampling Rate:** 20 MHz to 50 MHz  
- **Resolution:** 12 bits  

**A/D Converters (standard) (2 or 4):**  
- **Type:** Texas Instruments ADS5474  
- **Sampling Rate:** 20 MHz to 400 MHz  
- **Resolution:** 14 bits  

**Digital Downconverters (2 or 4):**  
- **Decimation Range:** 2x to 131,072x in 2x to 256x and one fixed 2x stage  
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$  
- **LO SFDR:** >120 dB  
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees  
- **FIR Filter:** 16-bit coefficients, 24-bit output, with user programmable coefficients  
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation  
- **Input Data Rate:** 250 MHz max.  
- **Output IF:** DC to 400 MHz max.  
- **Output Signal:** 2-channel real or 1-channel with frequency translation  
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation  
- **Resolution:** 16 bits  

**Digital Interpolators (1 or 2):**  
- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x  
- **Total Interpolation Range (D/A and Digital combined):** 2x to 524,288x  

**Front Panel Analog Signal Outputs (2 or 4):**  
- **Output Type:** Transformer-coupled, front panel female SSMC connectors  
- **Transformer:** Texas Instruments DAC5688  
- **Input Data Rate:** 250 MHz max.  
- **Output Data Rate:** 20 MHz to 400 MHz max.  
- **Output Signal:** 2-channel real or 1-channel with frequency translation  
- **Output Sampling Rate:** 800 MHz max. with 2x, 4x or 8x interpolation  
- **Resolution:** 16 bits  

**Synchronization:**  
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus  
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock  

**External Clocks (1 or 2):**  
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference  

**Timing Bus:**  
- **Bus Type:** 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs  

**Field Programmable Gate Arrays (1 or 2):**  
- **Standard:** Xilinx Virtex-7 XC7VX330T-2  
- **Optional:** Xilinx Virtex-7 XC7VX690T-2  

**Custom I/O:**  
- **Option -04:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57751; P3 and P5, Model 58751  
- **Option -05:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57751; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58751  

**Memory Banks (4 or 8):**  
- **Type:** DDR3 SDRAM  
- **Size:** 1 GB each  
- **Speed:** 800 MHz (1600 MHz DDR)  

**PCI-Express Interface:**  
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8  
- **Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled  

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57760 and 58760 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a VPX carrier board.

Model 57760 is a 6U board with one Model 71760 module while the Model 58760 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PcLe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

**A/D Converter Stages**

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.

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**A/D Acquisition IP Modules**

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An onboard clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an onboard programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

- **A/D Converters (4 or 8)**
  - **Type:** Texas Instruments ADS5485
  - **Sampling Rate:** 10 MHz to 200 MHz
  - **Resolution:** 16 bits

- **Sample Clock Sources (1 or 2)**
  - On-board clock synthesizer

- **Clock Synthesizers (1 or 2)**
  - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

- **External Clocks (1 or 2)**
  - **Type:** Front panel female SSMC connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS

- **Field Programmable Gate Arrays (1 or 2)**
  - **Standard:** Xilinx Virtex-7 XC7VX330T
  - **Optional:** Xilinx Virtex-7 XC7VX690T

- **Custom I/O**
  - **Option -104:** Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760
  - **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760

- **Memory Banks (4 or 8)**
  - **Type:** DDR3 SDRAM
  - **Size:** 1 GB each
  - **Speed:** 800 MHz (1600 MHz DDR)

- **PCI-Express Interface**
  - **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
  - **Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
  - **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

General Information

Models 57761 and 58761 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71761 XMC modules mounted on a VPX carrier board.

Model 57761 is a 6U board with one Model 71761 module while the Model 58761 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds, programmable DDCs and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57761; P3 and P5, Model 58761.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- Multiboard programmable beamformer
- 4 or 8 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

For applications in which the Virtex-7 FPGA is not required, the VX330T or VX690T can be replaced with one of the lower-cost VX330T or VX310T devices to reduce costs. Pentek GateFlow FPGA Design Kits include all of the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.

The VX330T features 2000 DSP48E1 slices and is ideal for logic, encryption/decryption, and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57761; P3 and P5, Model 58761.

Block Diagram, Model 57761.

Model 58761 doubles all resources except the PCIe-to-PCIe Switch and provides 24 LVDS pairs from the 2nd FPGA to VPX-P5

Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators, one or two programmable beamforming IP cores, and one or two Aurora gigabit serial interfaces complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop FPGA IP.
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_c$, where $f_c$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_c/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_c/N$.

Beamformer IP Cores

In addition to the DDCs, these models feature a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A programmable summation block provides summing of any of the four DDC core outputs. An additional programmable gain stage compensates for summation change bit growth. A power meter and threshold detect block is provided for the summed output. The output is then directed back into the A/D Acquisition IP Module 1 FIFO for reading over the PCIe. For larger systems, multiple boards can be chained together via a built-in Xilinx Aurora gigabit serial interface. This allows summation across channels on multiple boards.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically

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[Diagram of FPGA dataflow]

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**Models**

57761 & 58761

4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com

www.pentek.com
reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts four or eight analog HF or IF inputs on front panel SSMC connectors with transformer coupling into Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
4- or 8-Channel 200 MHz A/D with DDCs and Virtex-7 FPGA - 6U OpenVPX

Specifications
Model 57761: 4 A/Ds,
Model 58761: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Digital Downconverters (4 or 8)
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Beamformers (1 or 2)
Summation: Four channels on-board; multiple boards can be summed via Summation Expansion Chain
Summation Expansion Chain: One chain in and one chain out link via VPX P2 connector using Aurora protocol
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Channel Summation: 24-bit Multiboard Summation Expansion: 32-bit Sample Clock Sources (1 or 2)
On-board clock synthesizer
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock
External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
Timing Bus: (1 or 2) 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -076: XC7VX690T-2 FPGA
-04: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57761; P3 and P5, Model 58761
Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
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<tr>
<th>Model</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>57761</td>
<td>4-Channel 200 MHz A/D with DDCs, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58761</td>
<td>8-Channel 200 MHz A/D with DDCs, two Virtex-7 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Option:
-076  XC7VX690T-2 FPGA
-104  LVDS I/O between the FPGA and P3 connector, Model 57761; P3 and P5 connectors, Model 58761

Contact Pentek for availability of rugged and conduction-cooled versions

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Models 57791 & 58791

1 or 2 L-Band RF Tuners, 2-or 4-Channel 500 MHz A/D, Virtex-7 FPGAs - 6U VPX

New!

General Information

Models 57791 and 58791 are members of the Onyx® family of high-performance 6U VPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71751 XMC modules mounted on a 6U VPX carrier board.

Model 57791 is a 6U board with one Model 71751 module while the Model 58791 is a 6U board with two XMC modules rather than one.

They include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include general purpose and gigabit serial connectors for application-specific I/O.

The Onyx Architecture

The Pentek Onyx Architecture features one or two Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The factory-installed functions include two or four A/D acquisition IP modules, four or eight DDR3 memory controllers, two or four DDCs (digital downconverters), RF tuner controllers, one or two clock and synchronization generators, one or two test signal generators, and a Gen 3 PCIe interface.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs handle L-Band input signal levels from -50 dBm to +10 dBm
- Programmable analog downconverters provide IF or I+Q baseband signals at frequencies up to 123 MHz
- Two or four 500 MHz 12-bit A/Ds digitize IF or I+Q signals synchronously; optional: 400 MHz 14-bit A/Ds
- Two or four FPGA-based multiband digital downconverters
- Xilinx Virtex-7 VX330T or VX690T FPGAs
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to external system reference
- PCI Express (Gen. 1, 2, & 3) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

These models can operate as complete turnkey solutions with no need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for control or data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the received signals.

For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57791; P3 and P5, Model 58791.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57791; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58791.

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer automatically adapts to the length of the acquisition gate. This is extremely useful in applications where acquisition is driven by an external gate of unknown or variable length.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting two different output bandwidths. Decimations can be set from 2 to 131,072 to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to one of three selectable frequency references: the timing generator output, an external reference input between 12 and 30 MHz, or an on-board crystal oscillator.

Together, the RF LNA and baseband amplifiers accommodate input signal levels from –50 dBm to +10 dBm. The integrated low pass filter has a 3 dB bandwidth of 123.75 MHz.

For best performance, the analog outputs of the MAX2121 should be used in the IF mode instead of the analog baseband I+Q mode. In this case, the IF signal is digitized by the A/D converter and then delivered to the DDC to produce perfectly balanced digital I+Q complex samples, 16 bits each.
1 or 2 L-Band RF Tuners, 2-or 4-Channel 500 MHz A/D, Virtex-7 FPGAs - 6U VPX

➤ In this case the IF signal frequency is chosen by setting an appropriate VCO tuning frequency, A/D sample clock frequency, and DDC decimation factor to achieve optimal flatness, anti-aliasing, SNR and SFDR performance, based on the Maxim 2121 datasheet specifications. All three of these parameters are programmable by the user.

A/D Converters and DDCs

The analog tuner outputs are digitized by two or four Texas Inst. ADS5463 500 MHz 12-bit A/D converters. Another benefit of using the preferred IF analog output mode is that two or four independent A/D and DDC channels are now available for digitizing and downconverting signals with different center frequencies and bandwidths.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and re-loading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Clocking & Synchronization

One or two internal timing generators provide all timing, gating, triggering and synchronization functions required by the A/D converters. They also serve as optional sources for the L-Band tuner references.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports four or eight independent 1 GB DDR3 SDRAMs for transient capture and buffering data to PCIe.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be used to support custom user-installed IP within the FPGA.

PCI Express Interface

Models 57791 and 58791 include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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## Specifications

**Model 57791**: 1 L-Band Tuner, 2 A/Ds, 2 DDCs, 1 FPGA

**Model 58791**: 2 L-Band Tuners, 4 A/Ds, 4 DDCs, 2 FPGAs

**Front Panel Analog Signal Inputs (1 or 2)**
- Connector: Front panel female SSMC
- Impedance: 50 ohms

**L-Band Tuner (1 or 2)**
- Type: Maxim MAX2121
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: –97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer: \( \text{freq}_{\text{VCO}} = (N \times \text{freq}_{\text{REF}}) \) where integer \( N \) = 19 to 251 and fractional \( F \) is a 20-bit binary value
- PLL Reference (freq\(_{\text{REF}}\)): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
- LNA Gain: 60 dB range, controlled by a programmable 12-bit D/A converter
- Usable Full-Scale Input Range: –50 dBm to +10 dBm
- Baseband Low Pass Filter: 3 dB cutoff frequency: 123.75 MHz

**A/D Converters (2 or 4)**
- Type: Texas Instruments ADS5463
- Sampling Rate: 10 MHz to 500 MHz
- Resolution: 12 bits
- Option -014: 400 MHz, 14-bit A/Ds

**Sample Clock Sources (1 or 2)**
- On-board timing generator/synthesizer

**A/D Clock Synthesizer (1 or 2)**
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

**Timing Generator External Clock Input (1 or 2)**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm
- AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus (1 or 2)**
- 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input (2 or 4)**
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array (1 or 2)**
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

**Custom I/O**
- Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57791; P3 and P5, Model 58791
- Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57791; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58791

**Memory Banks (4 or 8)**
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

**PCI-Express Interface**
- PCI Express Bus: Gen. 1, 2 or 3*: x4 or x8

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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## Ordering Information

**Model** | **Description**
--- | ---
57791 | L-Band RF Tuner with 2-Channel 500 MHz A/D with DDCs and Virtex-7 FPGA - 6U VPX
58791 | Two L-Band RF Tuners with 4-Channel 500 MHz A/D with DDCs and two Virtex-7 FPGAs - 6U VPX

**Options:**
- -014: 400 MHz, 14-bit A/Ds
- -076: XC7VX690T-2 FPGA
- -100: 27 MHz crystal for MAX2121
- -104: LVDS I/O between the FPGA and P3 connector, Model 57791; P3 and P5 connectors, Model 58791
- -105: Gigabit link between the FPGA and P2 connector, Model 57791; gigabit links from each FPGA to P2 connector, Model 78791

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Contact Pentek for availability of rugged and conduction-cooled versions

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**Model** | **Description**
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8264 | VPX Development System. See 8264 Datasheet for Options

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* Gen 3 requires a compatible backplane and SBC
8- or 16-Channel 250 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX

General Information

Models 57131 and 58131 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71131 XMC modules mounted on a VPX carrier board. Model 57131 is a 6U board with one Model 71131 module while the Model 58131 is a 6U board with two XMC modules rather than one.

They include eight or 16 A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, multiband DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the application.
A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight associated A/Ds or a test signal generator.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients.

The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, a sync and gate or trigger signals. An onboard clock generator receives an external sample clock from the front panel MMCX connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel MMCX connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. A front panel 12-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Up to three additional boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. For larger systems, the Model 7893 System Synchronizer supports additional boards in increments of eight or four.

Memory Resources

The architecture supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4...
Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and testing a development system.

Options:
- 16-Ch annel 250 MHz A/D
- 8-Ch annel 250 MHz A/D
- LVDS FPGA I/O
- XCKU115-2 FPGA
- XCKU060-2 FPGA
- XCKU035-2 FPGA

Model Description

Model 57131: 8 A/Ds;
Model 58131: 16 A/Ds
Front Panel Analog Signal Inputs (8 or 16)
Input Type: Transformer-coupled, front panel female MMXC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
5 dB Passband: 300 kHz to 700 MHz

A/D Converters (8 or 16)
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Digital Downconverters (8 or 16)
Decimation Range: 2x to 32,768x in three stages of 2x to 32x
LO Tuning Freq. Resolution: 32 bits, 0 to \(f_s\)
LO SFDR: >108 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)
On-board clock synthesizers

Clock Synthesizer (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock (1 or 2)
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
12-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input (1 or 2)
Type: Front panel female MMXC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector, Model 57131; and P5 connector, Model 58131 for custom I/O
Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Type: DDR4 SDRAM
Size: 5 GB Model 57131; 10 GB Model 58131
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 9.187 in. x 6.717 in. (233.35 mm x 170.60 mm)
Models 57132 & 58132

8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U VPX

General Information

Models 57132 and 58132 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71132 XMC modules mounted on a VPX carrier board. Model 57132 is a 6U board with one Model 71132 module while the Model 58132 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include eight or 16 A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Eight or 16 250 MHz 16-bit A/Ds
- Eight or 16 wideband DDCs
- 64 or 128 multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201.818.5900 • Fax: 201.818.5904 • Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

These models feature eight or 16 A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators. Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to fs, where fs is the A/D sampling frequency. Decimations can be programmed from 16 to 1024 in steps of 8.

The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of fs/N.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with FPGAs to match the specific requirements of the processing task. Included are the KU060 and the KU 115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57132; P3 and P5 connectors, Model 58132.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into eight or 16 TI ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synthesizing the internal oscillator.

Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied

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### SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

### Models

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57132</td>
<td>8-Channel 250 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>58132</td>
<td>16-Channel 250 MHz A/D with multiband DDCs and two Kintex UltraScale FGPA - 6U VPX</td>
</tr>
</tbody>
</table>

### Ordering Information

<table>
<thead>
<tr>
<th>Options</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-084</td>
<td>XCKU060-2 FPGA</td>
</tr>
<tr>
<td>-087</td>
<td>XCKU115-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P3, Model 57132; P3 and P5 Model 58132</td>
</tr>
<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P2</td>
</tr>
<tr>
<td>-702</td>
<td>Air cooled, Level L2</td>
</tr>
<tr>
<td>-713</td>
<td>Conduction cooled, Level L3</td>
</tr>
</tbody>
</table>

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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### 8- or 16-Channel 250 MHz A/D with Multiband DDCs and Kintex UltraScale FPGA - 6U VPX

- DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

#### PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

#### Specifications

<table>
<thead>
<tr>
<th>Model</th>
<th>57132: 8 A/Ds; Model 58132: 16 A/Ds</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front Panel Analog Signal Inputs (8 or 16)</td>
<td>Transformer-coupled, front panel female SSMC connectors</td>
</tr>
<tr>
<td>Transformer Type</td>
<td>Coil Craft WBC4-6TLB</td>
</tr>
<tr>
<td>Full Scale Input</td>
<td>+8 dBm into 50 ohms</td>
</tr>
<tr>
<td>3 dB Passband</td>
<td>300 kHz to 700 MHz</td>
</tr>
<tr>
<td>A/D Converters (8 or 16)</td>
<td>Type: Texas Instruments ADS5485</td>
</tr>
<tr>
<td>Sampling Rate</td>
<td>10 MHz to 200 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 bits</td>
</tr>
<tr>
<td>Multiband Digital Downconverters (64 or 128)</td>
<td>Decimation Range: 16x to 1024x in steps of 8</td>
</tr>
<tr>
<td>LO Tuning Freq. Resolution</td>
<td>32 bits, 0 to ( f_c )</td>
</tr>
<tr>
<td>LO SFDR</td>
<td>&gt;120 dB</td>
</tr>
<tr>
<td>Phase Offset Resolution</td>
<td>32 bits, 0 to 360 degrees</td>
</tr>
<tr>
<td>FIR Filter</td>
<td>24-bit coefficients, 24-bit output, user-programmable coefficients</td>
</tr>
<tr>
<td>Default Filter Set</td>
<td>80% bandwidth, &lt;0.3 dB passband ripple, &gt;100 dB stopband attenuation</td>
</tr>
</tbody>
</table>

#### Multiplier Digital Downconverters

- DDR4 SDRAM memory (1 or 2 banks)
- Type: DDR4 SDRAM
- Size: 5 GB or 10 GB
- Speed: 1200 MHz (2400 MHz DDR)

#### Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

#### Contact Pentek for complete specifications of rugged and conduction-cooled versions

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New

Model 58141

**General Information**

Models 57141 and 58141 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a VPX carrier board. Model 57141 is a 6U board with one Model 71141 module while the Model 58141 is a 6U board with two XMC modules rather than one.

They include two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

**The Jade Architecture**

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include two or four A/D acquisition and two or four D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, one or two test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

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**Features**

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One or two-channel mode with 6.4 GHz, 12-bit A/Ds
- Two-or four-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two or four-Channel 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/As waveforms stored in either on-board memory or off-board host memory. A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex baseband input signals. It is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option-104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.

Option-105 provides two 4x gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 2x.

Memory Resources

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

These models accept a sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal...
**Models 57141 & 58141**

For multichannel systems. The μSync bus includes gate, reset, and in and out reference clock signals. The Model 5792 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

### Specifications

**Model 57141 One A/D**  
**Model 58141 Two A/Ds**

**Front Panel Analog Signal Inputs (2 or 4)**  
**Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converters (1 or 2)**  
**Type:** ADC12DJ3200

**Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz

**Resolution:** 12 bits

**Input Bandwidth:** Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

**D/A Converters (2 or 4)**  
**Type:** Texas Instruments DAC38RF82

**Output Sampling Rate:** 6.4 GHz

**Resolution:** 14 bits

**Sample Clock Source (1 or 2)**  
Front panel SSMC connector

**Timing Bus (1 or 2)**  
19-pin μSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input (1 or 2)**  
**Type:** Front panel female SSMC connector, LVTTL

**Function:** Programmable functions include: trigger, gate, sync and PPS

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX</td>
</tr>
<tr>
<td>58141</td>
<td>2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, 4-Ch. 6.4 GHz D/A, 2 ea. UltraScale FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- 084 XCKU060-2 FPGA  
- 087 XCKU115-2 FPGA  
- 104 LVDS FPGA I/O  
- 105 Gigabit serial FPGA I/O  
- 702 Air cooled, Level L2  
- 713 Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
General Information

Models 57821 and 58821 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71821 XMC modules mounted on a VPX carrier board. Model 57821 is a 6U board with one Model 71821 module while the Model 58821 is a 6U board with two XMC modules rather than one.

They include three or six A/Ds, complete multiboard clock and sync sections, large DDR4 memory, three or six DDCs, one or two DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces.

The factory-installed functions for these models include three or six A/D acquisition and one or two waveform playback IP modules for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: three or six powerful, programmable DDC IP cores; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; programmable interpolators, and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Three or six 200 MHz 16-bit A/Ds
- Three or six multiband DDCs (digital downconverters)
- One or two DUCs (digital upconverters)
- Two or four 800 MHz 16-bit D/As
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

These models feature three or six A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from three A/Ds, or the test signal generators.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving three DDCs or each of the three A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

D/A Waveform Playback IP Module

The factory-installed models in these models include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board memory or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition rate etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex UltraScale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57821; P3 and P5 connectors, Model 58821.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts three or six analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into three or six Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other board resources.

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3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

➤ Digital Upconverter and D/A Stage

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sample rate. It delivers real or quadrature (I+Q) analog outputs to the 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/ Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture of these models supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
3- or 6-Channel 200 MHz A/D, DDCs, DUC, 2- or 4-Channel 800 MHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

**Specifications**

Model 57821: 3 A/Ds  
Model 58821: 6 A/Ds  
Front Panel Analog Signal Inputs (3 or 6)  
- **Input Type**: Transformer-coupled, front panel female SSMC connectors  
- **Transformer Type**: Coil Craft WBC4-6TLB  
  - **Full Scale Input**: +5 dBm into 50 ohms  
  - **3 dB Passband**: 300 kHz to 700 MHz  
- **A/D Converters (3 or 6)**  
  - **Type**: Texas Instruments ADS5485  
  - **Sampling Rate**: 10 MHz to 200 MHz  
  - **Resolution**: 16 bits  
- **Digital Downconverters (3 or 6)**  
  - **Decimation Range**: 2x to 32,768x in three stages of 2x to 32x  
  - **LO Tuning Freq. Resolution**: 32 bits, 0 to \( f_s \)  
  - **LO SFDR**: >120 dB  
  - **Phase Offset Resolution**: 32 bits, 0 to 360 degrees  
- **D/A Converters (1 or 2)**  
  - **Type**: Texas Instruments DAC5688  
  - **Input Data Rate**: 250 MHz max.  
  - **Output IF**: DC to 400 MHz max.  
  - **Output Signal**: 2-channel real or 1-channel with frequency translation  
  - **Output Sampling Rate**: 800 MHz max. with 2x, 4x or 8x interpolation  
  - **Resolution**: 16 bits  
- **Digital Interpolator Core (1 or 2)**  
  - **Interpolation Range**: 2x to 32,768x in three stages of 2x to 32x  
- **Total Interpolation Range (D/A and interpolator core combined)**: 2x to 262,144x  
- **Front Panel Analog Signal Outputs (2 or 4)**  
  - **Output**: Transformer-coupled, front panel female SSMC connectors  
  - **Transformer**: Coil Craft WBC4-6TLB  
  - **Full Scale Output**: +4 dBm into 50 ohms  
  - **3 dB Passband**: 300 kHz to 700 MHz  
- **Sample Clock Sources**: (1 or 2)  
  - **On-board clock**: synthesizer generates two clocks: one A/D clock and one D/A clock  
  - **Clock Synthesizer (1 or 2)**  
    - **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus  
    - **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz  
    - **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock  
  - **External Clock (1 or 2)**  
    - **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference  
- **Timing Bus**: (1 or 2)  
  - 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs  
- **Programmable Gate Array (1 or 2)**  
  - **Standard**: Xilinx Kintex UltraScale XCKU035-2  
  - **Option -084**: Xilinx Kintex UltraScale XCKU060-2  
  - **Option -087**: Xilinx Kintext UltraScale XCKU115-2  
- **Custom I/O**  
  - **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57821; P3 and P5 connectors, Model 58821  
  - **Option -105** provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols  
- **Memory (1 or 2)**  
  - **Type**: DDR4 SDRAM  
  - **Size**: 5 GB  
  - **Speed**: 1200 MHz (2400 MHz DDR)  
  - **PCI-Express Interface**  
  - **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8  
- **Environmental**  
  - **Standard**: L0 (air cooled)  
    - **Operating Temp**: 0° to 50° C  
    - **Storage Temp**: -20° to 90° C  
    - **Relative Humidity**: 0 to 95%, non-condensing  
  - **Option -702**: L2 (air cooled)  
    - **Operating Temp**: -20° to 65° C  
    - **Storage Temp**: -40° to 100° C  
    - **Relative Humidity**: 0 to 95%, non-condensing  
  - **Option -713**: L3 (condensation cooled)  
    - **Operating Temp**: -40° to 70° C  
    - **Storage Temp**: -50° to 100° C  
    - **Relative Humidity**: 0 to 95%, non-condensing  
  - **Size**: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)
New! New! New! New! New!

Ruggedized and conduction-cooled versions available

Compatible with several VITA standards including:
VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)

New! Models 57841 & 58841

1- or 2-Ch. 3.6 GHz and 2- or 4-Ch. 1.8 GHz, 12-bit A/Ds, with Wideband DDCs, Kintex UltraScale FPGAs - 6U VPX

General Information
Models 57841 and 58841 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture
Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include one or two A/D acquisition IP modules.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, RF In

Features
- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with one or two 3.6 GHz, 12-bit A/Ds
- Two-channel mode with two or four 1.8 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- 5 or 10 GB of DDR4 SDRAM
- μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including:
  VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or the test signal generators. The IP modules have associated a 5 or 10 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of the SDRAM is used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory is supported with a DMA engine for moving A/D data through the PCI-X interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode: In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In single-channel mode, decimation can be programmed to 8 or 16 to 512 in steps of 16.

In dual-channel mode, decimation can be programmed to 4 or 8 to 256 in steps of 8. In dual-channel mode, both channels share the same decimation rate.

In either mode, the DDC can be bypassed completely.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8\( f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 and P5 connectors for custom I/O.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The full-scale input level of the ADC12D1800 can be digitally trimmed from +2 dBm to +4 dBm to simplify system calibration. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.
Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered and equipped with sufficient cooling and power to ensure optimum performance.

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O to VPX P2, Model 57861; P2 and P5 Model 58861
- 105 Gigabit serial FPGA I/O to VPX P1
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Specifications

Model 57861: One A/D
Model 58861: Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input Level: may be trimmed from +2 dBm to +4 dBm with a 15-bit integer
Digital Downconverters (2 or 4)
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Single-channel mode: decimation can be programmed to 8 or 16 to 512 in steps of 16
Dual-channel mode: decimation can be programmed to 4 or 8 to 256 in steps of 8; both channels share the same decimation value
Either mode: the DDC can be bypassed completely
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB

Phases Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: (1 or 2)
Front panel SSMC connectors
Timing Bus: (1 or 2)
19-pin μSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P1 connector, Model 57861; and P5 connector, Model 58861 for custom I/O
Option -105 provides two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Type: DDR4 SDRAM
Size: 5 GB Model 57841; 10 GB Model 58841
Speed: 1200 MHz (2400 MHz DDR)

PCI Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50°C
Storage Temp: –20° to 90°C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65°C
Storage Temp: –40° to 100°C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: –40° to 70°C
Storage Temp: –50° to 100°C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**General Information**

Models 57851 and 58851 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71851 XMC modules mounted on a VPX carrier board. Model 57851 is a 6U board with one Model 71851 module while the Model 58851 is a 6U board with two XMC modules rather than one. They include two or four A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two or four DDCs, one or two DUC, and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.
A/D Acquisition IP Modules

These models feature two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, or a test signal generator.

Each acquisition module has a DMA engine for easily moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \) where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

D/A Waveform Playback IP Modules

The factory-installed functions in these models include one or two sophisticated D/A Waveform Playback IP modules. They allow users to easily play back to the dual or quad D/A waveforms stored in either on-board memory or off-board host memory.

> Xilinx Kintex UltraScale FPGA

Depending on the requirements of the processing task, the Kintex Ultrascale can be selected from a range of FPGAs spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57851; P3 and P5 connectors, Model 58851.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts two or four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into two Texas Instruments ADS5463 500 MHz, 12-bit A/D converters.

Optionally, the Texas Instruments ADS5474 400 MHz, 14-bit A/D may be factory-installed instead of the ADS5463.

The digital outputs are delivered into the Kintex FPGA for signal processing, data capture and for routing to other module resources.
**Models 57851 & 58851**

2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - 6U VPX

➤ **Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x. In addition to the DAC5688, an FPGA-based interpolator core provides additional interpolation from 2x to 32,768x. The two interpolators can be combined to create a total range from 2x to 262,144x.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly for either the A/D or D/A sections or can be divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52851’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The architecture of these models supports 5 or 10 GB of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller cores within the FPGA can take advantage of the memory for custom applications.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
2- or 4-Channel 500 MHz A/D, DDC, DUC, 2- or 4-Channel 800 MHz D/A and Kintex UltraScale FPGAs - 6U VPX

### Specifications

Model 57851: 2 A/Ds  
Model 58851: 4 A/Ds  
Front Panel Analog Signal Inputs (2 or 4)  
- Input Type: Transformer-coupled, front panel female SSMC connectors  
- Transformer Type: Coil Craft WBC4-6TLB  
- Full Scale Input: +5 dBm into 50 ohms  
- 3 dB Passband: 300 kHz to 700 MHz  
- A/D Converters (standard) (2 or 4)  
  - Type: Texas Instruments ADS5463  
  - Sampling Rate: 20 MHz to 500 MHz  
  - Resolution: 12 bits  
- A/D Converters (option -014) (2 or 4)  
  - Type: Texas Instruments ADS5474  
  - Sampling Rate: 20 MHz to 400 MHz  
  - Resolution: 14 bits  
- Digital Downconverters (2 or 4)  
  - Quantity: Two channels  
  - Decimation Range: 2x to 65,536x in three stages of 2x x 32x and one fixed stage of 2x  
  - LO Tuning Freq. Resolution: 32 bits, 0 to f_s  
  - LO SFDR: >120 dB  
  - Phase Offset Resolution: 32 bits, 0 to 360 degrees  
- FIR Filter: 16-bit coefficients, 24-bit output, with user programmable coefficients  
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation  

- D/A Converters (2 or 4)  
  - Type: Texas Instruments DAC5688  
  - Input Data Rate: 250 MHz max.  
  - Output IF: DC to 400 MHz max.  
  - Output Signal: 2-channel real or 1-channel with frequency translation  
  - Output Sampling Rate: 800 MHz max. with 2x, 4x or 8x interpolation  
  - Resolution: 16 bits  

- Digital Interpolator Core (1 or 2)  
  - Interpolation Range: 2x to 32,768x in one stage of 2x to 256x and one stage of 2x to 128x  
  - Total Interpolation Range (D/A and interpolator core combined): 2x to 262,144x  

- Front Panel Analog Signal Outputs (2 or 4)  
  - Output: Transformer-coupled, front panel female SSMC connectors  
  - Transformer Type: Coil Craft WBC4-6TLB  
  - Full Scale Output: +4 dBm into 50 ohms  
  - 3 dB Passband: 300 kHz to 700 MHz  

- Sample Clock Sources (1 or 2)  
- Clock Synthesizer (1 or 2)  
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus  

### Ordering Information

#### Models 57851 & 58851

- **2-Channel 500 MHz A/D**  
  - with DDCs, DUC with 2-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX  
  - Model: 57851  
  - Size: 5 GB  
- **4-Channel 500 MHz A/D**  
  - with DDCs, DUC with 4-Channel 800 MHz D/A, and Kintex UltraScale FPGA - 6U VPX  
  - Model: 58851  
  - Size: 5 GB  

#### Options:

- **-014**  
  - 400 MHz, 14-bit A/Ds  
- **-084**  
  - XCKU060-2 FPGA  
- **-087**  
  - XCKU115-2 FPGA  
- **-104**  
  - LVDS FPGA  
- **-105**  
  - Gigabit serial FPGA  
- **-702**  
  - Air cooled, Level L2  
- **-713**  
  - Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

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Pentek, Inc.  
One Park Way ● Upper Saddle River ● New Jersey 07458  
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  
www.pentek.com
Models 57861 & 58861

4- or 8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX

General Information

Models 57861 and 58861 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71841 XMC modules mounted on a VPX carrier board. Model 57841 is a 6U board with one Model 71841 module while the Model 58841 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; clock controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com
www.pentek.com
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be achieved including one A/D per DDC. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. Front-panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.
## SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57861</td>
<td>4-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>58861</td>
<td>8-Channel 200 MHz A/D with DDCs and Kintex UltraScale FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O to VPX P3, Model 57861; P3 and P5 Model 58861
- 105 Gigabit serial FPGA I/O to VPX P2
- 702 Air cooled, Level L2
- 713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

### PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

#### Specifications

<table>
<thead>
<tr>
<th>Model</th>
<th>57861: 4 A/Ds</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>58861: 8 A/Ds</td>
</tr>
<tr>
<td>Front Panel Analog Signal Inputs (4 or 8)</td>
<td>Input Type: Transformer-coupled, front panel female SSMC connectors</td>
</tr>
<tr>
<td></td>
<td>Transformer Type: Coil Craft WBC4-6TLB</td>
</tr>
<tr>
<td></td>
<td>Full Scale Input: +8 dBm into 50 ohms</td>
</tr>
<tr>
<td></td>
<td>3 dB Passband: 300 kHz to 700 MHz</td>
</tr>
<tr>
<td>A/D Converters (4 or 8)</td>
<td>Type: Texas Instruments ADS5485</td>
</tr>
<tr>
<td></td>
<td>Sampling Rate: 10 MHz to 200 MHz</td>
</tr>
<tr>
<td></td>
<td>Resolution: 16 bits</td>
</tr>
<tr>
<td>Digital Downconverters (4 or 8)</td>
<td>Quantity: Four channels</td>
</tr>
<tr>
<td></td>
<td>Decimation Range: 2x to 32,768x in three stages of 2x to 32x</td>
</tr>
<tr>
<td></td>
<td>LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$</td>
</tr>
<tr>
<td></td>
<td>LO SFDR: &gt;120 dB</td>
</tr>
<tr>
<td></td>
<td>Phase Offset Resolution: 32 bits, 0 to 360 degrees</td>
</tr>
<tr>
<td></td>
<td>FIR Filter: 24-bit coefficients, 24-bit output, user-programmable coefficients</td>
</tr>
<tr>
<td></td>
<td>Default Filter Set: 80% bandwidth, &lt;0.3 dB passband ripple, &gt;100 dB stopband attenuation</td>
</tr>
<tr>
<td>Sample Clock Sources: (1 or 2)</td>
<td>On-board clock synthesizer</td>
</tr>
<tr>
<td>Clock Synthesizer (1 or 2)</td>
<td>Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus</td>
</tr>
<tr>
<td></td>
<td>Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz</td>
</tr>
<tr>
<td></td>
<td>Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock</td>
</tr>
</tbody>
</table>

**External Clock (1 or 2)**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus (1 or 2)**
- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input (1 or 2)**
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array (1 or 2)**
- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57861; P3 and P5 connectors, Model 58861, for custom I/O
- Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols

**Memory (1 or 2 banks)**
- Type: DDR4 SDRAM
- Size: 5 GB or 10 GB
- Speed: 1200 MHz (2400 MHz DDR)

**PCI-Express Interface**
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

**Environmental**
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: -20° to 65° C
  - Storage Temp: -40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: -40° to 70° C
  - Storage Temp: -50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Size: Board 9.187 in x 6.717 in (233.35 mm x 170.60 mm)
General Information

Models 57862 and 58862 are members of the Jade family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71862 XMC modules mounted on a VPX carrier board. Model 57862 is a 6U board with one Model 71862 module while the Model 58862 is a 6U board with two XMC modules rather than one.

They include four or eight A/Ds, complete multiboard clock and sync sections, and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight multiband DDCs
- 5 or 10 GB of DDR4 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc., One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the A/Ds or test signal generators.

Each IP module has an associated DMA engine for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module are two powerful DDC IP cores. A single-channel wideband DDC core and an eight-channel multiband DDC core. Each Acquisition Module can choose between the two cores allowing for a very flexible downconversion solution.

Each wideband DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting. Decimations can be programmed from 2 to 32.

Each multiband DDC has eight DDC channels each with its own independent 32-bit tuning frequency setting that ranges from DC to $f_s$ where $f_s$ is the A/D sampling frequency. Decimations can be programmed from 2 to 1024.

The decimating filter for all DDCs accept a unique set of user-supplied 24-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57862; P3 and P5 connectors, Model 58862.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front panel SSMC connectors with transformer coupling into four or eight TI ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Kintex UltraScale FPGAs for signal-processing or routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Front -panel 26-pin LVPECL Clock/Sync connectors allow multiple boards to be synchronized. In the slave mode, they accept LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied
**SPARK Development Systems**

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8268), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

## Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57862</td>
<td>4-Channel 200 MHz A/D with multiband DDCs and Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>58862</td>
<td>8-Channel 200 MHz A/D with multiband DDCs and 2 Kintex UltraScale FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 084  XCKU060-2 FPGA
- 087  XCKU115-2 FPGA
- 104  LVDS FPGA I/O to VPX P3, Model 57862; P3 and P5 Model 58862
- 105  Gigabit serial FPGA I/O to VPX P2
- 702  Air cooled, Level L2
- 713  Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions.

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### 4 or 8-Channel 200 MHz A/D with Multiband DDCs and Kintex UltraScale FPGAs - 6U VPX

- DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

#### PCI Express Interface

These models include industry-standard interfaces fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interfaces include multiple DMA controllers for efficient transfers to and from the boards.

#### Specifications

**Model 57862:** 4 A/Ds; **Model 58862:** 8 A/Ds

- **Front Panel Analog Signal Inputs (4 or 8):** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms, 3 dB Passband: 300 kHz to 700 MHz

#### A/D Converters (4 or 8)

- **Type:** Texas Instruments AD55485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

#### Wideband Digital Downconverters (4 or 8)

- **Decimation Range:** 2x to 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to 360 degrees
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

#### Multiband Digital Downconverters (4 or 8)

- **Decimation Range:** 2x to 1024x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to 360 degrees
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 24-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

#### Sample Clock Sources: (1 or 2)

- On-board clock synthesizer

#### Clock Synthesizer (1 or 2)

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing reference
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

#### Clock Dividers:

- External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

#### External Clock (1 or 2)

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

#### Timing Bus (1 or 2)

- 26-pin connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input (1 or 2)

- **Type:** Front panel female SSMC connector, LVITTL

#### Field Programmable Gate Array (1 or 2)

- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

#### Custom I/O

- **Option -104** provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57862; P3 and P5 connectors, Model 58862, for custom I/O
- **Option -105** provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols

#### Memory (1 or 2 banks)

- **Type:** DDR4 SDRAM
- **Size:** 5 GB or 10 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

#### PCI-Express Interface

- **PCI Express Bus: Gen. 1, 2 or 3: x4 or x8**

#### Environmental

- **Standard:** L0 (air cooled)
- **Operational Temp:** 0° to 50°C
- **Storage Temp:** -20° to 90°C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -702:** L2 (air cooled)
- **Operational Temp:** -20° to 65°C
- **Storage Temp:** -40° to 100°C
- **Relative Humidity:** 0 to 95%, non-condensing

- **Option -713:** L3 (conduction cooled)
- **Operational Temp:** -40° to 70°C
- **Storage Temp:** -50° to 100°C
- **Relative Humidity:** 0 to 95%, non-condensing

#### Size:

- Board 9.187 in x 6.717 in (233.35 mm x 170.60 mm)
Kintex UltraScale FPGA Coprocessor - 6U VPX

Models 57800 & 58800

General Information

Models 57800 and 58800 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71800 XMC modules mounted on a VPX carrier board. Model 57800 is a 6U board with one Model 71800 module while the Model 58800 is a 6U board with two XMC modules rather than one.

In addition to supporting PCI Express Gen. 3 as a native interface, the Model 57800 and Model 58800 include optional high-bandwidth serial and parallel connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed functions ideally matched to the board’s interfaces. The factory-installed functions in these models include one or two test signal generators, one or two metadata generators, one or two DDR4 SDRAM controllers, and DMA engines for moving data on and off the board.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite.

In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the wide range of IP functions contained in the Navigator IP library, or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.

The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800.

Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.
SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267), or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Specifications

Front Panel Digital I/O Interface

These models include one or two 80-pin front panel connectors that provide 38 or 76 LVDS pairs connected to one or both of the FPGAs. With user IP, these can be utilized for a control and status interface to other components of the system or as a data path.

Specifications

Front Panel Digital I/O (1 or 2)

- Connector Type: 80-pin connector, mates to a ribbon cable connector
- Signal Quantity: 38 or 76 pairs
- Signal Type: LVDS

Field Programmable Gate Array (1 or 2)

- Standard: Xilinx Kintex UltraScale XCKU035-2
- Option -084: Xilinx Kintex UltraScale XCKU060-2
- Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O (1 or 2)

- Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57800; P3 and P5 connectors, Model 58800
- Option -105 provides two 4X gigabit serial links between the FPGA and the VPX P2 connector to support serial protocols

Memory (1 or 2)

- Type: DDR4 SDRAM
- Size: 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: −20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -702: L2 (air cooled)
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- Option -713: L3 (conduction cooled)
  - Operating Temp: −40° to 70° C
  - Storage Temp: −50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size:

- 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Ordering Information

Model Description

57800 Kintex UltraScale FPGA Coprocessor - 6U VPX
58800 Double Kintex UltraScale FPGA Coprocessors - 6U VPX

Options:

-084 XCKU060-2 FPGA
-087 XCKU115-2 FPGA
-104 LVDS FPGA I/O
-105 Gigabit serial FPGA I/O
-702 Air cooled, Level L2
-713 Conduction cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201.818-5900 • Fax: 201.818-5904 • Email: info@pentek.com
www.pentek.com
General Information

The Model 8264 is a fully-integrated, 6U VPX development system for Pentek Cobalt® and Onyx® software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 9U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19” 9U rackmount chassis that is 16” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

All 8264 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8264 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

- Operating System: 64-bit Windows 7
- Processor: Intel Core i7 processor
- Clock Speed: 3.6 GHz
- SDRAM: 16 GB
- Dimensions: 6U Chassis, 19” W x 16” D x 10.5” H
- Weight: 50 lb, approx.
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model 8264 6U OpenVPX Development System for Cobalt and Onyx Boards

Options:
- 094 64-bit Linux OS
- 095 64-bit Windows 7 OS

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
## MODEL DESCRIPTION

- **5973**: Virtex-7 Processor and FMC Carrier - 3U VPX
- **5983**: Kintex UltraScale Processor and FMC Carrier - 3U VPX
- **7070**: Virtex-7 Processor and FMC Carrier - x8 PCIe
- **3312**: 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - FMC
- **5973-312**: FlexorSet: 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **5983-313**: FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **7070-312**: FlexorSet: 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCIe
- **3313**: 4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A w. DDC - FMC
- **5973-313**: FlexorSet: 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **5983-313**: FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **7070-313**: FlexorSet: 4-Channel 250 MHz 16-bit A/D with DDCs, 2-Channel 800 MHz 16-bit D/A - x8 PCIe
- **3316**: 8-Channel 250 MHz, 16-bit A/D - FMC
- **5973-316**: FlexorSet: 8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX
- **5983-317**: FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **7070-316**: FlexorSet: 8-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCI
- **5973-317**: FlexorSet: 8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX
- **7070-317**: FlexorSet: 8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe
- **3320**: 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC
- **5973-320**: FlexorSet: 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - 3U VPX
- **5983-320**: FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **7070-320**: FlexorSet: 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - x8 PCIe
- **3324**: 4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - FMC
- **5973-324**: FlexorSet: 4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - 3U VPX
- **5983-324**: FlexorSet: Kintex 4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A - 3U VPX
- **7070-324**: FlexorSet: 4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - x8 PCIe
- **8266**: PC Development System for PCIe Cobalt, Onyx and Flexor Boards
- **8267**: 3U VPX Development System for Cobalt, Onyx and Flexor Boards
- **3324-990**: Reference Design for the Xilinx VC707 Evaluation Kit

### Customer Information

**RADAR & SDR I/O - PMC/XMC**
**RADAR & SDR I/O - CompactPCI**
**RADAR & SDR I/O - x8 PCI Express**
**RADAR & SDR I/O - 3U VPX - FORMAT 1**
**RADAR & SDR I/O - AMC**
**RADAR & SDR I/O - 3U VPX - FORMAT 2**
**RADAR & SDR I/O - 6U VPX**

Last updated: April 2018
3U OpenVPX Virtex-7 Processor and FMC Carrier

General Information

The Flexor® Model 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCIe Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building a custom system.

The 8267 is designed to fill the void for Pentek Cobalt, Onyx and Flexor 3U VPX board developers and testing a development system for rugged and conduction-cooled applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit serial links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5973 supports the emerging VITA-66.4 standard, that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The 5973 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Specifications

I/O Module Interface: VITA-57.1, High Pin Count FMC site

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X optical lanes

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

The JadeFXTM Model 5983 is a high-performance 3U OpenVPX board based on the Xilinx Kintex UltraScale FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5983 includes a VITA-57.4 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface Flexor® FMCs to create a FlexorSet, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Jade family of Kintex UltraScale products, the JadeFX 5983 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering, and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 5983 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform generation engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel timing and sample-count information.

IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can ➤

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGAs
- 9 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Kintex UltraScale FPGA for custom I/O
- Optional optical Interface for backplane gigabit serial interboard communication
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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Model 5983

3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Model 5983

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5983 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

I/O Module Interface: VITA-57.4, High Serial Pin-Count FMC site

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O

Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental

Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

Model 5983 3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Options:
-087 XCKU115-2 FPGA
-110 VITA-66.4 12X optical interface
-180 GPS Support
-702 Air cooled, Level L2
-763 Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx, OnyxFx and JadeFX 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

FlexorSet Product Combinations

If you wish to purchase this FMC Carrier in combination with an FMC module, please see:

FlexorSet Model 5983-313
FlexorSet Model 5983-317
FlexorSet Model 5983-320
FlexorSet Model 5983-324

Model 8267

8267 VPX Development System

See 8267 Datasheet for Options

Model Description
8267 VPX Development System

Contact Pentek for availability of rugged and conduction-cooled versions

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FlexorSet Model 5983-313
FlexorSet Model 5983-317
FlexorSet Model 5983-320
FlexorSet Model 5983-324

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Options:

Data Plane – 2 Fat Pipes
Expansion Plane – 8 Pairs
Control Plane* – 2 Ultra-Thin Pipes
User Defined

VITA 65 Aperture E (VITA-66.4)

* not connected on board

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Contact Pentek for availability of rugged and conduction-cooled versions

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Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201 818-5900 Fax: 201 818-5904 Email: info@pentek.com

www.pentek.com
PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

General Information

The Flexor® Model 7070 is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 retains all of the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC module, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample-count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070 and installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCIe Express (Gen. 1, 2 and 3) interface up to x8
- Optional user-configurable 12X optical gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Commercial and extended-temperature versions available
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**FMC Product Combinations**

If you wish to purchase this FMC Carrier in combination with an A/D FMC module, please see:

- FlexorSet Model 7070-312
- FlexorSet Model 7070-313
- FlexorSet Model 7070-316
- FlexorSet Model 7070-317
- FlexorSet Model 7070-320
- FlexorSet Model 7070-324

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**Ordering Information**

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<th>Model</th>
<th>Description</th>
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<tr>
<td>7070</td>
<td>PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe</td>
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**Options:**

- 076  
  XC7VX690T-2 FPGA
- 104  
  16 pairs LVDS FPGA I/O
- 110  
  12x gigabit serial optical I/O

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**Contact Pentek for availability of extended-temperature versions**

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**Model 7070**

**PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe**

**Xilinx Virtex-7 FPGA**

The 7070 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided for the FPGA and a card edge connector for custom I/O. For applications requiring custom gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on a PCIe slot panel that can be installed in an empty, adjacent PCIe slot.

When configured with a VX330T FPGA, four duplex lanes are available.

**GateXpress for FPGA Configuration**

The 7070 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

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**Specifications**

- **I/O Module Interface:** VITA-57.1, High Pin Count FMC site
- **Field Programmable Gate Array**
  - **Standard:** Xilinx Virtex-7 XC7VX330T-2
  - **Optional:** Xilinx Virtex-7 XC7VX690T-2
- **Custom FPGA I/O**
  - **Parallel, Option -104:** 16 pairs of LVDS connections between the FPGA and a card-edge connector.
  - **Optical (Option -110):** User-configurable 12X (VX690T) or 4X (VX 330T) optical gigabit serial interface, MTP connector installed in an empty adjacent slot.
- **Memory**
  - **Type:** DDR3 SDRAM
  - **Size:** Four banks, 1 GB each
  - **Speed:** 800 MHz (1600 MHz DDR)
- **PCI-Express Interface**
  - **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;
  - **Environmental:** Level L1 & L2 air cooled,
  - **Size:** Half-length PCIe card

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**Pentek, Inc.**

One Park Way  •  Upper Saddle River  •  New Jersey 07458

Tel: 201-818-5900  •  Fax: 201-818-5904  •  Email: info@pentek.com

www.pentek.com
General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3312 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

The true performance of the 3312 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

Performance of the Model 3312

With the 3312 installed on either the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3312’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

D/A Waveform Generator IP Module

With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.
**FMC Interface**

The Model 3312 complies with the VITA S7 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If interpolation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

**Board Support Packages**

Pentek’s BSPs provide control of the 3312’s hardware and IP-based functions. Ready to run examples and a fully-sourced library provide a powerful, quick-start platform to create custom applications. BSPs are compatible with Windows and Linux operating systems. ReadyFlow BSP is used with OnyxFX Virtex-7 FPGA carriers and Navigator BSP is used for all new development going forward including the JadeFX Kintex UltraScale carriers.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the development kit to completely replace the Pentek IP with their own.

**Model 3312 Specifications**

- **Front Panel Analog Signal Inputs**
  - **Input Type:** Transformer-coupled, front panel connectors
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Input:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz
- **A/D Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Sampling Rate:** 800 MHz max. with interpolation
  - **Resolution:** 16 bits
- **D/A Converters**
  - **Type:** Texas Instruments ADS42LB69
  - **Input Type:** Texas Instruments DAC5688
- **External Clock**
  - **Type:** Texas Instruments DAC5688
- **Clock Source**
  - **Type:** Texas Instruments ADS42LB69
- **Sample Clock Sources**
  - **On-board clock synthesizer generates two clocks:** an A/D clock and a D/A clock
- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
- **Environmental:** Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized
- **I/O Module Interface:** VITA-57.1, High-Pin-Count FMC

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**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>3312</td>
<td>4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A FMC module</td>
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</tbody>
</table>

**Options:**
- 3312-990 Reference design for 3312 installed on Xilinx VC707 Evaluation Kit

**3U FlexorSet Description**

| 5973-312 | 4-Channel 250 MHz A/D with Virtex-7 FPGA |
| 5973-313 | 4-Channel 250 MHz A/D, Virtex-7 FPGA with 4 multiband DDCs and interpolator |
| 5983-313 | 4-Channel 250 MHz A/D, Kintex UltraScale FPGA with 4 multiband DDCs and interpolator |

**PCle FlexorSet Description**

| 7070-312 | 4-Channel 250 MHz A/D with Virtex-7 FPGA - x8 |
| 7070-313 | 4 Channel 250 MHz A/D, Virtex-7 FPGA with 4 DDCs and interpolator - x8 |

Contact Pentek for availability of rugged and conduction-cooled versions and other support options.
### Pentek FlexorSet Models

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>FPGA Type</th>
<th>Carrier Model</th>
<th>FMC Model</th>
<th>FlexorSet Model</th>
<th>Description</th>
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<tr>
<td>3U VPX</td>
<td>Virtex-7</td>
<td>5973</td>
<td>3312</td>
<td>5973-312</td>
<td>4 Ch 250 MHz A/D &amp; 2 Ch 800 MHz D/A</td>
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<td></td>
<td>5973-313</td>
<td>As above with 4 multiband DDCs &amp; interpolation filters</td>
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<td>3316</td>
<td>8 Ch 250 MHz 16-bit A/D</td>
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<td></td>
<td>5973-316</td>
<td>As above with 8 multiband DDCs</td>
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<td></td>
<td>3320</td>
<td>2 Ch 3 GHz A/D &amp; 2 Ch 2.8 GHz MHz D/A</td>
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<td></td>
<td>3324</td>
<td>4 Ch 500 MHz A/D &amp; 4 Ch 2 GHz D/A</td>
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<tr>
<td></td>
<td>Kintex UltraScale</td>
<td>5983</td>
<td>3312</td>
<td>5983-313</td>
<td>4 Ch 250 MHz A/D &amp; 2 Ch 800 MHz D/A</td>
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<td>5983-317</td>
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<td>8 Ch 250 MHz 16-bit A/D</td>
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<td></td>
<td>3324</td>
<td>4 Ch 500 MHz A/D &amp; 4 Ch 2 GHz D/A</td>
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</table>
General Information

Model 5973 is a member of the OnyxFx® family of high-performance 3U VPX baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5973-312 FlexorSet™ combines the Model 5973 and the Model 3312 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz 16-bit A/Ds, one digital upconverter, two 800 MHz 16-bit D/A’s, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-312 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP for DDR3 SDRAM memories.

The 5973-312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/A waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- Includes Xilinx Virtex-7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/A’s
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCIe Xpress (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 5973-312 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5973-312 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Virtex-7 FPGA

The 5973-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols. Sixteen pairs of LVDS connections between the FPGA and the VPX P2 connector for synchronization and custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed.

In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. ➤
FlexorSet
Model 5973-312

PCI Express Interface
The Model 5973-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources
The 5973-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

SPARK Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266, a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>5973-312</td>
<td>4-Channel 250 MHz A/D, 2-Channel 800 MHz 16-bit D/A with DUC - 3U VPX</td>
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<table>
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<tr>
<th>Options</th>
<th>Description</th>
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<td>-076</td>
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<tr>
<td>-110</td>
<td>VITA-66.4 12X optical interface</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A with DUC - 3U VPX

- In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage
The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

D/A Converters
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

Environmental
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)
- **Environmental:** Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Contact Pentek for availability of rugged and conduction-cooled versions.

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-313 FlexorSet™ combines the Model 5983 and the Model 3313 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FPGA carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-313 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a powerful DDC core.

The 5983-313 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can...
A/D Acquisition IP Modules

The 5983-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5983-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8\( f_s/N \) where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

inte grate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983-313 can be optionally populated with one of two Xilinx UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.
FlexorSet
Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

➤ The 5983-313 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

A/D Converter Stage
The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage
A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65,536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

PCI Express Interface
The Model 5983-313 includes an industry-standard interface fully compliant with PCIe Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources
The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

4-Channel Digital Downconverter
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to fs
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit user-programmable coefficients, 24-bit output
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- Phase Shift Coefficients: I & Q with 16-bit resolution
- Gain Coefficients: 16-bit resolution

provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.
SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications, Continued

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Total Interpolation Range
D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel connector
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: −20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: −20° to 65° C
Storage Temp: −40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: −40° to 70° C
Storage Temp: −50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

Model | Description
--- | ---
5983-313 | 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpolation and Kintex Ultra-Scale FPGA - 3U VPX

Options:
-087 | XCKU115-2 FPGA
-110 | VITA-66.4 12X optical interface
-180 | GPS Support
-702 | Air cooled, Level L2
-763 | Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model | Description
--- | ---
8267 | VPX Development System

See 8267 Datasheet for Options

Options:
General Information

Model 7070-312 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-312 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.
The 7070-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTOptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving iMPACT. Once booted, GateXpress allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the reconfigurations.
PCI Express Interface

The Model 7070-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 7070-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
--- | ---
7070-312 | 4-Channel 250 MHz A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCIe

Options:

-076 | XC7VX690T-2 FPGA
-076 | LVDS FPGA I/O to card-edge connector
-110 | 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model 8266

PC Development System
See 8266 Datasheet for Options

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A - x8 PCIe

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel connector
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

The 3312 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-313 3U VPX or the FlexorSet 7070-313 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loop-back mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s task of identifying and executing on the data.

D/A Waveform Playback IP Module

With the 5973 or the 7070 carrier, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming.
General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

The 3312 is available as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-312 3U VPX or the FlexorSet 7070-312 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support for the 3312 when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be best unlocked when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform recorder IP module.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform generator IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s task of identifying and executing on the data.

D/A Waveform Generator IP Module

With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from generator trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming.

Features

- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carriers as FlexorSets
- Ruggedized and conduction-cooled versions available
**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3312’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3312 or 7070/3312 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3312 complies with the VITA 57 High-Pin-Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

**Model 3312 Specifications**

- **Front Panel Analog Signal Inputs**
  - **Input Type:** Transformer-coupled, front panel connectors
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Sampling Rate:** 800 MHz max. with interpolation
  - **Resolution:** 16 bits

- **Digital Upconverters and D/A Converters**
  - **Type:** Texas Instruments ADS42LB69
  - **Sampling Rate:** 10 MHz to 250 MHz
  - **Resolution:** 16 bits

- **A/D Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Sampling Rate:** 800 MHz max. with interpolation
  - **Resolution:** 16 bits

- **Front Panel Analog Signal Outputs**
  - **Output Type:** Transformer-coupled, front panel connector
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

- **Sample Clock Sources:** On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks

- **External Clock**
  - **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- **External Trigger Input**
  - **Type:** Front panel connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS

- **Environmental**
  - **Level 1 & 2 air cooled, Level 3 conduction-cooled, ruggedized**

- **I/O Module Interface:** VITA-57.1, High-Pin Count FMC

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**Ordering Information**

<table>
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<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>3312</td>
<td>4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A with DUC - FMC module</td>
</tr>
</tbody>
</table>

**Options:**

- 3312-990 Reference design for 3312 installed on Xilinx VC707 Evaluation Kit

**FlexorSet Description**

- 5973-312 3U VPX FlexorSet for 3312
- 5973-313 3U VPX FlexorSet for 3312 with DDCs and interpolator
- 7070-312 PCIe FlexorSet for 3312
- 7070-313 PCIe FlexorSet for 3312 with DUCs and interpolator

Contact Pentek for availability of rugged and conduction-cooled versions and other support options.
New! New! New! New! New!

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

General Information

Model 5973 is a member of the OnyxFX® family of high-performance 3U VPX baseboards with a Xilinx Virtex-7 FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5973-313 FlexorSet™ combines the Model 5973 and the Model 3312 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The Model 5973-313 includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-313 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful D/A core. The 5973-313 features a sophisticated D/A waveform recorder IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- Includes Xilinx Virtex-7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- Sample clock synchronization to an external system reference
- PCIe Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 5973-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5973-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Xilinx Virtex-7 FPGA

The 5973-313 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.
GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.
### 4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

#### PCI Express Interface

The Model 5973-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

#### Memory Resources

The 5973-313 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

#### Specifications

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

**4-Channel Digital Downconverter**

- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit user-programmable coefficients, 24-bit output
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** 1 & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

**D/A Converters**

- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

**Digital Interpolator**

- **Interpolation Range:** 2x to 65,536x in two stages of 2x to 256x
- **Total Interpolation Range:** D/A and digital combined: 2x to 524,288x

**Front Panel Analog Signal Outputs**

- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources:**

- On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**External Trigger Input**

- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

**Custom FPGA I/O**

- **4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.**

**Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

**Optical (Option -110):** VITA-66.4, 12X duplex lanes

**Memory**

- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

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**Ordering Information**

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**Options:**

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<tr>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
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<td>-110</td>
<td>VITA-66.4 12X optical I/O with XC7VX690T FPGA, 4X w. XC7VX330T</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

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Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com  www.pentek.com
General Information

Model 5983 is a member of the JadeFx™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-313 FlexorSet™ combines the Model 5983 and the Model 3313 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FPGA carrier returns all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-313 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a powerful DDC core.

The 5983-313 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/A waveform stores in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can 

![FlexorSet Model 5983-313](image)
**A/D Acquisition IP Modules**

The 5983-313 features four A/D Acquisition IP Modules for easy capture and data movement. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Generator IP Module**

The 5983-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/A.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**DCC ICs**

Within each A/D Acquisition IP Module is a powerful DCC IC core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DCC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DCC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmable from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DCC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DCC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Each DCC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DCC core output in easy-to-read registers.

In addition, each DCC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DCC core falls below or exceeds a programmable threshold.

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator Kit to completely replace the Pentek IP with their own.

**Xilinx Kintex UltraScale FPGA**

The 5983-313 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

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**Pentek, Inc.**
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

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The 5983-313 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65,536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

PCI Express Interface

The Model 5983-313 includes an industry-standard interface fully compliant with PCIe Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters

- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

4-Channel Digital Downconverter

- **Decimation Range:** 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to fs
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit user-programmable coefficients, 24-bit output

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Phase Shift Coefficients: I & Q with 16-bit resolution

Gain Coefficients: 16-bit resolution

Gain Coefficients: 16-bit resolution
FlexorSet
Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

General Information
Model 7070-313 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

The Model 7070-313 includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture
Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-313 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains a powerful DDC core.

The 7070-313 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed functions and enable the 7070-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Features
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  www.pentek.com
Tel: 201 818-5900  Fax: 201-818-5904  Email: info@pentek.com

Model 3312 FMC

Model 7070 FMC Carrier

GTX
Serial I/O
GIGABIT
SERIAL интерфейс
VIRTEX-7 FPGA
VX330T or VX690T

FPGA Configure Bus
PCIE Gen. 3 x8

GateXpress PCIe Configuration Manager

GTX
Serial I/O
GIGABIT SERIAL интерфейс
VIRTEX-7 FPGA
VX330T or VX690T

FPGA Configure Bus
PCIE Gen. 3 x8

GateXpress PCIe Configuration Manager

Model 3312 FMC

Model 7070 FMC Carrier

PV Generator
Clock / Sync / Gate / PPS

Sample Clock / Reference Clock / Gate / Trigger / Sync / PPS

VCXO

ADC Clock/Sync Bus

DAC Clock/Sync Bus

Generator
Clock / Sync / Gate

VCXO

Upconverting

Downconverting

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe
A/D Acquisition IP Modules

The 7070-313 features four A/D Acquisition IP Modules for easy capture and data movement. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The 7070-313 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s / N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s / N \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Xilinx Virtex-7 FPGA

The 7070-313 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.
FlexorSet
Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

➤ GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules. ➤
FlexorSet
Model 7070-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - x8 PCIe

PCI Express Interface
The Model 7070-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources
The 7070-313 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits
4-Channel Digital Downconverter
Decimation Range: 2x to 65,536x in two stages of 2x to 256x
LO Tuning Freq. Resolution: 32 bits, 0 to fs
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit user-programmable coefficients, 24-bit output
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits
DigitalInterpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Total Interpolation Range
D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel connector
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock
External Clock
Type: Front panel female SMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2
Custom FPGA I/O
Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T
Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)
Pentek Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information
Model Description
5973-313 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpolation and Virtex-7 FPGA -x8 PCIe
Options:
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O between the FPGA and a card-edge connector for custom I/O
-110 VITA-66.4 12x optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model Description
8266 PC Development System
See 8266 Datasheet for Options
General Information

The Flexor® Model 3316 is a multi-channel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

When combined with a Pentek 3U VPX or a PCIe FMC carrier, the 3316 is available as a FlexorSet, a complete turnkey data acquisition solution. For applications that require custom processing, FlexorSets are ideal for IP development and deployment.

Pentek also offers the option -990 reference design with software and IP support when installed on the Xilinx VC707 Evaluation Kit board.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3316

The true performance of the 3316 can be best unlocked when used with the Pentek FMC carriers as a FlexorSet. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

A/D Acquisition IP Modules

With the 3316 installed on a Pentek FMC carrier, the FlexorSet features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s task of identifying and executing on the data.

Features

- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Pentek FMC carriers
- Ruggedized and conduction-cooled versions available

New!
When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3316’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows or Linux operating systems.

**Model 3316 Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

**Sample Clock Source:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16

**External Clock**
- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**External Trigger Input**
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Environmental:** Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

**I/O Module Interface:** VITA-57.1, High-Pin-Count FMC
## Pentek FlexorSet Models

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**General Information**

Model 5973-316 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**The Flexor Architecture**

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-316 to operate as a turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The 5973-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSPs/48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

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**Features**

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**New!**
Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.
Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Memory Resources
The 5973-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface
The Model 5973-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model 5973-316 8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

Options:
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O to VPX P2
-110 VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267
VPX Development System
See 8267Datasheet for Options

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
**General Information**

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot. As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

**The Flexor Architecture**

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.
**A/D Acquisition IP Modules**

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8* f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

**A/D Converter Stage**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

**Memory Resources**

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

**PCI Express Interface**

The Model 5983-317 includes an industry-standard interface fully compliant with PCIe Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported.
GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits
Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32,768x in three stages of 32x
LO Tuning Freq. Resolution: 32 bits, 0 to ƒs
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution
Sample Clock Sources: On-board clock synthesizer
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: –20° to 65° C
Storage Temp: –40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: –40° to 70° C
Storage Temp: –50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1
General Information

Model 7070-316 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O. Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on the PCIe slot panel.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. ▶
8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe

Memory Resources

The 7070-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 7070-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel connectors
Transformer Type: CoilCraft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kH to 700 MHz

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the card-edge connector for custom I/O
Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

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General Information

The Flexor® Model 3317 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channel count systems.

The 3317 is sold as a complete turnkey data acquisition solution as the FlexorSet™ 5973-317 3U VPX or the FlexorSet 7070-317 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

The 3317 is identical to the 3316 but with different FPGA functionality since it includes DDCs (digital downconverters) when attached to a 5973 or a 7070 FMC carrier.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3317

The true performance of the 3317 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable DDCs, programmable linked-list DMA engines, and a metadata packet creator.

A/D Acquisition IP Modules

With the 3317 installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s task of identifying and executing on the data.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the FlexorSet to operate as a turnkey solution without the need to develop any FPGA IP.

Features

- Sold as the:
  - FlexorSet Model 5973-317
  - FlexorSet Model 7070-317
- Eight 250 MHz, 16-bit A/Ds
- Eight multiband DDCs
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U VPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available
Model 3317

8-Channel 250 MHz, 16-bit A/D with DDCs - FMC

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized to create larger multiboard systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3317’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973-317 (3U VPX) or 7070-317 (x8 PCIe) IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973-317/7070-317 IP with their own.

FMC Interface

The Model 3317 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3317 and the FMC carrier.

Model 3317 Specifications

Front Panel Analog Signal Inputs

| Input Type: | Transformer-coupled, front panel connectors |
| Transformer Type: | Coil Craft WBC4-6TLB |
| Full Scale Input: | +4 dBm into 50 ohms |
| 3 dB Passband: | 300 kHz to 700 MHz |

A/D Converters

| Type: | Texas Instruments ADS42LB69 |
| Resolution: | 16 bits |

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer

| Clock Source: | Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock |
| Synchronization: | VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz |
| Clock Dividers: | External clock or VCXO can be divided by 1, 2, 4, 8, or 16 |

External Clock

| Type: | Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference |

External Trigger Input

| Type: | Front panel connector |
| Function: | Programmable functions include: trigger, gate, sync and PPS |

Environmental:

Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC
General Information

Model 5973-317 is a member of the Flexor family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 5973-317 includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, it includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Supports Xilinx Virtex-7 VTX FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s/\text{N} \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8\times f_s/\text{N} \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/\text{N} \).

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress\textsuperscript{®}, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed.

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**8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - 3U VPX**

**A/D Acquisition IP Modules**

The 5973-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.
Memory Resources
The 5973-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 5973-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
- Model 5973-317: 8-Channel 250 MHz A/D with DDCs and Virtex-7 FPGA - 3U VPX

Options:
- -104: LVDS FPGA I/O to VPX P2
- -110: VITA-66.4 12X optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Specifications
- A/D Converters
  - Texas Instruments ADS42LB69
  - Sampling Rate: 10 MHz to 250 MHz
  - Resolution: 16 bits
- Front Panel Analog Signal Inputs
  - Type: Transformer-coupled, front panel connectors
  - Transformer Type: CoilCraft WBC4-6TLB
  - Full Scale Input: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

Digital Downconverters
- Quantity: Eight channels
- Decimation Range: 2x to 65,536x in two stages of 2x to 256x
- LO Tuning Freq. Resolution: 32 bits, 0 to f_s
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
- Default Filter Set: Highpass to 300 kHz
- Phase Shift Coefficients: 16-bit resolution

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX690T-2
- Custom FPGA I/O
  - 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
New!

FlexorSet
Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

General Information
Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX base-boards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture
Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.

Features
- VITA-57.4 HSPC FMC+
  - site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB and 5 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-85 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 www.pentek.com Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com
A/D Acquisition IP Modules

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Memory Resources

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported.
FlexorSet
Model 5983-317

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

Digital Downconverters
- **Quantity:** Eight channels
- **Decimation Range:** 2x to 32,768x in three stages of 32x
- **LO Tuning Freq. Resolution:** 32 bits, 0 to $f_s$
- **LO SFDR:** >120 dB
- **Phase Offset Resolution:** 32 bits, 0 to 360 degrees
- **FIR Filter:** 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients:** I & Q with 16-bit resolution
- **Gain Coefficients:** 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- **Type:** Front panel female MMCX connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU060-2
- **Optional:** Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- **Serial:** 4x gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel:** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- **Type:** DDR4 SDRAM
- **Size:** Two banks, one 4 GB and one 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Standard:** L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: −20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - Operating Temp: −20° to 65° C
  - Storage Temp: −40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing
- **Option -763:** L3 (conduction cooled)
  - Operating Temp: −40° to 70° C
  - Storage Temp: −50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1

Contact Pentek for availability of rugged and conduction-cooled versions

Model 5983-317 8-Channel 250 MHz A/D with DDCs and Kintex Ultra Scale FPGA - 3U VPX

Options:
- 087 XCKU115-2 FPGA
- 110 VITA-66.4 12X optical interface
- 180 GPS Support
- 702 Air cooled, Level L2
- 763 Conduction-cooled, Level L3

Model 8267 VPX Development System
See 8267 Datasheet for Options
8-Channel 250 MHz A/D with DDCs, Virtex-7 FPGA - x8 PCIe

General Information

Model 7070-317 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-317 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-317 is populated with a VX690T FPGA. It features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Features

- Supports Xilinx Virtex-7 VXT FPGA
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- Eight multiband DDCs
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCIe Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
www.pentek.com
Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to 1/f_s where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 mSec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed.

**DDC IP Cores**

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all eight DDCs or each of the eight A/Ds driving its own DDC.
Memory Resources

The 7070-317 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 7070-317 includes an industry-standard interface fully compliant with PCI e Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building a development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building a development system that ensures optimum performance of Pentek boards.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Specifications

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel connectors
- **Transformer Type**: CoilCraft WBC4-6TLB
- **Full Scale Input**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz
- **A/D Converters**: Texas Instruments ADS42LB69
- **Sampling Rate**: 10 MHz to 250 MHz
- **Resolution**: 16 bits

Digital Downconverters

- **Quantity**: Eight channels
- **Decimation Range**: 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq. Resolution**: 32 bits, 0 to f_s
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 18-bit coefficients, 24-bit output, user-programmable coefficients
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients**: I & Q with 16-bit resolution
- **Gain Coefficients**: 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

- **Type**: Front panel connector
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard**: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

- **Parallel (Option -104)**: 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110)**: 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory

- **Type**: DDR3 SDRAM
- **Size**: Four banks, 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

PCI-Express Interface

- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8

Environmental

- **Level L1 & L2 air-cooled, Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

The Flexor™ Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

The 3320 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-320 3U VPX or the FlexorSet 7070-320 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Performance of the Model 3320

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

A/D and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

A/D Acquisition IP Modules

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.

Features

- Sold as the:
  - FlexorSet Model 5973-320
  - FlexorSet Model 7070-320
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Ruggedized and conduction-cooled versions available

* See last page for configuration profiles
Model 3320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

➤ **Digital Upconverter and D/A Stage**

Two Texas Instruments DAC39J84 D/As accept two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

**D/A Waveform Playback IP Modules**

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

**Clocking and Synchronization**

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973 or the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the pre-defined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3320’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/320 or 7070/320 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3320 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier. ➤
## Model 3320 Specifications

### Front Panel Analog Signal Inputs

**Input Type:** Transformer-coupled, front panel SSMC connectors  
**Transformer Type:** Mini-Circuits TC1-1-13M  
**Full Scale Input:** +6.6 dBm into 50 ohms  
**3 dB Passband:** 4.5 to 3000 MHz

### A/D Converters

**Type:** Texas Instruments ADC32RF45  
**Sampling Rate and Resolution:** See table below

### Front Panel Analog Signal Outputs

**Output Type:** Transformer-coupled, front panel SSMC connectors  
**Transformer Type:** Coil Craft WBC4-14L  
**Full-Scale Output:** +4 dBm into 50 ohms  
**3 dB Passband:** 1.5 MHz to 1200 MHz

### D/A Converters

**Type:** Texas Instruments DAC39J84  
**Sampling Rate and Resolution:** See table below

### Sample Clock Sources

Timing bus generator provides A/D and D/A clocks

### Timing Bus Generator

**Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock  
**Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

### External Clock

**Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

### External Trigger Input

**Type:** Front panel SSMC connector  
**Function:** Programmable functions include: trigger, gate, sync and PPS

### Environmental

**Level L1 & L2** air-cooled, **Level L3** conduction-cooled, ruggedized  
**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

### Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>Converter Sample Rate</th>
<th>A/D Converter</th>
<th>D/A Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output Resolution</td>
<td>Decimation</td>
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<tr>
<td>3.0 GHz</td>
<td>16 bit</td>
<td>4</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
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<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
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</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
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<td>14 bit</td>
<td>bypass</td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user  
** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

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### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5973-320</td>
<td>2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- -076 XC7VX690T-2 FPGA  
- -104 LVDS FPGA I/O to VPX P2  
- -110 VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8267</td>
<td>VPX Development System See 8267 Datasheet for Options</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-320</td>
<td>2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- -076 XC7VX690T-2 FPGA  
- -104 LVDS FPGA I/O to card-edge connector  
- -110 VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>

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Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

General Information

Model 5973-320 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-320 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back the D/A waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.
A/D Acquisition IP Modules

The 5973-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator, or from the two D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 5973-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 5973-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

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A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Coil Craft WBC4-14L
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **4x gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;

Environmental
- **Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5973-320</td>
<td>2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A wth Virtex-7 - 3U VPX</td>
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</tbody>
</table>

Options:
- **-076:** XC7VX690T-2 FPGA
- **-104:** LVDS FPGA I/O to VPX P2
- **-110:** VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>Converter</th>
<th>A/D Converter</th>
<th>D/A Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate</td>
<td>Output Resolution</td>
<td>Decimation</td>
</tr>
<tr>
<td>3.0 GHz</td>
<td>16 bit</td>
<td>4</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
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<td>14 bit</td>
<td>bypass</td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user
** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer
**General Information**

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-320 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor© FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

**The Flexor Architecture**

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-320 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-320 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP.
**A/D Acquisition IP Modules**

The 5983-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Generator IP Modules**

The 5983-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

**Memory Resources**

The 5983-320 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

**PCI Express Interface**

The Model 5983-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**A/D Converter and Digital Downconverter Stage**

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the next page for supported modes. 

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**Xilinx Kintex UltraScale FPGA**

The 5983-320 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.
GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Digital Upconverter and D/A Stage
A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel SSMC connectors
- Transformer Type: Mini-Circuit TC1-1-13M
- Full Scale Input: +6.6 dBm into 50 ohms
- 3 dB Passband: 4.5 to 3000 MHz

A/D Converters
- Type: Texas Instruments ADC32RF45
- Sampling Rate and Resolution: See the 3320 preconfigured modes table

Front Panel Analog Signal Outputs
- Output Type: Transformer-coupled, front panel SSMC connectors
- Transformer Type: Coil Craft WBC4-14L
- Full-Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
- Type: Texas Instruments DAC39J84
- Sampling Rate and Resolution: See the 3320 preconfigured modes table

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
- Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- Type: Front panel SSMC connector
- Function: Programmable functions include: trigger, gate, sync and PPS

➤
FlexorSet
Model 5983-320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

- Field Programmable Gate Array
  - Standard: Xilinx Kintex UltraScale XCKU060-2
  - Optional: Xilinx Kintex UltraScale XCKU115-2

- Custom FPGA I/O
  - Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
  - Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
  - Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- Type: DDR4 SDRAM
- Size: Two banks, one 4 GB and one 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCIe Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
- Standard: L0 (air cooled)
  - Operating Temp: 0° to 50° C
  - Storage Temp: –20° to 90° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -702: L2 (air cooled)
  - Operating Temp: –20° to 65° C
  - Storage Temp: –40° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

- Option -763: L3 (conduction cooled)
  - Operating Temp: –40° to 70° C
  - Storage Temp: –50° to 100° C
  - Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility:
The Model 5983-320 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:

SLT3-PAY-2F1F2U1E-14.6.6-1

SPARK Development Systems
The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
--- | ---
5983-320 | 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX

Options:
-087 | XCKU115-2 FPGA
-110 | VITA-66.4 12X optical interface
-180 | GPS Support
-702 | Air cooled, Level L2
-763 | Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model | Description
--- | ---
8267 | VPX Development System

See 8267 Datasheet for Options

SPARK Development Systems

The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A with Virtex-7 - x8 PCIe

**General Information**

Model 7070-320 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**The Flexor Architecture**

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-320 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

**Features**

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

*See last page for configuration profiles
A/D Acquisition IP Modules

The 7070-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator, or from data from any of the two A/Ds, in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources

The 7070-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface

The Model 7070-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

Digital Upconverter and D/A Stage

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.
Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SS/MC connectors
- **Transformer Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel SS/MC connectors
- **Transformer Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference
- **External Clock:**
  - **Type:** Front panel SS/MC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
- **External Trigger Input:**
  - **Type:** Front panel SS/MC connector
  - **Function:** Programmable functions include: trigger, gate, sync and PPS
- **Field Programmable Gate Array**
  - **Standard:** Xilinx Virtex-7 XC7VX330T-2
  - **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8;
- **Environmental:** Level L1 & L2 air-cooled
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>A/D Converter</th>
<th>D/A Converter</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Converter</strong></td>
<td><strong>Output Data Rate</strong></td>
</tr>
<tr>
<td>Sample Rate</td>
<td>Resolution</td>
</tr>
<tr>
<td>3.0 GHz</td>
<td>16 bit</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user
** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-320</td>
<td>2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- **-076:** XC7VX690T-2 FPGA
- **-104:** LVDS FPGA I/O to card-edge connector
- **-110:** VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
General Information

The Flexor® Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3324 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet® 5973-324 3U VPX or the FlexorSet 7070-324 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

Performance of the Model 3324

The true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3324 installed on either the 5973 or the 7070, the 3324 features four sophisticated A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

With the 5973 or the 7070, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

Features

- Sold as the:
  - FlexorSet Model 5973-324
  - FlexorSet Model 7070-324
- Four 500 MHz, 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz, 16-bit D/As (500 MHz input data rate, 2 GHz output sample rate with interpolation)
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx, and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 8267**

The Model 8267 is a VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Digital Upconverters and D/As**

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconverter, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 1.5 GHz. In both modes the D/A provide interpolation factors of 2x, 4x, 8x and 16x.

**Clocking and Synchronization**

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized and create larger multiboard systems.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3324’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful tool to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3324 or 7070/3324 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3324 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3324 and the FMC carrier.

**Model 3324 Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBCI-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** up to 500 MHz
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**

- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**D/A Converters**

- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

**Sample Clock Source:** On-board clock synthesizer

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D and D/A clocks

**External Clock**

- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**External Trigger Input**

- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Environmental**

- **Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized FMC**

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**Model 3324**

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A-FMC
General Information

Model 5973-324 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3324 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen.3 as a native interface, the Model 5973-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-324 to operate as a turnkey solution without the need to develop any FPGA IP.
A/D Acquisition IP Modules

The 5973-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of the transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-324 factory-installed functions include four sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extensible IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4x connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. ➤
cession of Pentek boards. It was developed to save engineers and system integrators the time and expense associated with building a custom development system.

Memory Resources

The 5973-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8267

The Model 8267 features a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8267-076</td>
<td>4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-6 FPGA - 3U VPX</td>
</tr>
<tr>
<td>8267-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td>8267-110</td>
<td>VITA-66.4 12X optical interface</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel clock connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator. A front panel LVTTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs

<table>
<thead>
<tr>
<th>Input Type</th>
<th>Transformer-coupled, front panel connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer Type</td>
<td>Coil Craft WBC1-1TBL</td>
</tr>
</tbody>
</table>

Full Scale Input: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 750 MHz

A/D Converters

<table>
<thead>
<tr>
<th>Type</th>
<th>Texas Instruments ADS54760</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>Up to 500 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

Front Panel Analog Signal Outputs

<table>
<thead>
<tr>
<th>Output Type</th>
<th>Transformer-coupled, front panel connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer Type</td>
<td>Coil Craft WBC4-6TLB</td>
</tr>
</tbody>
</table>

Full-Scale Output: +4 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

D/A Converters

<table>
<thead>
<tr>
<th>Type</th>
<th>Texas Instruments DAC38J84</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Data Rate</td>
<td>Up to 500 MHz</td>
</tr>
<tr>
<td>Output Sample Rate</td>
<td>Up to 2 GHz (with interpolation)</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

Sample Clock Sources: On-board clock generator provides two clocks: an A/D clock and a D/A clock.

Clock Synthesizer

<table>
<thead>
<tr>
<th>Clock Source</th>
<th>Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Synchronization</td>
<td>VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz</td>
</tr>
<tr>
<td>Clock Dividers</td>
<td>External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks</td>
</tr>
</tbody>
</table>

External Clock

<table>
<thead>
<tr>
<th>Type</th>
<th>Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function</td>
<td>Front panel connector</td>
</tr>
<tr>
<td>Field Programmable Gate Array</td>
<td>Programmable functions include: trigger, gate, sync and PPS</td>
</tr>
</tbody>
</table>

Custom FPGA I/O

<table>
<thead>
<tr>
<th>Option</th>
<th>Xilinx Virtex-7 XC7VX690T-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>Xilinx Virtex-7 XC7VX330T-2</td>
</tr>
<tr>
<td>Option-076</td>
<td>Xilinx Virtex-7 XC7VX690T-2</td>
</tr>
</tbody>
</table>

Memory

<table>
<thead>
<tr>
<th>Type</th>
<th>DDR3 SDRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>Four banks, 1 GB each</td>
</tr>
<tr>
<td>Speed</td>
<td>800 MHz (1600 MHz DDR)</td>
</tr>
</tbody>
</table>

PCI-Express Interface

<table>
<thead>
<tr>
<th>PCI Express Bus</th>
<th>Gen. 1, 2 or 3: x4 or x8;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Environmental</td>
<td>Level L1 &amp; L2 air-cooled,</td>
</tr>
<tr>
<td></td>
<td>Level L3 conduction-cooled,</td>
</tr>
<tr>
<td></td>
<td>ruggedized</td>
</tr>
<tr>
<td>Size</td>
<td>3.937 in. x 6.717 in. (100 mm x 170.6 mm)</td>
</tr>
</tbody>
</table>

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
**General Information**

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-324 FlexorSet™ combines the Model 5983 and the Model 3324 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances.

**The Flexor Architecture**

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-324 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.
A/D Acquisition IP Modules
The 5983-324 features four A/D Acquisition IP Modules for easy capture and data movement. Each IP module can receive data from any of the four A/Ds, a test signal generator, or from the four D/A Waveform Recorder IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Recorder IP Modules
The 5983-324 factory-installed functions include four sophisticated D/A Waveform Recorder IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design
For applications that require specialized functions, users can install their own custom FPGA IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA
The 5983-324 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a PCIe connection is supported between the FPGA and the VPX connector to supply those signals with a programmable interface.

Memory Resources
The 5983-324 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 5983-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Downconverter
The front end accepts four analog RF or IF inputs on front-panel connectors with transformer-coupling into Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

Digital Upconverter and D/A
Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. ➤
GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

Specifications
FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A Kintex UltraScale FPGA - 3U VPX

- External Clock
  Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- External Trigger Input
  Type: Front panel connector
  Function: Programmable functions include: trigger, gate, sync and PPS

- Field Programmable Gate Array
  Standard: Xilinx Kintex UltraScale XCKU060-2
  Optional: Xilinx Kintex UltraScale XCKU115-2

- Custom FPGA I/O
  Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
  Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

- Optical (Option -110): VITA-66.4, 12X duplex lanes

- Memory
  Type: DDR4 SDRAM
  Size: Two banks, one 4 GB and one 5 GB
  Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
  Operating Temp: 0° to 50° C
  Storage Temp: -20° to 90° C
  Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
  Operating Temp: -20° to 65° C
  Storage Temp: -40° to 100° C
  Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
  Operating Temp: -40° to 70° C
  Storage Temp: -50° to 100° C
  Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-324 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

SPARK Development Systems
The Model 8267 is a fully-integrated development system for Pentek 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model  Description
5983-324 4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Kintex UltraScale FPGA - 3U VPX

Options:
-087  XCKU115-2 FPGA
-110  VITA-66.4 12X optical interface
-180  GPS Support
-702  Air cooled, Level L2
-763  Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model  Description
8267  VPX Development System
      See 8267 Datasheet for Options

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
General Information

Model 7070-324 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 324 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HP or IP ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, two 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their custom
A/D Acquisition IP Modules

The 7070-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Modules in loopback mode.

Each IP module has an associated memory bank for buffering data into FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-324 factory-installed functions include four sophisticated D/A Waveform Playback IP Modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space.
**PCI Express Interface**

The Model 7070-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 7070-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-324</td>
<td>4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>-076</td>
<td>4x w. XC7VX690T-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to card-edge connector</td>
</tr>
<tr>
<td>-110</td>
<td>12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T</td>
</tr>
</tbody>
</table>

**Specifications**

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel connectors
- **Transformer Type**: Coil Craft WBC1-1TLB
- **Full-Scale Input**: +4 dBm into 50 ohms
- **Passband**: 300 kHz to 750 MHz
- **Output Sample Rate**: Up to 2 GHz
- **Resolution**: 16 bits

Front Panel Digital Signal Outputs

- **Output Type**: Transformer-coupled, front panel connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full-Scale Output**: +4 dBm into 50 ohms
- **Passband**: 300 kHz to 700 MHz
- **Resolution**: 16 bits

Clocking and Synchronization

- **Sample Clock Sources**: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock
- **Clock Synthesizer**
  - **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

A/D Converters

- **Type**: Texas Instruments ADS54J60
- **Sampling Rate**: Up to 500 MHz
- **Resolution**: 16 bits

D/A Converters

- **Type**: Texas Instruments DAC38J84
- **Input Data Rate**: Up to 500 MHz
- **Output Sample Rate**: Up to 2 GHz (with interpolation)
- **Resolution**: 16 bits

**Field Programmable Gate Array**

- **Standard**: Xilinx Virtex-7 XC7VX330T-2
- **Option -076**: Xilinx Virtex-7 XC7VX690T-2

**Custom FPGA I/O**

- **Parallel Option -104**: 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical Option -110**: 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

**Memory**

- **Type**: DDR3 SDRAM
- **Size**: Four banks, 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

**PCI-Express Interface**

- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8
- **Environmental**: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
Model 8266 PC Development System for PCIe Cobalt, Onyx and Flexor Boards

General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx® and Flexor™ PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19” 4U rackmount chassis that is 21” deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux

Processor: Intel® Core™ i7 3.6 GHz

Clock Speed: 3.6 GHz

SDRAM: 16 GB standard

Dimensions: 4U Chassis, 19” W x 21” D x 7” H

Weight: 35 lb, approx.

Operating Temp: 0° to +50° C

Storage Temp: -40° to +85° C

Relative Humidity: 5 to 95%, non-condensing

Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Features

- 4U 19-inch rackmount PC server chassis, 21-inch deep
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 16 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box test examples

Ordering Information

Model 8266 Description
8266 PC Development System for PCIe Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.
Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

General Information

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19” 4U rackmount chassis that is 12” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and extended memory support.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB standard
Dimensions: 4U Chassis, 19” W x 12” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model Description
8267 3U VPX Development System for Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS
-101 Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
Pentek offers the option -990 reference design with software and IP support for the Pentek Model 3312 when installed on the Xilinx VC707 Evaluation Kit board.

The Virtex®-7 FPGA VC707 Evaluation Kit is a PCIe platform using the Virtex-7 XC7VX485T-2FFG1761C. It includes basic components of hardware, design tools, IP, and preverified reference designs.

When coupled with Pentek’s option -990 reference design for the 3312, the user has a complete development environment for custom applications. The industry-standard FPGA Mezzanine Connectors (FMC) are directly compatible with the 3312.

Features

- Supports the Xilinx Virtex-7 FPGA
- Complete development environment with Pentek’s reference design
- Supports the Pentek Model 3312 FMC I/O Module

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tr>
<td>3312-990</td>
<td>Reference Design for the Xilinx VC707 Evaluation Kit</td>
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</table>


The Xilinx Virtex®-7 FPGA VC707 Evaluation Kit gives designers an easy starting point for evaluating and leveraging devices that deliver breakthrough performance, capacity, and power efficiency. Out of the box, this platform speeds time to market for the full-range of Virtex-7 FPGA-based applications including advanced systems for wired and wireless communications, aerospace, and defense. The highly flexible kit combines fully integrated hardware, software, and IP with preverified reference designs that maximize productivity and let designers immediately focus on their unique project requirements.

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We're glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

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Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

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Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

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You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at:

Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900 • fax: 201-818-5697 • email: custsvc@pentek.com

www.pentek.com
**MODEL**

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<td>Jade 78141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - x8 PCIe</td>
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<td>Jade 53141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - 3U VPX</td>
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**Customer Information**
**General Information**

Model 71663 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 71663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**GSM Channelizer Cores**

The 71663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
Model 71663

1100-Channel GSM Channelizer with Quad A/D - XMC

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 71663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 71663 and host.

➤

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 71663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 71663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.
1100-Channel GSM Channelizer with Quad A/D - XMC

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
- Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks

DDC Channels
- Channel Spacing: 200 kHz, fixed
- DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
- < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
- > 18 dB attenuation at ±100 kHz
- > 78 dB attenuation at ±170 kHz
- > 83 dB attenuation at ±600 kHz
- > 93 dB attenuation at ±800 kHz
- > 96 dB attenuation at > ±3 MHz

DDC Output Rate f_s: Resampled to 180 MHz * 13/2160 = 1.083333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
- Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
- Frequency Offsets for each DDC:
  - First: -f_s/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +f_s/4 (+270.8333 kHz)
  - Fourth: +f_s/2 (+541.666 kHz)

Superchannel Sample Rate: f_s

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- PCI Express Bus: Gen. 2 x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com www.pentek.com
Model 78663 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 78663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 78663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCIe Express Gen. 2 x8
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 78663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 78663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 78663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 78663 and host.
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- **DDCs per bank:** two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank:** 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

DDC Channels
- **Channel Spacing:** 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
- < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
- > 18 dB attenuation at ±100 kHz
- > 78 dB attenuation at ±170 kHz
- > 83 dB attenuation at ±600 kHz
- > 93 dB attenuation at ±800 kHz
- > 96 dB attenuation at > ±3 MHz

DDC Output Rate \( f_s \) Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: \(-f_s/4\) (-270.8333 kHz)
  - Second: 0 Hz
  - Third: \(+f_s/4\) (+270.8333 kHz)
  - Fourth: \(+f_s/2\) (+541.666 kHz)
- **Superchannel Sample Rate:** \( f_s \)

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6SVX315T

PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 x 7.13 in.
General Information

Model 53663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 53663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 53663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers. ➤
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 53663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 53663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 53663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 53663 and host.

Fabric-Transparent Crossbar Switch

The 53663 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks

DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq + k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics:
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 KHz
> 96 dB attenuation at ±3 MHz

DDC Output Rate \( f_s \): Resampled to 180 MHz/13/260 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
Frequency Offsets for each DDC:
First: \(-\frac{f_s}{4} \) (-270.8333 kHz)
Second: 0 Hz
Third: \(\frac{f_s}{4} \) (+270.8333 kHz)
Fourth: \(\frac{f_s}{2} \) (+541.666 kHz)

Superchannel Sample Rate: \( f_s \)
Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank: 175-channel banks: 44; 375-channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: 3357 in. x 6717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

### VPX Family Comparison

<table>
<thead>
<tr>
<th></th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x4 or x8</td>
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<tr>
<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
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<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Ordering Information

Model 53663
1100-Channel GSM Channelizer with Quad A/D - VPX

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267
VPX Development System. See 8267 Datasheet for Options
1100-Channel GSM Channelizer with Quad A/D - VPX

General Information

Model 52663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 2 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 52663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores

The 52663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 52663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 52663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 2 GB/sec peak rate of PCIe Gen 2 x4 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is slightly above the capability of the PCIe Gen 2 x4 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 52663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x4, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 52663 and host.
1100-Channel GSM Channelizer with Quad A/D - VPX

Specifications

Front Panel Analog Signal Inputs
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +8 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
  - Type: Texas Instruments ADS5485
  - Sampling Rate: 10 MHz to 200 MHz
  - Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
  - Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
  - DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
  - Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
  - IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
  - Channel Spacing: 200 kHz, fixed
  - DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics:
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 kHz
  - > 96 dB attenuation at ±800 kHz

DDC Output Rate $f_s$: Resampled to 180 MHz/13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
  - Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
  - Frequency Offsets for each DDC:
    - First: $-f_s/4$ (-270.8333 kHz)
    - Second: 0 Hz
    - Third: $+f_s/4$ (+270.8333 kHz)
    - Fourth: $+f_s/2$ (+541.666 kHz)
  - Superchannel Sample Rate: $f_s$
  - Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
  - 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
  - PCI Express Bus: Gen. 2 x8

Environmental
  - Operating Temp: 0° to 50° C
  - Storage Temp: –20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td>Lowest Price</td>
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</table>

Ordering Information

Model: 52663
Description: 1100-Channel GSM Channelizer with Quad A/D - VPX

Model: 8267
Description: VPX Development System. See 8267 Datasheet for Options
New! New! New! New! New!

Models 57663 & 58663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - 6U OpenVPX

General Information
Models 57663 and 58663 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a VPX carrier board.

Model 57663 is a 6U board with one Model 71663 module while the Model 58663 is a 6U board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture
The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

A/D Converter Stage
The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization
The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Features
- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- PCIe Express (Gen. 1 & 2) interface up to x4
- LVPECL clock/sync bus for multiboard synchronization
- Ruggedized and conduction-cooled versions available

Block Diagram, Model 57663.
Model 58663 doubles all resources except the PCIe-to-PCIe Switch

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
www.pentek.com
GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz/10/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.
### Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Specifications

**Model 57663**: 4 A/Ds, 1100 Channels  
**Model 58663**: 8 A/Ds, 2200 Channels  
**Front Panel Analog Signal Inputs (4 or 8)**  
- **Input Type**: Transformer-coupled, front panel female SSMC connectors  
- **Transformer Type**: Coil Craft WBC4-6TLB  
- **Full Scale Input**: +8 dBm into 50 ohms  
- **3 dB Passband**: 300 kHz to 700 MHz  
**A/D Converters (4 or 8)**  
- **Type**: Texas Instruments ADS5485  
- **Sampling Rate**: 10 MHz to 200 MHz  
- **Resolution**: 16 bits  
**Sample Clock Sources (1 or 2)**  
- **Clock Synthesizers (1 or 2)**  
- **Clock Source**: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus  
- **Synchronization**: VCXO can be locked to an external 10 MHz system reference  
**External Clocks (1 or 2)**  
- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference  
**Timing Bus (1 or 2)**: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs  
**External Trigger Inputs (1 or 2)**  
- **Type**: Front panel female SSMC connector, LVTTL  
- **Function**: Programmable functions include: trigger, gate, sync and PPS  
**GSM Channel Banks (1 or 2)**  
- **DDC Channels**: 200 kHz, fixed  
- **Channel Spacing**: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187  
- **DDC Center Freqs**: 45, 135 or 225 MHz  
- **IF (Center) Freq**: ± 20 kHz  
- **DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.083333 MS/sec  
- **DDC Data Output Format**: 24 bits I + 24 bits Q  
**Superchannels**  
- **Content**: Four consecutive DDC channels are frequency-offset from each other and then summed together  
- **Frequency Offsets for each DDC**: First: -f_s/4 (-270.8333 kHz)  
  Second: 0 Hz  
  Third: +f_s/4 (+270.8333 kHz)  
  Fourth: +f_s/2 (+541.666 kHz)  
- **Superchannel Sample Rate**: f_s  
- **Superchannel Output Format**: 26 bits I + 26 bits Q  
**Number of Superchannels per Bank**:  
- 175-Channel banks: 44; 375-Channel banks: 94  
**Field Programmable Gate Arrays (1 or 2)**  
- **Xilinx Virtex-6 XC6VSX315T**  
**PCI-Express Interface**  
- **PCI Express Bus**: Gen. 1 or 2; x4  
**Environmental**  
- **Level L1 & L2 air-cooled**  
- **Level L3 ruggedized, conduction-cooled**  
**Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>57663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 6U VPX</td>
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<tr>
<td>58663</td>
<td>2200-Channel GSM Channelizer with Octal A/D - 6U VPX</td>
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</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

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**Seat-Express Development Systems**

### Pentek, Inc.

One Park Way  ●  Upper Saddle River  ●  New Jersey 07458  
Tel: 201-818-5900  ●  Fax: 201-818-5904  ●  Email: info@pentek.com  
www.pentek.com
Models 72663, 73663 and 74663

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

General Information
Models 72663, 73663 and 74663 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a cPCI carrier board.

Model 72663 is a 6U cPCI board while the Model 73663 is a 3U cPCI board; both are equipped with one Model 71663 XMC. Model 74663 is a 6U cPCI board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture
The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

A/D Converter Stage
The front end accepts four or eight analog IF inputs on front panel SSMC connectors. This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

Clocking and Synchronization
The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz. The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Features
- Complete GSM channelizer with analog IF interface
- Four or eight 180 MHz 16-bit A/Ds
- Two or four banks of 375 DDCs for upper GSM band
- Two or four banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization

Block Diagram, Model 72663
Model 74663 doubles all resources except the PCI-to-PCI Bridge

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-9904 • Email: info@pentek.com

www.pentek.com
GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73663: 32 bits only.

The PCI-X interface is also used as the programming interface for all status and control between these models and host.
Specifications

Model 72663 or Model 73663: 4 A/Ds
Model 74663: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +8 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
  - Type: Texas Instruments ADS5485
  - Sampling Rate: 10 MHz to 200 MHz
  - Resolution: 16 bits

Sample Clock Sources (1 or 2)
  - On-board clock synthesizer

Clock Synthesizers (1 or 2)
  - Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clocks (1 or 2)
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks (1 or 2)
  - DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
  - Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
  - IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
  - Channel Spacing: 200 kHz, fixed
  - DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
  - DDC Channel Filter Characteristics
    - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
    - > 18 dB attenuation at ±100 kHz
    - > 78 dB attenuation at ±170 kHz
    - > 83 dB attenuation at ±600 kHz
    - > 93 dB attenuation at ±800 KHz
    - > 96 dB attenuation at > ±3 MHz
  - DDC Output Rate $f_s$: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec
  - DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
  - Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
  - Frequency Offsets for each DDC:
    - First: $-f_s/4$ (-270.8333 kHz)
    - Second: 0 Hz
    - Third: $+f_s/4$ (+270.8333 kHz)
    - Fourth: $+f_s/2$ (+541.666 kHz)
  - Superchannel Sample Rate: $f_s$
  - Superchannel Output Format: 26 bits I + 26 bits Q
  - Number of Superchannels per Bank:
    - 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Arrays (1 or 2)
  - Xilinx Virtex-6 XC6VSX315T

PCI-X Interface
  - PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
  - Model 73663: 32 bits only

Environmental
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.

Size:
  - Standard 6U or 3U cPCI board

Ordering Information

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**General Information**

Model 56663 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 56663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

**GSM Channelizer Cores**

The 56663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

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**Features**

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express Gen. 2 x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 56663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 56663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz×13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 56663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 56663 and host.

AMC Interface

The Model 56663 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
- DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
- Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
- IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
- Channel Spacing: 200 kHz, fixed
- DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
- < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
- > 18 dB attenuation at ±100 kHz
- > 78 dB attenuation at ±170 kHz
- > 83 dB attenuation at ±600 kHz
- > 93 dB attenuation at ±800 kHz
- > 96 dB attenuation at > ±3 MHz

DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
- Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:
- First: -f_s/4 (-270.8333 kHz)
- Second: 0 Hz
- Third: +f_s/4 (+270.8333 kHz)
- Fourth: +f_s/2 (+541.666 kHz)

Superchannel Sample Rate: f_s

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
- 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- PCI Express Bus: Gen. 2 x8

AMC Interface
- Type: AMC.1
- Module Management: IPMI Version 2.0

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model 56663 1100-Channel GSM Channelizer with Quad A/D - AMC

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
LVDS Digital I/O with Virtex-6 FPGA - XMC

General Information

Model 71610 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O to the carrier board.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
LVDS Digital I/O with Virtex-6 FPGA - XMC

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Options:
- * This option is always required
- **-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-105 Gigabit serial FPGA I/O through P16 connector
- **-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

**-104 LVDS FPGA I/O through P14 connector

Ordering Information

Model Description
- 71610 LVDS Digital I/O with Virtex-6 FPGA - XMC

Options:
- -062 XC6VLX240T
- -064 XC6VSX315T
- -104 LVDS FPGA I/O through P14 connector
- -105 Gigabit serial FPGA I/O through P16 connector
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

PCI Express Interface

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Memory Resources

The 71610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2). In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

Specifications

Front Panel Input/Output
- Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- Clock: One LVDS differential pair, 2.5 V compliant
- Data Valid: One LVDS differential pair, 2.5 V compliant
- Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 78610 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 78610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 78610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCIe Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

**Model 78610**

LVDS Digital I/O with Virtex-6 FPGA - x8 PCIe

**Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 78610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**PCI Express Interface**

The Model 78610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 78610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

### Specifications

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Half-length PCIe card, 4.38 in. x 7.13 in.

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**Model Ordering Information**

**Model Description**

- **78610** LVDS Digital I/O with Virtex-6 FPGA - PCIe
- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**SPARK Development Systems**

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**Pentek, Inc.** One Park Way • Upper Saddle River • New Jersey 07458

Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 53610 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 53610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 53610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

Fabric-Transparent Crossbar Switch

The 53610 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output preemphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model Description
53610 LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T
-064 XC6VSX315T
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Acquisition IP Module

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 53610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Module

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

PCI Express Interface

The Model 53610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 53610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

Specifications

Front Panel Input/Output

Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
Clock: One LVDS differential pair, 2.5 V compliant
Data Valid: One LVDS differential pair, 2.5 V compliant
Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCIE-Express Interface

PCI Express Bus: Gen. 1: x4 or x8

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>Yes</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
Model 52610 LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

**General Information**

Model 52610 is a member of the Cobalt® family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 52610 includes a general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 52610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

**Features**

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

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**Diagram:**

- **80-pin Front Panel Connector**
  - 32 Pairs LVDS Data
  - LVDS Clock
  - Data Valid
  - Data Suspend

- **VIRTEx-6 FPGA**
  - LX130T, LX240T or SX315T

- **Memory Banks:**
  - Memory Banks 1 & 2
  - Memory Banks 3 & 4
  - Option 105

- **Option -104**
  - 4X4X4X PCIe
  - 4X Gigabit Serial I/O

- **Option -105**
  - 4X PCIe

---

**Model 52610 COTS (left) and rugged version**
LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model Description</th>
<th>Options:</th>
</tr>
</thead>
<tbody>
<tr>
<td>52610 LVDS Digital I/O with Virtex-6 FPGA - 3U VPX</td>
<td>-062 XC6VLX240T</td>
</tr>
<tr>
<td></td>
<td>-064 XC6VLX315T</td>
</tr>
<tr>
<td></td>
<td>-104 LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td></td>
<td>-105 Gigabit serial FPGA I/O to VPX P1</td>
</tr>
<tr>
<td></td>
<td>-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td></td>
<td>-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 52610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**PCI Express Interface**

The Model 52610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 52610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

**Specifications**

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VX315T

**Custom I/O**

- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 16:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<td><strong>Crossbar Switch</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
<td>20 pairs on VPX P2</td>
<td>35 pairs on VPX P2</td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
Single or Dual LVDS Digital I/O with Virtex-6 FPGA - 6U OpenVPX

**Models 57610 and 58610**

**General Information**

Models 57610 and 58610 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71610 XMC modules mounted on a VPX carrier board.

Model 57610 is a 6U board with one Model 71610 module while the Model 58610 is a 6U board with two XMC modules rather than one.

These models include one or two general-purpose connectors for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The factory-installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, controllers for all data clocking, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58610.

**Features**

- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- Ruggedized and conduction-cooled versions available

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**New! New! New! New! New!**

- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- Ruggedized and conduction-cooled versions available
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57610</td>
<td>Single LVDS Digital I/O with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58610</td>
<td>Dual LVDS Digital I/O with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:

-062 XC6VLX240T
-064 XC6VSX315T
-104 LVDS I/O between the FPGA and P3 connector, Model 57610; P3 and P5 connectors, Model 58610
-105 Gigabit link between the FPGA and P2 connector, Model 57610; gigabit links from each FPGA to P2 connector, Model 78610
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

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**Acquisition IP Modules**

These models can be configured for digital input mode by the setting of one or two jumpers. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that these models are no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Modules**

These models can be configured for digital output mode by the setting of one or two jumpers. In this case, the board generates output data Clock and output data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

One or two linked-list controllers allow users to generate 32-bit digital words output through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table generation, etc. can be programmed for entry. Up to 64 or 128 individual link entries can be chained together to create complex output patterns with minimum programming.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The hardware architecture supports up to four or eight independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 4 GB.

**Specifications**

Model 57610: Single LVDS Digital I/O
Model 58610: Dual LVDS Digital I/O

**Front Panel Input/Output (1 or 2)**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array (1 or 2)**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58610

**Memory Banks (1 or 2)**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI Express Interface**

- **PCI Express Bus:** Gen. 1 or 2: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information
Models 72610, 73610 and 74610 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71610 XMC modules mounted on a cPCI carrier board.

Model 72610 is a 6U cPCI board while the Model 73610 is a 3U cPCI board; both are equipped with one Model 71610 XMC. Model 74610 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two general-purpose connectors for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The factory-installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, controllers for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610.

Features
- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3 SDRAM
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board

Block Diagram, Model 72610
Model 74610 doubles all resources except the PCI-to-PCI Bridge

<table>
<thead>
<tr>
<th>VIRTEX-6 FPGA</th>
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<tbody>
<tr>
<td>LX130T, LX240T, or SX315T</td>
</tr>
<tr>
<td>SXT up to 1344 DSP48E slices</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MEMORY BANKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x 512 MB DDR3 SDRAM</td>
</tr>
<tr>
<td>1x 32 MB CARBON FLASH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Optional FPGA I/O (Option -104)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe to XMC Bridge</td>
</tr>
<tr>
<td>PCIe V.1.1 to V.1.0 Bridge</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>80-pin Front Panel Connector</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 LVDS Data</td>
</tr>
<tr>
<td>16 Data Valid</td>
</tr>
<tr>
<td>16 Data Suspend</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>PCIe Board Support Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS Clock</td>
</tr>
<tr>
<td>LVDS Data</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MEMORY BANKS 1 &amp; 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2x 512 MB DDR3 SDRAM</td>
</tr>
<tr>
<td>1x 32 MB CARBON FLASH</td>
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</tbody>
</table>

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<th>Optional FPGA I/O (Option -104)</th>
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<tr>
<td>PCIe to XMC Bridge</td>
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<td>PCIe V.1.1 to V.1.0 Bridge</td>
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</table>

<table>
<thead>
<tr>
<th>From/To Other XMC Module of MODEL 74610</th>
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</thead>
<tbody>
<tr>
<td>PCIe V.1.1 to V.1.0 Bridge</td>
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<table>
<thead>
<tr>
<th>PCIe Board Support Package</th>
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<tbody>
<tr>
<td>LVDS Clock</td>
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<tr>
<td>LVDS Data</td>
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</tbody>
</table>

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458 Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com www.pentek.com
## Single or Dual LVDS Digital I/O with Virtex-6 FPGA - cPCI

### Acquisition IP Module

These models can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that these models are no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

### Generation IP Module

These models can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data. A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

### PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73610: 32 bits only.

### Memory Resources

The hardware architecture supports up to four or eight independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2). In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM for Models 72610 and 73610 or a total of 4 GB for Model 74610.

### Specifications

**Model 72610 or Model 73610: Single LVDS Digital I/O**

**Model 74610: Dual LVDS Digital I/O**

<table>
<thead>
<tr>
<th>Front Panel Input/Output (1 or 2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant</td>
</tr>
<tr>
<td>Clock: One LVDS differential pair, 2.5 V compliant</td>
</tr>
<tr>
<td>Data Valid: One LVDS differential pair, 2.5 V compliant</td>
</tr>
<tr>
<td>Data Suspend: One LVDS differential pair, 2.5 V compliant</td>
</tr>
</tbody>
</table>

### Field Programmable Gate Array (1 or 2)

**Standard:** Xilinx Virtex-6 XC6VLX130T

**Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

### Custom I/O

**Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector,** Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610

### Memory Banks (1 or 2)

**Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR

**Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

### Environmental

**Operating Temp:** 0° to 50° C

**Storage Temp:** –20° to 90° C

**Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard 6U or 3U cPCI board

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**Ordering Information**

**Model Description**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>72610</td>
<td>Single LVDS Digital I/O with Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73610</td>
<td>Single LVDS Digital I/O with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74610</td>
<td>Dual LVDS Digital I/O with Virtex-6 FGPA - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**

- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS I/O between the FPGA and J2 connector, Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610
- 155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

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**Pentek, Inc.**
One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201 818-5900 ● Fax: 201 818-5904 ● Email: info@pentek.com

www.pentek.com
LVDS Digital I/O with Virtex-6 FPGA - AMC

General Information
Model 56610 is a member of the Cobalt® family of high-performance AMC boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 56610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 56610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features
- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
**Model 56610**

**LVDS Digital I/O with Virtex-6 FPGA - AMC**

➤ **Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 56610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**AMC Interface**

The Model 56610 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56610 includes an industry-standard interface fully compliant with PCIe Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 56610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

**Specifications**

**Front Panel Input/Output**

- **Data Lines**: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock**: One LVDS differential pair, 2.5 V compliant
- **Data Valid**: One LVDS differential pair, 2.5 V compliant
- **Data Suspend**: One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard**: Xilinx Virtex-6 XC6VLX130T
- **Optional**: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104**: Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**

- **Standard**: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165**: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**AMC Interface**

- **Type**: AMC.1
- **Module Management**: IPMI Version 2.0

**PCI-Express Interface**

- **PCI Express Bus**: Gen. 1: x4 or x8

**Environmental**

- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.

**Size**: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

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**Ordering Information**

**Model Description**

- 56610 LVDS Digital I/O with Virtex-6 FPGA - PCIe

**Options:**

- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS FPGA I/O through 68-pin ribbon cable connector
- 105 Gigabit serial FPGA I/O through two 4X top edge connectors
- 155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions.
Model 7811

Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

General Information
Model 7811 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 7811 serves as a flexible platform for developing and deploying custom FPGA processing IP.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 7811 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T or SX315T. The SX315T part features 1,344 DSP48E slices and is ideal for modulation/demodulation, encoding/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LX130T FPGA can be installed.

Features
- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fibre optic or copper serial interfaces
- PCIe Express interface up to x8
Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

➤ Serial FPDP Interface

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces or copper interfaces the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

PCI Express Interface

The Model 7811 includes an industry-standard interface fully compliant with PCI Express bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- Number of Connectors: 4
- Fiber Optic Connector Type: LC
  - Laser: 850 nm (standard, other options available)
- Copper Connector Type: SFP+
- Fiber or Copper Link Rates:
  - 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>7811</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe</td>
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</tbody>
</table>

Options:
- 062  XC6VLX240T FPGA
- 064  XC6VSX315T FPGA
- 280  Copper serial interfaces
- 281  Multi-mode optical serial interfaces

Model 8266

The Model 8266 is a fully-integrated PC development system. See 8266 Datasheet for Options.

Ordering Information

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<th>Description</th>
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<tr>
<td>8266</td>
<td>PC Development System</td>
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</tbody>
</table>

See 8266 Datasheet for Options
Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

General Information

Model 71611 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 71611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O

![Diagram of Model 71611 with FPGA and interfaces]
Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

Model 71611

➤ Serial FPDP Interface

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 71611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the module.

Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA

Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model 8266 PC Development System
See 8266 Datasheet for Options

Model Description
8266 PC Development System

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O through P14 connector
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
71611 Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O through P14 connector
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
Model 78611 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 78611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 78611 includes a general purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 78611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

**Features**

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O
Serial FPDP Interface

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 78611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4

Fiber Optic Connector Type: LC

Laser: 850 nm (standard, other options available)

Copper Connector Type: Micro Twinax

Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)

Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx

Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>78611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe</td>
</tr>
<tr>
<td>-062</td>
<td>XC6VLX240T FPGA</td>
</tr>
<tr>
<td>-064</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>-065</td>
<td>XC6VSX475T FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O through 68-pin ribbon cable connector</td>
</tr>
<tr>
<td>-155</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>-165</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
<tr>
<td>-280</td>
<td>Copper serial interfaces</td>
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<tr>
<td>-281</td>
<td>Multi-mode optical serial interfaces</td>
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<table>
<thead>
<tr>
<th>Model</th>
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</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
**General Information**

Model 78611 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 78611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 78611 includes a general purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 78611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe

**Serial FPDP Interface**

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

**Memory Resources**

The 78611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 78611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

**Specifications**

Front Panel Serial FPDP Inputs/Outputs
- Number of Connectors: 4
- Fiber Optic Connector Type: LC
- Laser: 850 nm (standard, other options available)
- Copper Connector Type: Micro Twinax
- Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.

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**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

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**Ordering Information**

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</tr>
</thead>
<tbody>
<tr>
<td>78611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -065 XC6VSX475T FPGA
- -104 LVDS FPGA I/O through 68-pin ribbon cable connector
- -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- -280 Copper serial interfaces
- -281 Multi-mode optical serial interfaces

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Model 53611 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 53611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express over the 3U VPX backplane, the Model 53611 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 53611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

**Model 53611 COTS (left) and rugged version**
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

➤ Serial FPDP Interface

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 53611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 53611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Crossbar Switch

The 53611 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4
Fiber optic Connector Type: LC
Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates:
1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

Orders Information

Model 53611 Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O to VPX P2
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Ordering Information

Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description
53611 Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O to VPX P2
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

VPX Family Comparison

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<thead>
<tr>
<th>Form Factor</th>
<th>52xxx</th>
<th>53xxx</th>
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<tbody>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td></td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
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<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
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</table>
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

**General Information**

Model 52611 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 52611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 52611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express over the 3U VPX backplane, the Model 52611 includes a general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 52611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

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**Features**

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x4
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

PCI Express Interface
The Model 52611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x4, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<tbody>
<tr>
<td>52611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
- 062  XC6VLX240T FPGA
- 064  XC6VSX315T FPGA
- 065  XC6VSX475T FPGA
- 104  LVDS FPGA I/O to VPX P2
- 205  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 215  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- 280  Copper serial interfaces
- 281  Multi-mode optical serial interfaces

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4

Environmental
Operating Temp: 0° to 50°C
Storage Temp: -20° to 90°C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

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<th>Form Factor</th>
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<td>3U VPX</td>
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<td>Crossbar Switch</td>
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<td>Yes</td>
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<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
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<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
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<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
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<td>Lowest Power</td>
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<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
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<th>Specifications</th>
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</thead>
<tbody>
<tr>
<td>Front Panel Serial FPDP Inputs/Outputs</td>
</tr>
<tr>
<td>Number of Connectors: 4</td>
</tr>
<tr>
<td>Fiber Optic Connector Type: LC Laser: 850 nm (standard, other options available)</td>
</tr>
<tr>
<td>Copper Connector Type: Micro Twinax Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)</td>
</tr>
<tr>
<td>Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port</td>
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<tr>
<td>Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T</td>
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<table>
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<tr>
<td>VPX Development System See 8267 Datasheet for Options</td>
<td></td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - 6U OpenVPX

Models 57611 and 58611

General Information
Models 57611 and 58611 are members of the Cobalt® family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71611 XMC modules mounted on a VPX carrier board.

Model 57611 is a 6U board with one Model 71611 module while the Model 58611 is a 6U board with two XMC modules rather than one.

These models are fully compatible with the VITA 17.1 Serial FPDP specification. Their built-in data transfer features make them complete turnkey solutions. For users who require application-specific functions, they serve as flexible platforms for developing and deploying custom FPGA processing IP.

The Cobalt Architecture
The Pentek Cobalt Architecture features one or two Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611.

Features
- Four or eight channels of Serial FPDP interface
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- One or two Virtex-6 FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - 6U OpenVPX

➤ Serial FPDP Interface

These models are fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the boards can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The architecture supports up to four or eight independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4 or 8
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)
 Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port
Field Programmable Gate Arrays: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T
Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611
Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8264 VPX Development System. See 8264 Datasheet for Options

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - cPCI

General Information
Models 72611, 73611 and 74611 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71611 XMC modules mounted on a cPCI carrier board.

Model 72611 is a 6U cPCI board while the Model 73611 is a 3U cPCI board; both are equipped with one Model 71611 XMC. Model 74611 is a 6U cPCI board with two XMC modules rather than one.

These models are fully compatible with the VITA 17.1 Serial FPDP specification. Their built-in data transfer features make them complete turnkey solutions. For users who require application-specific functions, they serve as flexible platforms for developing and deploying custom FPGA processing IP.

The Cobalt Architecture
The Pentek Cobalt Architecture features one or two Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a cPCI interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611.

Features
- Four or eight channels of Serial FPDP interface
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- One or two Virtex-6 FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM
- LVDS connections to the Virtex-6 FPGA for custom I/O

Block Diagram, Model 72611
Model 74611 doubles all resources except the PCI-to-PCI Bridge
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - cPCI

➤ Serial FPDP Interface
These models are fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gb/s link rates and the option for multi-mode and single-mode optical interfaces, the boards can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources
The architecture supports up to four or eight independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits (32 bits only, Model 73611) and data rates of 33 and 66 MHz are supported.

Specifications
Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4 or 8
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)

Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gb/s (copper rate depends on cable length)

Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
Option -104: provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611

Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

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<th>Description</th>
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<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI</td>
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<td>73611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 3U cPCI</td>
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<tr>
<td>74611</td>
<td>Octal Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
-062  XC6VLX240T FPGA
-064  XC6VSX315T FPGA
-065  XC6VSX475T FPGA

-104  LVDS I/O between the FPGA and J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611

-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280  Copper serial interfaces
-281  Multi-mode optical serial interfaces
Quad Serial FPDP Interface with Virtex-6 FPGA - AMC

**General Information**
Model 56611 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 56611 serves as a flexible platform for developing and deploying custom FPGA processing IP. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56611 includes a front panel general-purpose connector for application-specific I/O.

**The Cobalt Architecture**
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 56611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

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**Features**
- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

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**Configuration**

<table>
<thead>
<tr>
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<th>Memory Banks 3 &amp; 4</th>
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<th>AMC Ports 4 to 11</th>
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<td>DDR3 SDRAM 512 MB</td>
<td>DDR3 SDRAM 512 MB</td>
<td>64 MB</td>
<td>Front Panel</td>
</tr>
<tr>
<td>Option 155</td>
<td>Option 165</td>
<td></td>
<td>Front Panel</td>
</tr>
</tbody>
</table>

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**Diagram**

- Fiber optic or copper interfaces
- Up to 2 GB DDR3 SDRAM
- PCIe Gen. 2 x8 interface
- IPMI 2.0 compliant MMC
- AMC.1 compliant
- Optional front panel LVDS connections

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**Contact**
Pentek, Inc.
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Serial FPDP Interface

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 56611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the module.

Specifications

Front Panel Serial FPDP Inputs/Outputs

- Number of Connectors: 4
- Fiber Optic Connector Type: LC
  - Laser: 850 nm (standard, other options available)
- Copper Connector Type: Micro Twinax
- Copper or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O

- Option -04: Installs a front panel connector with 20 LVDS pairs to the FPGA
- Memory
  - Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- PCIe Bus: Gen. 1: x4 or x8
- AMC Interface
  - Type: AMC.1
  - Module Management: IPMI Version 2.0

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

<table>
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<th>Model</th>
<th>Description</th>
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<tr>
<td>56611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

Options:

-062  XC6VLX240T FPGA
-064  XC6VSX315T FPGA
-065  XC6VSX475T FPGA
-104  LVDS FPGA I/O through front panel connector
-155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280  Copper serial interfaces
-281  Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3312 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-312 3U VPX or the FlexorSet 7070-312 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312

The true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s task of identifying and executing on the data.

D/A Waveform Playback IP Module

With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming.

Features

- Sold as the:
  - FlexorSet Model 5973-312
  - FlexorSet Model 7070-312
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carriers
- Ruggedized and conduction-cooled versions available
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 3312**

- **4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A - FMC**

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3312’s hardware and IP-based functions. Ready to run examples and a full-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3312 or 7070/3312 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3312 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.

**Model 3312 Specifications**

- **Front Panel Analog Signal Inputs**
  - **Input Type:** Transformer-coupled, front panel connectors
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Input:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz
- **A/D Converters**
  - **Type:** Texas Instruments ADS42LB69
  - **Sampling Rate:** 10 MHz to 250 MHz
  - **Resolution:** 16 bits
- **D/A Converters**
  - **Type:** Texas Instruments DAC5688
  - **Input Data Rate:** 250 MHz max.
  - **Output IF:** DC to 400 MHz max.
  - **Output Sampling Rate:** 800 MHz max. with interpolation
  - **Resolution:** 16 bits
- **Front Panel Analog Signal Outputs**
  - **Output Type:** Transformer-coupled, front panel connector
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz
- **Sample Clock Sources**
  - **On-board clock**
  - **Clock Synthesizer**
    - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
    - **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
    - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
- **Clock Synthesizer**
  - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
  - **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
- **External Clock**
  - **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- **External Trigger Input**
  - **Type:** Front panel connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS
- **Environmental**
  - **Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized**
- **I/O Module Interface:** VITA-57.1, High-Pin Count FMC

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**Model 8266**

- **4-Ch. 250 MHz, 16-bit A/D, 2-Ch. 800 MHz, 16-bit D/A - FMC**

**Model 8267**

- **300 kHz to 700 MHz**
  - **3 dB Passband:** +4 dBm into 50 ohms
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Output Type:** Transformer-coupled, front panel connector
  - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
  - **Clock Synthesizer**
    - **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
    - **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
    - **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
  - **External Clock**
    - **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
  - **External Trigger Input**
    - **Type:** Front panel connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS
  - **Environmental**
    - **Level L1 & L2 air cooled, Level L3 conduction-cooled, ruggedized**
  - **I/O Module Interface:** VITA-57.1, High-Pin Count FMC

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**Ordering Information**

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<td>4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - FMC</td>
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**Contact Pentek for availability of rugged and conduction-cooled versions**

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**Model 8266**

- **PC Development System**
  - See 8266 Datasheet for Options

**Model 8267**

- **VPX Development System**
  - See 8267 Datasheet for Options
8-Channel 250 MHz, 16-bit A/D - FMC

**General Information**

The Flexor® Model 3316 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3316 is sold as a complete turnkey data acquisition solution as the FlexorSet™ 5973-316 3U OpenVPX or the FlexorSet 7070-316 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

**A/D Converters**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

**Performance of the Model 3316**

The true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

**A/D Acquisition IP Modules**

With the 3316 installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s task of identifying and executing on the data.

---

**Features**

- Sold as the:
  - **FlexorSet Model 5973-316**
  - **FlexorSet Model 7070-316**
- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available
8-Channel 250 MHz, 16-bit A/D - FMC

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from a front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized to create larger multiboard systems.

ReadyFlow Board Support Package
When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3316’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3316 or 7070/3316 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface
The Model 3316 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3316 and the FMC carrier.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<th>Model</th>
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<tbody>
<tr>
<td>3316</td>
<td>8-Channel 250 MHz, 16-bit A/D - FMC</td>
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Contact Pentek for availability of rugged and conduction-cooled versions

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
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<td>VPX Development System</td>
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<td></td>
<td>See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>

Model 8266 Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Sample Clock Source: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16

External Clock
- Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

I/O Module Interface: VITA-57.1, High-Pin Count FMC
**General Information**

The Flexor™ Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

The 3320 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-320 3U VPX or the FlexorSet 7070-320 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

**Performance of the Model 3320**

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**A/D and Digital Downconverter Stage**

The front end accepts two analog RF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

**A/D Acquisition IP Modules**

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data. See last page for configuration profiles.

---

**Features**

- Sold as the:
  - FlexorSet Model 5973-320
  - FlexorSet Model 7070-320
- Supports Xilinx Virtex-7 XTX FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Ruggedized and conduction-cooled versions available

---

**Diagram**

The diagram illustrates the flow of signals and data between the various components of the Model 3320, including the timing bus generator, A/D and D/A acquisition IP modules, and the FMC connector. Each component is labeled with its respective function and connections. The diagram also includes notes for configuration profiles and links to the next page for additional details.
**Model 3320**

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

➤ **Digital Upconverter and D/A Stage**

Two Texas Instruments DAC39J84 D/As accept two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

**D/A Waveform Playback IP Modules**

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

**Clocking and Synchronization**

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973 or the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the pre-defined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3320’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/320 or 7070/320 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3320 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier. ➤
### Model 3320 Specifications

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

**A/D Converters**

- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See table below

**Front Panel Analog Signal Outputs**

- **Output Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Coil Craft WBC4-14L
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 1.5 MHz to 1200 MHz

**D/A Converters**

- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See table below

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### Ordering Information

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**Options:**

- **-076** XCV7V90T-2 FPGA
- **-104** LVDS FPGA I/O to VPX P2
- **-110** VITA-66.4 12X (with VX90T), 4X (with VX330T) optical interface

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
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**Options:**

- **-076** XCV7V90T-2 FPGA
- **-104** LVDS FPGA I/O to card-edge connector
- **-110** VITA-66.4 12X (with VX90T), 4X (with VX330T) optical interface

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### Pre-configured Conversion Profiles*

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<tr>
<th>Converter Sample Rate</th>
<th>Output Resolution</th>
<th>Decimation</th>
<th>Output Data Rate**</th>
<th>Real / Complex</th>
<th>Interpolation</th>
<th>Input Data Rate**</th>
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<td>16 bit</td>
<td>4</td>
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<td>n/a</td>
<td>n/a</td>
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<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>2</td>
<td>5.6 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
<td>bypass</td>
<td>5.0 GB/sec</td>
<td>real</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>4.0 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
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<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>2.0 GB/sec</td>
<td>real</td>
<td>1</td>
<td>2.0 GB/sec</td>
<td>real</td>
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</table>

* Other modes can be custom-configured by the user

** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

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**Sample Clock Sources:** Timing bus generator provides A/D and D/A clocks

**Timing Bus Generator**

- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

**External Clock**

- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

**External Trigger Input**

- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Environmental**

- **Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized**
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

The Flexor™ Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3324 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-324 3U VPX or the FlexorSet 7070-324 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

Performance of the Model 3324

The true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3324 installed on either the 5973 or the 7070, the 3324 features four sophisticated A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gateway-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

With the 5973 or the 7070, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

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<td>4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A - FMC</td>
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</table>

Contact Pentek for availability of rugged and conduction-cooled versions

Model 3324 Specifications

- **Digital Upconverters and D/As**
  - Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.
  - When operating as DCUs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.
  - If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 1.5 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

- **Clocking and Synchronization**
  - Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.
  - A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized and create larger multiboard systems.

- **ReadyFlow Board Support Package**
  - When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3324’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

- **Extendable IP Design**
  - For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3324 or 7070/3324 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3324 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3324 and the FMC carrier.

**Model 3324 Specifications**

- **Front Panel Analog Signal Inputs**
  - **Input Type**: Transformer-coupled, front panel connectors
  - **Transformer Type**: Coil Craft WBC1-1TLB
  - **Full Scale Input**: +4 dBm into 50 ohms
  - **3 dB Passband**: 250 kHz to 750 MHz

- **A/D Converters**
  - **Type**: Texas Instruments ADS54J60
  - **Sampling Rate**: up to 500 MHz
  - **Resolution**: 16 bits

- **Front Panel Analog Signal Outputs**
  - **Output Type**: Transformer-coupled, front panel connectors
  - **Transformer Type**: Coil Craft WBC4-6TLB
  - **Full-Scale Output**: +4 dBm into 50 ohms
  - **3 dB Passband**: 300 kHz to 700 MHz

- **D/A Converters**
  - **Type**: Texas Instruments DAC38J84
  - **Input Data Rate**: Up to 500 MHz
  - **Output Sample Rate**: Up to 2 GHz (with interpolation)
  - **Resolution**: 16 bits

- **Sample Clock Source**: On-board clock synthesizer

- **Clock Synthesizer**
  - **Clock Source**: Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
  - **Synchronization**: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D and D/A clocks

- **External Clock**
  - **Type**: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

- **External Trigger Input**
  - **Type**: Front panel connector
  - **Function**: Programmable functions include: trigger, gate, sync and PPS

- **Environmental**
  - **Level L1 & L2**: air-cooled, 0 to +10 dBi, AC-coupled, 50 ohms
  - **Accuracy**: Level L3 air-cooled, Level L3 conduction-cooled, ruggedized

- **I/O Module Interface**: VITA-57.1, High-pin-count FMC
**General Information**

The Bandit Model 7120 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PMC/XMC module with front-panel connectors for easy integration into RF systems, the module offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7120 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 7120 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

The 7120 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

The 7120 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, the 7120 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

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**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

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**Diagram:**

[Diagram of Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC Model 7120]
**Specifications**

**RF Input**
- Connector Type: SSMC
- Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm

**Flatness:**
- ±2 dB from 400 MHz to 1 GHz,
- ±3 dB from 1 GHz to 3 GHz,
- ±5 dB from 3 GHz to 4 GHz

**RF Attenuator:** Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- Connector Type: SSMC
- Impedance: 50 ohms

**Reference Input Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**Reference Output Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**OCXO Reference**
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm

**Aging**
- Daily: ±10 ppb/day
- First Year: ±300 ppb
- Total Frequency Tolerance (20 years): ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 kHz Offset: –148 dBc/Hz
- 10 kHz Offset: –154 dBc/Hz
- 100 kHz Offset: –155 dBc/Hz

**IF Output**
- Connector Type: SSMC
- Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Attenu, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12 VDC
- Current: 1.5 A

**PMC/XMC Interface:** Power only on PMC P11 (option -104) or XMC P15 (option -105)

**Size:** Standard PMC module, 2.91 in. x 5.87 in.

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**Ordering Information**

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<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<td>Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC</td>
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<tr>
<th>Option</th>
<th>Description</th>
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<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-104</td>
<td>PMC P11 Power</td>
</tr>
<tr>
<td>-105</td>
<td>XMC P15 Power</td>
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<tr>
<td>-106</td>
<td>PCIe 6-pin connector (Power only)</td>
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<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
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<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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**General Information**

The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, the 7820 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
**Specifications**

**RF Input**
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm

**Flatness:**
- ±2 dB from 400 MHz to 1 GHz,
- ±3 dB from 1 GHz to 3 GHz,
- ±5 dB from 3 GHz to 4 GHz

**RF Attenuator:** Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: -90 dBc/Hz
- 100 kHz: -110 dBc/Hz
- 1 MHz: -130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms

**Reference Input Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**Reference Output Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**OCXO Reference**
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm

**Aging**
- Daily: ±10 ppb/day
- First Year: ±300 ppb

**Total Frequency Tolerance**
- (20 years): ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: -67 dBc/Hz
- 10 Hz Offset: -100 dBc/Hz
- 100 Hz Offset: -130 dBc/Hz
- 1 KHz Offset: -148 dBc/Hz
- 10 KHz Offset: -154 dBc/Hz
- 100 KHz Offset: -155 dBc/Hz

**IF Output**
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12 VDC
- Current: 1.5 A

**PCI-Express Interface**
- PCI Express Bus: x4 or x8, power only

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

**Size:** Half length PCIe card, 4.38 in. x 7.13 in.

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**Ordering Information**

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<th>Description</th>
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<td>Bandit Two-Channel Analog RF Wideband Downconverter - PCIe</td>
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<th>Description</th>
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<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

General Information

The Bandit® Model 5220 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded 3U VPX board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5220 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5220 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5220 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5220 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5220 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference
Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

Specifications

RF Input
Connector Type: SSMC
Input Impedance: 50 ohms
Input Level Range: -60 dBm to -20 dBm
Flatness: ±2 dB from 400 MHz to 1 GHz,
±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
Frequency range: 400–4000 MHz,
Resolution: < 10 kHz
Tuning Speed: < 500 µsec
Phase-Locked Loop Bandwidth: 100 kHz
Phase Noise
1 kHz: –90 dBc/Hz
100 kHz: –110 dBc/Hz
1 MHz: –130 dBc/Hz

Noise Figure (referred to input)
60 dB gain: 2.6 dB

RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

IF Output
Connector Type: SSMC
Output Impedance: 50 ohms
Center Frequency: User definable
Output Level: 0 dBm, nominal

Programming
Functions: RF Attenu, IF Attenu, Int/Ext Reference Select, LO Synthesizer Frequency Interface: USB
Connector Type: MicroUSB
Power
Voltage: +12 VDC
Current: 1.5 A

PCI Express Interface
PCIe Bus: x4, power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model | Description
--- | ---
5220 | Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

Option | Description
--- | ---
-015 | Oven Controlled Reference Oscillator
-145 | 1.45 GHz lowpass input filter
-280 | 2.80 GHz lowpass input filter
General Information

These Bandit® models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded 6U VPX boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 5720 is a 6U VPX board that provides two channels, while Model 5820 is a double-density 6U VPX board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U OpenVPX

Specifications

RF Input
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm

Flatness: ±2 dB from 400 MHz to 1 GHz,
±3 dB from 1 GHz to 3 GHz, ±5 dB from
3 GHz to 4 GHz

RF Attenuator: Programmable from 0 to
63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

Phase Noise
- 1 kHz: -90 dBc/Hz
- 10 kHz: -110 dBc/Hz
- 1 MHz: -130 dBc/Hz

Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in
  Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  (20 years): ±4.60 ppm

Phase Noise
- 1 Hz Offset: -67 dBc/Hz
- 10 Hz Offset: -100 dBc/Hz
- 100 Hz Offset: -130 dBc/Hz
- 1 KHz Offset: -148 dBc/Hz
- 10 KHz Offset: -154 dBc/Hz
- 100 KHz Offset: -155 dBc/Hz

IF Output
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Reference Input/Output
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms

Reference Input Signal
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

Reference Output Signal
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI Express Interface
- PCI Bus: x4 or x8, power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)

Ordering Information

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<td>5820</td>
<td>Bandit Four-Channel Analog RF Wideband Downconverter - 6U VPX Double Density</td>
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<th>Option</th>
<th>Description</th>
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<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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</tbody>
</table>
General Information

These Bandit™ models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded cPCI boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 7320 is a 3U cPCI board while Model 7220 is a 6U cPCI board; both provide two channels, while Model 7420 is a double-density 6U cPCI board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
## Specifications

| RF Input | Connector Type: SSMC  
| Input Impedance: 50 ohms  
| Input Level Range: -60 dBm to -20 dBm  
| Flatness: ±2 dB from 400 MHz to 1 GHz,  
| ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz |  
| RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps |

| LO Synthesizer Tuning | Frequency range: 400–4000 MHz,  
| Resolution: < 10 kHz  
| Tuning Speed: < 500 µsec |

| Phase Noise | 1 kHz: −90 dBc/Hz  
| 100 kHz: −110 dBc/Hz  
| 1 MHz: −130 dBc/Hz |

| Noise Figure (referred to input) | 60 dB gain: 2.6 dB |

| Inband Output IP3 | 20 dB gain: +10 dBm  
| 60 dB gain: +42 dBm |

| Reference Input/Output | Connector Type: SSMC  
| Input/Output Impedance: 50 ohms  
| Reference Input Signal | Frequency: 10 MHz  
| Level: 0 dBm, sine wave |

| Reference Output Signal | Frequency: 10 MHz  
| Level: 0 dBm, sine wave |

## OCXO Reference

| Center Frequency: 10 MHz  
| Frequency Stability vs. Change in Temperature: ±50.0 ppb  
| Frequency Calibration: ±1.0 ppm |

| Aging | Daily: ±10 ppb/day  
| First Year: ±300 ppb  
| Total Frequency Tolerance (20 years): ±4.60 ppm |

| Phase Noise | 1 Hz Offset: −67 dBc/Hz  
| 10 Hz Offset: −100 dBc/Hz  
| 100 Hz Offset: −130 dBc/Hz  
| 1 kHz Offset: −148 dBc/Hz  
| 10 kHz Offset: −154 dBc/Hz  
| 100 kHz Offset: −155 dBc/Hz |

## IF Output

| Connector Type: SSMC  
| Output Impedance: 50 ohms |

| Center Frequency: User definable  
| Output Level: 0 dBm, nominal |

## Programming

| Functions: RF Atten, IF Atten, Int/Ext  
| Reference Select, LO Synthesizer Frequency Interface: USB  
| Connector Type: MicroUSB |

## Power

| Voltage: +12 VDC  
| Current: 1.5 A |

## PCI Interface

| PCI Bus: 32-bit, 66 MHz (supports 33 MHz), power only |

## Environmental

| Operating Temp: 0° to 50° C  
| Storage Temp: −20° to 90° C  
| Relative Humidity: 0 to 95%, non-cond. |

## Size

| Standard 3U or 6U cPCI board |

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### Ordering Information

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<th>Model</th>
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<td>7320</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - 3U cPCI</td>
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<td>7420</td>
<td>Bandit Four-Channel Analog RF Wideband Downconverter - 6U cPCI</td>
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<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
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</table>
**General Information**

The Bandit® Model 5620 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded AMC board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5620 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 5620 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

The 5620 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

The 5620 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, the 5620 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

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**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

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**Diagram**

- RF In
- Ref In
- Low Noise Amp
- Gain 1 Control
- Gain 2 Control
- USB Interface
- SYNTESIZER
- Tuning Control
- Ref Out
- IF I Out
- IF Q Out
- Option 015
- Oven Controlled Reference Oscillator

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> Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
### Specifications

**RF Input**
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: -90 dBc/Hz
- 100 kHz: -110 dBc/Hz
- 1 MHz: -130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave
- Reference Output Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave

**OCXO Reference**
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  - (20 years): ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: -67 dBc/Hz
- 10 Hz Offset: -100 dBc/Hz
- 100 Hz Offset: -130 dBc/Hz
- 1 KH Offset: -148 dBc/Hz
- 10 KH Offset: -154 dBc/Hz
- 100 KH Offset: -155 dBc/Hz

**IF Output**
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12 VDC
- Current: 1.5 A

**PCI-Express Interface**
- PCI Express Bus: Gen. 1 x4 or x8, power only

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

---

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
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<tbody>
<tr>
<td>5620</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - AMC</td>
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<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
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**General Information**

The Bandit® Model 8111 provides a series of high-performance, stand-alone analog RF slot downconverter modules. Packaged in a small, shielded enclosure with connectors for easy integration into RF systems, the modules offer programmable gain, high dynamic range and a low noise figure. With input options to cover specific frequency bands of the RF spectrum, and an IF output optimized for A/D converters, the 8111 is an ideal solution for amplifying and down-converting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 8111 accepts RF signals on a front panel SMA connector. An LNA (Low Noise-figure Amplifier) is provided along with two programmable attenuators allowing downconversion of input signals ranging from -60 dBm to -20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Preselector Options**

Seven different input-frequency band options are offered, each tunable across a 400 MHz band, with an overlap of 100 MHz between adjacent bands. As a group, these seven options accommodate RF input signals from 800 MHz to 3.000 GHz as follows:

<table>
<thead>
<tr>
<th>Option</th>
<th>Frequency Band</th>
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</thead>
<tbody>
<tr>
<td>001</td>
<td>800-1200 MHz</td>
</tr>
<tr>
<td>002</td>
<td>1100-1500 MHz</td>
</tr>
<tr>
<td>003</td>
<td>1400-1800 MHz</td>
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<tr>
<td>004</td>
<td>1700-2100 MHz</td>
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<td>005</td>
<td>2000-2400 MHz</td>
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<tr>
<td>006</td>
<td>2300-2700 MHz</td>
</tr>
<tr>
<td>007</td>
<td>2600-3000 MHz</td>
</tr>
</tbody>
</table>

**Tuning Accuracy**

The 8111 uses a low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy, its frequency is programmable across the 400 MHz band with a tuning resolution of 1 MHz. Alternatively, for applications demanding custom local oscillator characteristics, an external LO input signal can be accepted on a front panel connector and used instead of the on-board frequency synthesizer.

**On-board Reference Clock**

In addition to accepting a reference signal on the front panel, the 8111 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**IF Output**

An 80 MHz-wide IF output is provided at a 225 MHz center frequency. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Modular Analog RF Slot Downconverter Series

**Model 8111**

### Specifications

**RF Input**
- Connector Type: SMA
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±1 dB typical over each 400 MHz range

**RF Attenuator**: Programmable from 0 to 31.5 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 800-3000 MHz, across seven different options
- Resolution: 1 MHz
- Tuning Speed: < 500 µsec
- PLL Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: -90 dBc/Hz
- 100 kHz: -110 dBc/Hz
- 1 MHz: -130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**Inband Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference / External LO Input**
- Connector Type: SMA
- Input Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm to +20 dBm, sinewave

**External LO Input Signal**
- Frequency: $f_{\text{RF}} + 225$ MHz, where $f_{\text{RF}}$ = RF input signal frequency
- Level: 0 dBm ±2 dBm

**OCXO Reference Output**
- Connector Type: SMA
- Center Frequency: 10 MHz
- Output Impedance: 50 ohms
- Output Level: +10 dBm, nominal, sine wave
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance (20 years): ±4.60 ppm

**Phase Noise**
- 1 Hz Offset: -67 dBc/Hz
- 10 Hz Offset: -100 dBc/Hz
- 100 Hz Offset: -130 dBc/Hz
- 1 KHz Offset: -148 dBc/Hz
- 10 KHz Offset: -154 dBc/Hz
- 100 KHz Offset: -155 dBc/Hz

**IF Attenuator**: Programmable from 0 to 31.5 dB in 0.5 dB steps

**IF Output**
- Connector Type: SMA
- Output Impedance: 50 ohms
- Center Frequency: 225 MHz
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Atten, IF Atten, Int/Ext LO Select, LO Synthezier Frequency Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12VDC
- Current: 1.5 A
- Connector Type: Micro DB-9, female

**Size**: Module, 3.75 in x 7.5 in x 0.7 in

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**Ordering Information**

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<td>Bandit Modular Analog RF Slot Downconverter</td>
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<tr>
<th>Option</th>
<th>Input Frequency Band</th>
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<tr>
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</tr>
<tr>
<td>-006</td>
<td>2300-2700 MHz</td>
</tr>
<tr>
<td>-007</td>
<td>2600-3000 MHz</td>
</tr>
</tbody>
</table>
General Information

The Model 8264 is a fully-integrated, 6U VPX development system for Pentek Cobalt® and Onyx® software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 9U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19” 9U rackmount chassis that is 16” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

All 8264 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8264 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB
Dimensions: 6U Chassis, 19” W x 16” D x 10.5” H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model Description
8264 6U VPX Development System for Cobalt and Onyx Boards
Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
Model 8266

PC Development System for PCIe Cobalt, Onyx and Flexor Boards

General Information
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx® and Flexor™ PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation
Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19” 4U rackmount chassis that is 21” deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration
Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options
Options for high-end multicore CPUs and extended memory support applications that require additional horsepower are available.

Specifications
Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 8 GB
Dimensions: 4U Chassis, 19” W x 21” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information
Model Description
8266 PC Development System for PCIe Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS
-101 Upgrade to 64 GB DDR3 SDRAM

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.

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Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
Model 8267

3U VPX Development System for Cobalt, Onyx and Flexor Boards

General Information
The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software
Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19” 4U rackmount chassis that is 12” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options
Available options include high-end multi-core CPUs and extended memory support.

Specifications
Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 8 GB standard, 16 GB optional
Dimensions: 4U Chassis, 19” W x 12” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Features
- 9-slot, 4U 19-inch rackmount, 12-inch deep chassis which houses 3U VPX boards
- 64-bit Windows® 7 Professional or Linux® workstation
- Intel® Core™ i7 3.6 GHz processor
- 8 GB DDR3 SDRAM
- ReadyFlow® drivers and board support libraries installed
- Out-of-the-box ready-to-run examples

System Information
All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Ordering Information
Model Description
8267 3U VPX Development System for Cobalt, Onyx and Flexor Boards

Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS
-101 Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.

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Tel: 201-818-5900 ♦ Fax: 201-818-5904 ♦ Email: info@pentek.com www.pentek.com
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We’re glad to respond to your request for price quotation just contact the corporate office, or your local representative.

Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at:

Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900 • fax: 201-818-5697 • email: custsvc@pentek.com

www.pentek.com
# High-Speed Recording Systems

## Model Description

**Talon**
- Talon® High-Speed Recording Systems: Flexible and Deployable Solutions

**RTX Rackmount**
- Talon RTX Extreme Rackmount Recorders - Mechanical Design

## Analog Recording Systems

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<tr>
<th>Model</th>
<th>Description</th>
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</thead>
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<td>RTV 2601</td>
<td>200 MS/sec RF/IF Rackmount Value Recorder</td>
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<tr>
<td>RTS 2706</td>
<td>200 MS/sec RF/IF Rackmount Recorder</td>
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<td>RTR 2726</td>
<td>200 MS/sec RF/IF Rugged Portable Recorder</td>
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<td>RTR 2726A</td>
<td>200 MS/sec RF/IF Rugged Portable Recorder</td>
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<td>RTR 2746</td>
<td>200 MS/sec RF/IF Rugged Rackmount Recorder</td>
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<td>200 MS/sec RF/IF Extreme Rackmount Recorder</td>
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[Customer Information](#)

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**ANALOG RECORDING SYSTEMS**

[Click Here for the PRODUCT SELECTOR](#)

Last updated: April 2018
# HIGH-SPEED RECORDING SYSTEMS

## MODEL DESCRIPTION

### DIGITAL RECORDING SYSTEMS

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</tr>
<tr>
<td>RTS 2718</td>
<td>LVDS Digital I/O Rackmount Recorder</td>
</tr>
<tr>
<td>RTR 2738A</td>
<td>LVDS Digital I/O Rugged Portable Recorder</td>
</tr>
<tr>
<td>RTR 2758</td>
<td>LVDS Digital I/O Rugged Rackmount Recorder</td>
</tr>
<tr>
<td>RTX 2778</td>
<td>LVDS Digital I/O Extreme Rackmount Recorder</td>
</tr>
<tr>
<td>RTR 2555</td>
<td>1, 10, 40-Gigabit Ethernet Rugged SFF Recorder</td>
</tr>
<tr>
<td>RTR 2556</td>
<td>Serial FPDP Rugged SFF Recorder</td>
</tr>
<tr>
<td>RTR 2558</td>
<td>LVDS Digital I/O Rugged SFF Recorder</td>
</tr>
</tbody>
</table>

Customer Information

Last updated: April 2018
Talon High-Speed Recording Systems: Flexible and Deployable Solutions

Systems Include:
- High-performance Windows® workstation
- High-performance Intel® Processor
- Pentek SystemFlow® recording software with graphical user interface
- SystemFlow analysis tools such as virtual oscilloscope and spectrum analyzer
- Supported RAID levels of up to 0, 1, 5, 6, 10 and 50
- Time and position stamping support
- Detailed technical documentation

Systems Benefits:
- Complete turnkey systems
- Rack-mountable and portable form factors
- C-callable API for integration of recorder into application
- Aggregate recording rates of up to 5.0 GB/sec
- Recording to non-proprietary NTFS file system for easy and immediate data access
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom
- They are easy to use right out-of-the-box
- Can be controlled over the Ethernet or over the Internet

High-Speed Recording Systems
Talon® High-Speed Recording Systems eliminate the time and risk associated with new technology system development. With increasing pressure in both the defense and commercial arenas to get to the market first, today’s system engineers are looking for more complete off-the-shelf system offerings.

Out of the box, these systems arrive complete with a full-featured virtual operator control panel ready for immediate data recording and/or playback operation.

Because they consist of modular COTS board-level products and the flexible Pentek SystemFlow software, they are easily scalable to larger multichannel data acquisition and recording applications requiring aggregate recording rates of up to 5.0 GB/sec.

Ready-to-Run Recording Systems
Depending on model, the Pentek offerings are fully integrated systems featuring a range of A/D and D/A resources or digital I/O with high-speed disk arrays.

Since these systems are built on a Windows workstation, users can easily install post-processing and analysis tools to operate on the recorded data.

Pentek systems provide a flexible architecture that can be easily customized to meet user needs. Multiple RAID levels of up to 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

Systems for All Recording Needs
Pentek’s High-Speed Recording Systems are available as Lab Systems, Portable Systems, Rugged, and Extreme Systems.

RTV and RTS Lab Systems are housed in a 19-in. rack-mountable chassis in a PC server configuration. They are designed for commercial applications in a lab or office environment.

RTR Portable Systems are available in a small briefcase-sized enclosure with an integral LCD display and keyboard. They, too, provide a PC server configuration and are designed for commercial or harsh environment field applications where size and weight is of paramount importance.

RTR Rugged Rackmount Systems are housed in a 19-in. rugged rack-mountable chassis. They are built to survive shock and vibration and they target operation in harsh environments and remote locations that may be unsuitable for humans.

RTX Extreme Systems are available in either a rackmount chassis designed to military specs, or a ½ ATR chassis.

They are designed to operate under extreme environmental conditions using forced-air or conduction-cooling to draw heat from system components.
SystemFlow Architecture

Server/Client Architecture
As shown in the block diagram, the SystemFlow architecture provides for easy communication between the recording system Server on the right and the Client PC on the left.

SystemFlow GUI
The SystemFlow architecture features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Function Libraries
The function libraries and tools for controlling the recording and playback functions include the Application Programming Interface, the Graphical User Interface and the integrated Signal Viewer.

SystemFlow API
The SystemFlow API allows developers to configure and customize the system interfaces and operation. Source code is supplied for all client API functions. A well-defined set of plugins allows the user to extend server API functions.

SystemFlow Record/Play GUI Application
SystemFlow JAVA Client API
SystemFlow Record/Play Server Application
LabVIEW Signal Viewer
Sockets
SystemFlow Command Processor
User Control Block
User Proc. Block
Windows Drivers
Windows Operating System
NTFS
Client Operating System (Windows/Linux/Other)

Server/Client Communication
Server and Client communicate through a standard socket connection. This arrangement enables the Server to provide real-time recording and playback functions that can be controlled from a local or a remote Client. It also allows Client and Server to run on different operating systems.

SystemFlow Signal Viewer
SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer. More information on the Signal Viewer is provided on the next page.

NTFS File System
The NTFS file management system provides immediate access to the recorded data, thereby eliminating time-consuming data conversion processes required with proprietary file management systems. It also eliminates the need for custom hardware and software platforms where the recorded data may need to be physically transported for conversion.
SystemFlow Graphical User Interface

The SystemFlow GUI displays a block diagram of the system and provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels.

SystemFlow Recorder Interface

SystemFlow Hardware Configuration Interface

The SystemFlow Recorder Interface

The SystemFlow Hardware Configuration Interface

The SystemFlow Configure screen provides a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Recorder Interface

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

SystemFlow Hardware Configuration Interface

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.
Recording and Playback Dataflow

Recording Dataflow

Shown in this diagram is the dataflow during a typical recording session. The Pentek Transceiver Board contains a 2-channel 200 MHz A/D for digitizing two input analog channels. The digitized outputs are downconverted by the two DDCs (Digital Downconverters) and moved on to the PC system memory via the PCI Express interface. Both the DDCs and the PCIe interface are implemented in the board’s FPGA. Data then moves from the system memory to the Recording System RAID Controller and is then recorded to disk via the SATA interface. DMA controllers conduct all data transfers, bypassing the CPU for guaranteed real-time operation.

Playback Dataflow

During a playback session, data stored on disk moves through the SATA interface of the Playback System RAID Controller. From there, data is passed to the PC system memory through the PCIe interface and then to the Pentek Transceiver board through its PCIe interface, all via hardware DMA controllers for real-time operation. This board also contains DUCs (Digital Upconverters) which upconvert the data to the original IF frequency bands. Two 800 MHz D/As convert the data to analog form and provide signals that are identical to the analog signals that were originally recorded. These can be further analyzed with any Windows-compatible analysis software.
**Extreme Rackmount Recorders**

Pentek’s Talon® RTX Rackmount series recorders are designed to provide a combination of high performance and large storage capacity in a military-specified rackmount chassis. Designed for field operation, the RTX Rackmount series provides up to 30 TB of SSD storage with aggregate recording rates up to 5 GB/sec.

**Military Specifications**

All Talon RTX rackmount recorders are designed to meet military specifications for temperature, altitude, shock, vibration, radiated emissions, conducted emissions, ESD, sand, and dust.

The following list contains these military specifications.

- **Vibration:** MIL-STD-810F, method 514.5
- **Shock:** MIL-STD-810F, method 516.5
- **EMI/EMC:** MIL-STD-461E, CE101, CE102, CS101 CS114, RE101, RE102, RS101, RS103
- **ESD:** MIL-STD-1686A
- **Sand & Dust:** MIL-STD-810F, method 510

**Chassis Design**

All Talon RTX rackmount chassis are specially designed using heavy-duty wrought aluminum extrusions to provide superior torsional strength. Extrusions are partially overlapped for superior EMC. The chassis is 4U in height, with a depth of only 22". A fully-loaded chassis weighs as little as 45 lb. Rear-panel I/O includes bulk-head mounted SMA connectors, a 4-pin 38999 power connector as well as motherboard I/O. Rear-panels are modular and customizable allowing the end-user to specify the desired connectors.

The Operating System drive can be internally hard-mounted or can be made removable. Additionally an internally-mounted optical DVD writer is optional. All drives, OS, DVD and data drives are protected from dust with EMI filters.

**QuickPac Canisters**

In order to provide field engineers the ability to quickly remove and replace storage drives in the field, Pentek has developed the QuickPac™ canisters for use in the Talon RTX rackmount chassis. These canisters hold eight SSDs, providing up to 7.68 TB of storage capacity in each canister. Up to four QuickPac canisters can be installed in a Talon RTX rackmount chassis, providing a total storage capacity of 30 TB.

Fastened by four thumbscrews, QuickPac canisters can easily be swapped in the field, allowing users to replace those filled with data with new, empty ones with very little down time. QuickPac canisters can be transported to the lab for offload or analysis, using one of Pentek’s Talon offload or playback systems.

**Floating Inner Chassis**

In order to withstand conditions of high vibration and shock, the RTX rackmount chassis is designed to isolate all critical system components by placing them on a floating inner chassis.

This inner chassis is suspended using multiaxis mounts that attenuate externally-transmitted shock and vibration energy. This allows the system to perform flawlessly in aircraft, ships, ground vehicles, UAVs or any other areas of high shock or vibration.
Cooling and Filtering

Every RTX recorder includes a high-powered forced air-cooling system, to allow the proper transfer of heat from hot system components out the back of the chassis. Cool air is pulled from the front of the system through the QuickPac drive packs and forced over the hottest system components to ensure optimal cooling.

High-powered fans can be controlled via system software to allow the system to run quietly with lower cooling levels or at maximum air flow levels. This can be adjusted to match the user’s application.

Every RTX recorder includes filtering necessary to protect the system as well as the surrounding operating environment. EMI filters are placed on the front and rear of the chassis, to protect the surrounding environment from radiated emissions. A removable front panel filter protects the system against dust and sand.

Modular Power Supply

Every Talon RTX rackmount Recorder includes a 600 Watt, 85 – 264 V, 47– 400 Hz AC power supply. The power supply has an inline EMI filter to protect against conducted emissions and is isolated from the other electronics in the system, via an isolated chassis compartment. The 400 Hz rating allows every RTX rackmount recorder to operate in aircraft and other environments where smaller, 400 Hz generators are used. For applications that require DC power, 24 V and 28 V DC power supplies are available to replace the AC power supply.

Talon Solutions Chart

The chart below compares Pentek’s different Talon Recording System solutions. As seen here, the RTX Rackmount series provide high performance and large storage capacity in a rugged package that meets high-level military specifications.

<table>
<thead>
<tr>
<th>Talon Chassis Type</th>
<th>RTS-COTS Rackmount</th>
<th>RTR Portable</th>
<th>RTR Rackmount</th>
<th>RTX Rackmount</th>
<th>RTX 1/2 ATR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dimensions (H&quot;xW&quot;xL&quot;)</td>
<td>7x19x26</td>
<td>13.4x16.9x9.5</td>
<td>7x19x21/26</td>
<td>7x19x22</td>
<td>8.1x7.1x16.5</td>
</tr>
<tr>
<td>Weight (lb)</td>
<td>60–85</td>
<td>30–35</td>
<td>45–85</td>
<td>45–60</td>
<td>30–35</td>
</tr>
<tr>
<td>Cooling</td>
<td>Forced-air</td>
<td>Forced-air</td>
<td>Forced-air</td>
<td>Forced-air</td>
<td>Conduction</td>
</tr>
<tr>
<td>Storage Drive Type</td>
<td>HDD</td>
<td>SSD</td>
<td>SSD</td>
<td>SSD</td>
<td>SSD</td>
</tr>
<tr>
<td>Max. Storage Capacity (TB)</td>
<td>60</td>
<td>7.6</td>
<td>38.4</td>
<td>30.7</td>
<td>3.8</td>
</tr>
<tr>
<td>Max. Record Rate (MB/sec)</td>
<td>1600</td>
<td>1600</td>
<td>5000</td>
<td>5000</td>
<td>500</td>
</tr>
<tr>
<td>Drive Removal</td>
<td>Individual (with trays)</td>
<td>Individual (no trays)</td>
<td>Individual (with trays)</td>
<td>QuickPac Canisters (needs disassembly)</td>
<td></td>
</tr>
<tr>
<td>Operating Temperature (deg C)</td>
<td>5 to 45</td>
<td>0 to 50</td>
<td>–10 to 55</td>
<td>–20 to 55</td>
<td>–40 to 71</td>
</tr>
<tr>
<td>Operating Altitude (ft)</td>
<td>10,000</td>
<td>10,000</td>
<td>10,000</td>
<td>10,000</td>
<td>65,000</td>
</tr>
<tr>
<td>Shock</td>
<td>–</td>
<td>15 g</td>
<td>15 g</td>
<td>MIL-STD-810F Method 516.5</td>
<td>MIL-STD-810F Method 516.5</td>
</tr>
<tr>
<td>Vibration</td>
<td>–</td>
<td>1.4 g</td>
<td>1.4 g</td>
<td>MIL-STD-810F Method 514.5</td>
<td>MIL-STD-810F Method 514.5</td>
</tr>
<tr>
<td>ESD</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>MIL-STD-1686A</td>
<td>–</td>
</tr>
<tr>
<td>Sand and Dust</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>MIL-STD-810F Method 510</td>
<td>MIL-STD-810F Method 510</td>
</tr>
</tbody>
</table>
Appendix A - System Specifications Summary

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>Operating</td>
<td>–20° C to +55° C</td>
</tr>
<tr>
<td></td>
<td>Non-operating</td>
<td>–40° C to +70° C</td>
</tr>
<tr>
<td>Altitude</td>
<td>Operating</td>
<td>0 to 15,000 ft</td>
</tr>
<tr>
<td></td>
<td>Non-operating</td>
<td>0 to 40,000 ft</td>
</tr>
<tr>
<td>Humidity</td>
<td>Operating</td>
<td>0–95%, non-condensing</td>
</tr>
<tr>
<td>Fungus</td>
<td>Operating</td>
<td>No fungus nutrient material shall be used</td>
</tr>
<tr>
<td>Shock</td>
<td>Operating</td>
<td>MIL-STD-810F, Method 516.5, Procedure I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(functional shock), 20 g half sine, 12 msec in each axis</td>
</tr>
<tr>
<td>Vibration</td>
<td>Operating</td>
<td>MIL-STD-810F, Method 514.5, Procedure I</td>
</tr>
<tr>
<td>Airborne Noise</td>
<td>Operating</td>
<td>60 dBA max at 1 meter from the equipment</td>
</tr>
<tr>
<td>Structure-borne Noise</td>
<td>Operating</td>
<td>Maximum structure-borne noise per MIL-STD-704-2 is no greater than 60 dB one-third octave La, (Type III)</td>
</tr>
<tr>
<td>Blowing Dust</td>
<td>Operating</td>
<td>The unit shall resume specified performance after exposed to settling-dust conditions defined in MIL-STD-810F, Method 510, Procedure II - See Note 1</td>
</tr>
<tr>
<td>Inclination Angles</td>
<td>Operating</td>
<td>The unit shall maintain specified performance when subjected to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• A static pitch angle of ±5°</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• A list angle of 15°</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• A roll angle of 45°</td>
</tr>
</tbody>
</table>

Note 1: Standard maintenance includes cleaning of the dust filter(s) as required.

Appendix B - Emissions Specifications Summary

CE101: Conducted Emissions, Power Leads, 30 Hz to 10 kHz
CE102: Conducted Emissions, Power Leads, 10 kHz to 10 MHz
CS101: Conducted Susceptibility, Power Leads, 30 Hz to 50 kHz
CS114: Conducted Susceptibility, Bulk Cable Injection, 10 kHz to 400 MHz
CS116: Conducted Susceptibility, Damped Sinusoidal Transients, Cable and Power Leads, 10 kHz to 100 MHz
RE101: Radiated Emissions, Magnetic Field, 30 Hz to 100 kHz
RE102: Radiated Emissions, Electric Field, 10 kHz to 18 GHz
RS101: Radiated Susceptibility, Magnetic Field, 30 Hz to 100 kHz
RS103: Radiated Susceptibility, Electric Field, 10 kHz to 40 GHz

Specifications are subject to change without notice
General Information

The Talon® RTV 2601 is a turnkey multi-band recording and playback system used for recording and reproducing signals with bandwidths up to 80 MHz. The RTV 2601 uses a 16-bit, 200 MHz A/D converter to provide real-time sustained recording rates to disk of up to 400 MB/sec. The A/D is complemented with a 16-bit 800 MHz D/A that provides the ability to reproduce signals captured in the field.

The RTV 2601 comes in a 4U 19 in. rack-mount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available at the front. Air is pulled through the system from front to back allowing it to operate at ambient temperatures from 5 to 35 deg C.

The RTV 2601 includes a programmable digital downconverter so users can configure the system to capture signals with frequencies as low as 300 kHz and as high as 700 MHz. Corresponding signal bandwidths range from a few kilohertz to 80 MHz. A digital upconverter and D/A produce an analog output matching the recorded IF signal frequency.

The system includes a built-in sample clock synthesizer programmable to any desired frequency from 10 MHz to 200 MHz. This clock synthesizer can be locked to an external 10 MHz reference clock and has excellent phase noise characteristics. Alternately, the user can supply an external sample clock to drive the A/D and D/A converters. The RTV 2601 also supports external triggering, allowing users to trigger a recording or playback on an external signal.

As an option, a GPS or IRIG receiver card can be supplied with the system providing accurate time stamping of recorded data. Additionally, the GPS receiver delivers GPS position information that can be recorded along with the analog input signal.

SystemFlow Software and API

The RTV 2601 includes the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, so users can select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, for monitoring the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

In addition to the GUI, the RTV 2601 provides a C-callable API, which allows the user to integrate the recorder control into any application. A simple set of commands that provide configuration and control come with source code and examples to allow for an exceptionally fast integration.

Features

- Single-channel multiband recording and playback system.
- 4U 19-inch industrial rack-mount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i3 processor
- 200 MHz max. 16-bit A/D sampling for recording
- 800 MHz max. 16-bit D/A sampling for playback
- 80 MHz recording and playback signal bandwidths
- Capable of record/playback of IF frequencies to 700 MHz
- Real-time aggregate recording rates up to 400 MB/sec
- 4 TB of data storage to NTFS RAID disk array
- SystemFlow® recording software with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- DDC decimation and DUC interpolation range from 2 to 65,536
- Optional GPS time and position stamping

Analog Input

Analog Output

Gigabit Ethernet
USB
PS/2 Keyboard
PS/2 Mouse
Video Output
GPS Antenna (Optional)

INTEL PROCESSOR

SYSTEM DRIVE DDR SDRAM

HOST PROCESSOR RUNNING SYSTEMFLOW

DATA DRIVES

MODEL RTV 2601

4 TB DATA STORAGE

DIGITAL DOWN-CONVERTER
Decimation: 2 to 65,536

DIGITAL UP-CONVERTER
Decimation: 2 to 65,536

200 MHz
16-bit A/D

800 MHz
16-bit D/A

Pentek, Inc.  One Park Way  Upper Saddle River, NJ 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
**Model RTV 2601**

200 MS/sec RF/IF Rackmount Value Recorder

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**SystemFlow Graphical User Interface**

The SystemFlow Graphical User Interface includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

---

**SystemFlow Recorder Interface**

The RTV 2601 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, playback a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

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**SystemFlow Hardware Configuration Interface**

The RTV 2601 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

---

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
**System Architecture**

Built on a Windows 7 Professional workstation, the RTV 2601 allows the user to install post-processing and analysis tools to operate on the recorded data. The recorder stores data in the native NTFS file system, providing immediate access to any installed Windows application. Alternately, the NTFS drive can be accessed remotely over the built-in gigabit Ethernet link from a remote Windows or Linux machine.

Recorded data can be off-loaded via the rear-panel gigabit Ethernet port, two front-panel USB 3.0 ports, two rear-panel USB 3.0 ports or four rear-panel USB 2.0 ports. A built-in DVD +/- R/RW drive allows the user to burn recorded data to disk. Hot-swappable front-panel drives can be easily removed and replaced with empty drives to provide additional data storage.

**Specifications**

**PC Workstation (standard configuration)**
- **Operating System:** Windows 7 Professional
- **Processor:** Intel Core i3 processor
- **Clock Speed:** 2.0 GHz or higher
- **SDRAM:** 8 GB
- **RAID**
  - Storage: 4 TB
  - **Number of Drives:** Six, removable, front panel access
  - **Optical Drive:** DVD+/-R/RW, front panel access
  - **USB Ports:** Front panel: 2x USB 3.0; rear panel: 2x USB 3.0, 4x USB 2.0
  - **Ethernet:** Single 1GbE, rear panel
  - **Supported RAID Levels:** 0

**Analog Recording Input**

- **Analog Signal Inputs**
  - **Input Type:** Transformer-coupled, rear-panel female SSMC connectors
  - **Transformer Type:** Coil Craft WBC4-6TLB
  - **Full Scale Input:** +8 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS5485
- **Sampling Rate** ($f_s$): 10 MHz to 200 MHz
- **Resolution:** 16 bits
- **A/D Record Bandwidth:** $f_s/2$ = Nyquist bandwidth
- **Anti-Aliasing Filter:** External, user-supplied

**Digital Downconverter**

- **Type:** Virtex-6 FPGA, Pentek DDC IP Core
- **Decimation** (D): 2 to 65,536
- **IF Center Frequency Tuning:** DC to $f_s$, 32 bits
- **DDC Usable Bandwidth:** $0.8f_s/D$

**Analog Recording Output**

- **Output Type:** Transformer-coupled, rear-panel female SSMC connector
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Digital Upconverter and D/As**

- **Interpolation:** 2 to 65,536
- **Input Data Rate:** 250 MHz max.
- **Bandwidth:** matches digital downconverter
- **Output IF:** DC to 400 MHz
- **Output Signal:** Analog, real or quadrature
- **Output Sampling Rate:** 800 MHz max. with 2, 4 or 8 interpolation
- **Resolution:** 16 bits

**Clock Sources**

- **Function:** Selectable from onboard programmable VCXO or external

**External Clocks**

- **Function:** Synthesizer reference clock (10 MHz typical) or A/D or D/A sample clock
- **Type:** Rear-panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 800 MHz

**Physical and Environmental**

- **Size:** 19” W x 22.75” D x 7” H
- **Weight:** 50 lbs
- **Operating Temp:** +5° to +35° C
- **Storage Temp:** −40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

**Model RTV 2601 Options Information**

**General Options**

- **Option -261**
  - GPS time & position stamping
- **Option -264**
  - IRIG-B time stamping

Specifications are subject to change without notice
General Information

The Talon® RTS 2706 is a turnkey, multi-band recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2706 uses 16-bit, 200 MHz A/D converters and provides sustained recording rates up to 1.6 GB/sec in four-channel configuration.

The RTS 2706 uses Pentek's high-powered Virtex-6-based Cobalt® modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 1.25 GHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

The RTS 2706 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTS 2706 allows the user to install post processing and analysis tools to operate on the recorded data. The RTS 2706 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports, six USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Flexible Architecture

The RTS 2706 is configured in a 4U 19” rack-mountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

Contact factory for options, number and type of analog channels, recording rates, and disk capacity.
SystemFlow Graphical User Interface

SystemFlow Recorder Interface
The RTS 2706 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface
The RTS 2706 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Specifications

PC Workstation (standard configuration)
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 2.0 GHz or higher
SDRAM: 6 GB
RAID
  Storage: 2–100 TB
  Supported RAID Levels: 0, 1, 5, 6, 10 and 50

Analog Recording Inputs/Outputs

Analog Signal Inputs
  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

A/D Converters
  Type: Texas Instruments ADS5485
  Sampling Rate ($f_s$): 10 MHz to 200 MHz
  Resolution: 16 bits
  A/D Record Bandwidth: $f_s/2 = \text{Nyquist bandwidth}$
  Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
  Type: Virtex-6 FPGA, Pentek DDC IP Core
  Decimation Range (D): 2 to 65,536
  IF Center Frequency Tuning: DC to $f_s$, 32 bits
  DDC Usable Bandwidth: $0.8f_s/D$ (80 MHz max)

Analog Signal Outputs
  Output Type: Transformer-coupled, front panel female SSMC connectors
  Full Scale Output: +4 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter and D/As
  Type: TI DAC5688 and Pentek-installed interpolation IP core
  Interpolation: 2 to 65,536
  Input Data Rate: 250 MHx max.
  Output IF: DC to 400 MHz
  Output Signal: Analog, real or quadrature
  Output Sampling Rate: 800 MHz max. with 2, 4 or 8 interpolation
  Resolution: 16 bits

Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clocks
  Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 200 MHz

Multi-Recorder Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Physical and Environmental
Size: 19” W x 26” D x 7” H
Weight: 60-85 lb
Operating Temp: +5° to +45° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>-201</td>
<td>1-channel recording</td>
</tr>
<tr>
<td>-202</td>
<td>2-channel recording</td>
</tr>
<tr>
<td>-203</td>
<td>3-channel recording</td>
</tr>
<tr>
<td>-204</td>
<td>4-channel recording</td>
</tr>
<tr>
<td>-208</td>
<td>8-channel recording</td>
</tr>
<tr>
<td>-221</td>
<td>1-channel playback</td>
</tr>
<tr>
<td>-222</td>
<td>2-channel playback</td>
</tr>
<tr>
<td>-224</td>
<td>4-channel playback</td>
</tr>
<tr>
<td>-228</td>
<td>8-channel playback</td>
</tr>
</tbody>
</table>

Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Storage Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>-406</td>
<td>2.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-411</td>
<td>4.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-416</td>
<td>8.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-421</td>
<td>16.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-423</td>
<td>20.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-439</td>
<td>30.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-450</td>
<td>45.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-460</td>
<td>60.0 TB HDD storage capacity</td>
</tr>
<tr>
<td>-480</td>
<td>100.0 TB HDD storage capacity</td>
</tr>
</tbody>
</table>

Note: Options -450 and -460 require a 5U Chassis; Option -480 requires a 6U Chassis

General Options (append to all options)

<table>
<thead>
<tr>
<th>Option</th>
<th>Feature</th>
</tr>
</thead>
<tbody>
<tr>
<td>-261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>-264</td>
<td>IRIG-B time stamping</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
Model RTR 2726

200 MS/sec RF/IF Rugged Portable Recorder

General Information
The Talon® RTR 2726 is a turnkey, multi-band recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726 provides aggregate recording rates of up to 2.4 GB/sec and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726 is supplied in a small footprint portable package measuring only 16.9" W x 9.5" D x 13.4" H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel® Core™ i7 processor a high-resolution 17" LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2726 are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software
Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2726 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2726 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded through two 1 Gb Ethernet ports, eight USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged & Flexible Architecture
The RTR 2726 is configured in a portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum Alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using shock- and vibration-resistant SSDs, the RTR 2726 is designed to reliably operate as a portable field instrument.

The hot-swappable SSDs provide storage capacities of up to 7.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0,1,5 and 6, provide a choice for the required level of redundancy.

Features
- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.9" W x 9.5" D x 13.4" H
- Lightweight: approximately 30 pounds
- Rugged aluminum alloy chassis
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Recording and playback of IF signals up to 700 MHz
- 80 MHz record and playback signal bandwidths
- 200 MHz 16-bit A/Ds
- 800 MHz 16-bit D/As
- SFDR >80 dBFS
- Real-time aggregate recording rates up to 2.4 GB/sec
- Up to 7.6 TB storage with hot-swap SSD drives
- NTFS file format
- SystemFlow® GUI with Signal Viewer analysis tool
- File headers include time stamping and recording parameters
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom
- Optional GPS time and position stamping
- Complete high-performance Windows® workstation

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.
➤ SystemView Graphical User Interface

![Image of SystemView Graphical User Interface]

**SystemFlow Recorder Interface**

The RTR 2726 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

![Image of SystemFlow Recorder Interface]

**SystemFlow Hardware Configuration Interface**

The RTR 2726’s Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

![Image of SystemFlow Hardware Configuration Interface]

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

➤
Specifications

PC Workstation (standard configuration)
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 2.0 GHz or higher
Operating System Drive: 128 GB SSD
SDRAM: 6 GB
Monitor: Built-in 17” high-resolution LCD
1440 x 900 pixels, 200 nits
RAID
Total Storage: 1.9, 3.8 or 7.6 TB
Supported RAID Levels: 0, 1, 5 and 6
Drive Bays: Hot-swap, removable, rear panel
USB 2.0 Ports: Eight (8) left side, two (2) front panel
USB 3.0 Ports: Two (2) left side
1 Gb Ethernet Port: One (1) left side
eSATA 3 Ports: Two (2) left side
Aux Video Output: 15-pin VGA left side

Analog Recording Inputs
Analog Signal Inputs
Quantity: 1, 2, 3, or 4
Input Type: Transformer-coupled, female SSMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz
A/D Converters
Type: Texas Instruments AD95485
  Sampling Rate (f_s): 10 MHz to 200 MHz
  Resolution: 16 bits
  A/D Record Bandwidth: f_s/2 = Nyquist bandwidth
  Anti-Aliasing Filters: External, user-supplied
Digital Downconverter
Type: Virtex-6 FPGA, Pentek DDC IP Core
  Decimation (D): 2 to 65,536
  IF Center Frequency Tuning: DC to f_s, 32 bits
  DDC Usable Bandwidth: 0.8 f_s / D
  Bandwidth Range: 2.5 kHz to 80 MHz at f_s = 200 MHz

Analog Playback Outputs
Analog Signal Outputs
Quantity: 1 or 2
Output Type: Transformer-coupled, female SSMC connectors
  Full Scale Output: +4 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz
Digital Upconverter, Interpolator and D/As
D/A Resolution: 16 bits
Output Signal: Analog, real or quadrature
Type: TI DAC5688 and Pentek-installed IP core interpolator
  IP Core Interpolation: 2 to 65,536
  DAC5688 Interpolation: 2, 4 or 8
  Overall Interpolation: 2 to 524,288
Input Data Rate to DAC5688: 250 MS/sec max.
  Output Sampling Rate: 800 MHz max
  Output IF: DC to 400 MHz
  Bandwidth Range: Matches recording bandwidths
Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clocks
Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 200 MHz

Physical and Environmental
Dimensions: 16.9” W x 9.5” D x 13.4” H
Weight: 30 lb, approximately
Power: 90 to 265 VAC, 50 - 60 Hz
Operating Temp: 0° to +50° C
Storage Temp: −40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Specifications subject to change without notice
Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information
Specifications subject to change without notice

Model RTR 2726 Ordering Information and Options

<table>
<thead>
<tr>
<th>Channel Configurations</th>
<th>Storage Options</th>
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</thead>
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<td>Option -405 1.9 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -202 2-channel recording</td>
<td>Option -410 3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -203 3-channel recording</td>
<td>Option -415 7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -204 4-channel recording</td>
<td></td>
</tr>
<tr>
<td>Option -208 8-channel recording</td>
<td></td>
</tr>
<tr>
<td>Option -221 1-channel playback</td>
<td></td>
</tr>
<tr>
<td>Option -222 2-channel playback</td>
<td></td>
</tr>
<tr>
<td>Option -224 4-Channel playback</td>
<td></td>
</tr>
<tr>
<td>Option -228 8-Channel playback</td>
<td></td>
</tr>
<tr>
<td></td>
<td>General Options (append to all options)</td>
</tr>
<tr>
<td></td>
<td>Option -261 GPS time &amp; position stamping</td>
</tr>
<tr>
<td></td>
<td>Option -264 IRIG-B time stamping</td>
</tr>
</tbody>
</table>

Specifications subject to change without notice
**General Information**

The Talon® RTR 2726A is a turnkey, multiband recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726A provides sustained recording rates of up to 3.2 GB/sec in a four-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726A is supplied in a small footprint portable package measuring only 16.0” W x 6.9” D x 13.0” H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17” LCD monitor, and up to 30.7 TB of SSD storage.

At the heart of the RTR 2726A are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

Optional GPS time and position stamping allows the user to record this critical signal information.

**SystemFlow Software**

Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

The GUI provides a very simple interface for system setup. This includes pull-down selections for a handful of parameters, a checkbox to enable/disable the DDC and a data-entry field for the sample rate. Once set up, the GUI provides the ability to save profiles that can be reloaded at the click of a button.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2726A allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2726A records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk using the 8X double-layer DVD±R/RW drive. Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

**Rugged Chassis with SSD Storage**

The RTR 2726A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

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**Features**

- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 200 MHz 16-bit A/Ds
- 800 MHz 16-bit D/A
- 80 MHz record and playback signal bandwidths
- Recording and playback of IF signals up to 700 MHz
- Real-time sustained recording rates up to 3.2 GB/sec
- Windows® workstation with high-performance Intel® Core™ i7 processor
- Up to 61 terabytes of SSD storage to NTFS RAID solid state disk array
- SystemFlow® GUI with Signal Viewer analysis tool
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Optional 10–36 VDC power supply

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.

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**Contact Information**

Pentek, Inc.
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com

www.pentek.com
Model RTR 2726A

200 MS/sec RF/IF Rugged Portable Recorder

➤ SystemView Graphical User Interface

SystemFlow Recorder Interface

The RTR 2726A GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTR 2726A’s Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Model RTR 2726A 200 MS/sec RF/IF Rugged Portable Recorder

Specifications

PC Workstation (standard configuration)
Operating System: Windows workstation
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
Operating System Drive: 128 GB SSD
SDRAM: 8 GB
Monitor: Built-in 17.3” high-resolution LCD, 1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface
Brightness: 300 cd/m²; Contrast ratio: 400:1 typical

RAID
Total Storage: 3.8 TB – 61.4 TB
Supported RAID Levels: 0, 5 and 6
Drive Bays: Hot-swap, removable, side panel
USB 2.0 Ports: Four on left side, two on front panel
USB 3.0 Ports: Two on left side
1 Gb Ethernet Ports: Two on left side
Aux Video Output: 15-pin VGA on left side

Analog Signal Inputs
Connectors: 1, 2, 3, or 4 transformer-coupled, female SSMC
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate (fₛ): 10 MHz to 200 MHz
Resolution: 16 bits
A/D Record Bandwidth: fₛ/2 = Nyquist bandwidth
Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
Type: Virtex-6 FPGA, Pentek DDC IP Core
Decimation (D): 2 to 65,536
IF Center Frequency Tuning: DC to fₛ/2, 32 bits
DCC Usable Bandwidth: 0.8×fₛ/D

Analog Signal Outputs
Connectors: 1 or 2, transformer-coupled, female SSMC
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter, Interpolator and D/A's
D/A Resolution: 16 bits
Output Signal: Analog, real or quadrature
Type: TI DAC5688 and Pentek-installed IP core interpolator
IP Core Interpolation: 2 to 65,536
DAC5688 Interpolation: 2, 4 or 8
Overall Interpolation: 2 to 524,288

Input Data Rate to DAC5688: 250 MS/sec max.
Output Sampling Rate: 800 MHz max
Output IF: DC to 400 MHz
Bandwidth Range: Matches recording bandwidths
Clock Sources: Selectable from onboard programmable VCCO, external or LVDS clocks

External Clocks
Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

Optional DC Power supply
Voltage: 10 to 36 VDC
Input Current: 42 to 26 A (39 A at 24 VDC)
Inrush Current: 100 A at 24 VDC
Temperature Range: Oper.: 0° to 50° C, Store: –0° to 80° C
Efficiency: >80% typical at 24 V full load
Power Good Signal: On delay 100 to 500 msec
OverPower Protection: 110% to 160%
Remote Control: On/Off
Safety: Meets UL, TUV, CB specifications

Physical and Environmental
Size: 16.0” W x 6.9” D x 13.0” H
Weight: 30 lb max.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing

Operating Shock: 30 g max. (11 msec, half-sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
20 to 500 Hz: 1.4 g peak acceleration
Non-operating Vibration: 5 to 500 Hz: 2.06 g RMS
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Channel Configurations
Option -201: 1-Channel Recording
Option -202: 2-Channel Recording
Option -203: 3-Channel Recording
Option -204: 4-Channel Recording
Option -208: 8-Channel Recording
Option -221: 1-Channel Playback
Option -222: 2-Channel Playback
Option -224: 4-Channel playback
Option -228: 8-Channel playback

Storage Options
Option -410: 3.8 TB SSD Storage
Option -415: 7.6 TB SSD Storage
Option -420: 15.3 TB SSD Storage
Option -430: 30.7 TB SSD Storage
Option -460: 61.4 TB SSD Storage
Option -681: 18 to 36 VDC Power Supply

Additional Options
Option -261: GPS Time and Position stamping
Option -264: IRIG-B Time stamping
Option -285: Raid 5 Configuration
Option -286: Raid 6 Configuration
Option -309: 16 GB System Memory
Option -311: 64 GB System Memory
Option -625: Removable Operating System Drive
Option -681: 10 to 36 VDC Power Supply

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTR 2746 is a turnkey, multi-band record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTR 2746 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (Solid-State Drive) storage, the RTR 2746 can be configured to stream data to and from disk at rates as high as 3.2 GB/sec.

The RTR 2746 uses Pentek’s high-powered Virtex-6-based Cobalt® boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 1.25 GHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates, and DUC interpolations are among the GUI-selectable system parameters, providing a fully programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

The RTR 2746 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2746 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2746 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded through two rear-access gigabit Ethernet ports or two USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2746 performs well in ground, shipborne and airborne environments. The hot-swap capable SSDs provide storage capacity of up to 46 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2746 is configured in a 4U 19” rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

Features

- Designed to operate under conditions of shock and vibration
- 4U 19-inch rugged rackmount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- 200 MHz max. 16-bit A/D sampling for recording, up to eight channels
- 80 MHz recording and playback signal bandwidths
- Capable of record/playback of IF frequencies to 700 MHz
- Real-time aggregate recording rates of up to 3.2 GB/sec
- Removable SSD drives
- Up to 46 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- DDC decimation and DUC interpolation range from 2 to 65,536
- Optional GPS time and position stamping

Contact factory for options, number and type of analog channels, recording rates, and disk capacity.
Model RTR 2746
200 MS/sec RF/IF Rugged Rackmount Recorder

➤ SystemFlow Graphical User Interface

The SystemFlow Graphical User Interface (GUI) includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The signal viewer, integrated into the recording GUI, also allows the user to monitor real-time signals or signals recorded on disk.

➤ SystemFlow Recorder Interface

The RTR 2746 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

➤ SystemFlow Hardware Configuration Interface

The RTR 2746 Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

➤ SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Specifications

PC Workstation (standard configuration)
- Operating System: Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 2.0 GHz or higher
- SDRAM: 6 GB
- RAID
  - Storage: 3.8, 7.6, 15.3, 30.7 or 46.0 TB
  - Supported Levels: 0, 1, 5, 6, 10 and 50

Analog Recording Inputs
- Analog Signal Inputs
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +8 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz
  - A/D Converters
    - Type: Texas Instruments ADS5485
    - Sampling Rate: 10 MHz to 200 MHz
    - Resolution: 16 bits
    - A/D Record Bandwidth: $f_s/2 = \text{Nyquist bandwidth}$
    - Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
- Type: Virtex-6 FPGA Pentek DDC IP Core
- Decimation (D): 2 to 65,536
- IF Center Frequency Tuning: DC to $f_s$, 32 bits
- DDC Usable Bandwidth: $0.8 f_s / D$

Analog Signal Outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter and D/As
- Type: TI DAC5688 and Pentek-installed interpolation IP core
- Interpolation: 2 to 65,536
- Input Data Rate: 250 MHz max.
- Output IF: DC to 400 MHz
- Output Signal: Analog, real or quadrature
- Output Sampling Rate: 800 MHz max. with 2, 4 or 8 interpolation
  - Resolution: 16 bits

Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clocks
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 200 MHz

Multi-Recorder Sync/Gate Bus: 26-pin connector, dual clock/sync/gate input/output LVDS buses; one sync/gate input TTL signal

Physical and Environmental

Dimensions
- 4U Short Chassis: 19" W x 21" D x 7" H
- Weight: 50 lb, approx.
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTR 2746 Ordering Information and Options

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<td>Option -228</td>
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<tr>
<td>8-Channel playback</td>
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</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
**Model RTX 2766**

200 MS/sec RF/IF Extreme Rackmount Recorder

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### General Information

The Talon® RTX 2766 is a turnkey, multiband record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2766 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (Solid-State Drive) storage, the RTX 2766 can be configured to stream data to and from disk at rates as high as 3.2 GB/sec.

The RTX 2766 uses Pentek’s high-powered Virtex-6-based Cobalt® boards that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

### SystemFlow Software

The RTX 2766 includes the SystemFlow® Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTX 2766 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2766 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

### Rugged Mil-Spec Chassis

The Talon RTX 2766 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.
SystemFlow Recorder Interface

The RTX 2766 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTX 2766 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Specifications

PC Workstation (standard configuration)
- Operating System: Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 3.0 GHz or higher
- SDRAM: 8 GB

Data Storage
- Style: Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
- Capacity: Up to 30.7 TB
- Number of Drives: Up to 32 total
- Supported RAID Levels: 0, 1, 5 and 6

Analog Recording Input Channels
- Connector Type: Rear-panel female SMA connectors
- Input Type: Transformer-coupled
- Full Scale Input: +6 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sample Rate \( f_s \): 10 MHz to 200 MHz
- Resolution: 16 bits
- A/D Record Bandwidth: \( f_s/2 \) = Nyquist bandwidth
- Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
- Type: Virtex-6 FPGA, Pentek DDC IP Core
- Decimation(D): 2 to 65,536
- IF Center Frequency Tuning: DC to \( f_s \), 32 bits
- DDC Usable Bandwidth: 0.8\( f_s \)/D

Sample and Reference Clocks
- External Sample Clock: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms 800 MHz or 2.5 GHz, common to all A/Ds
- VCXO Sample Clock: Programmable, up to 1.25 GHz, phase-locked to 10 MHz reference, common to all A/Ds
- Reference Clock: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 MHz, used for phase-locking the VCXO
- Connector Type: Rear panel female SMA connector for external sample or reference clock input

External Trigger
- Number: One common trigger for all input channels
- Input Level: LVTTL with selectable rising or falling edge

Model RTX 2766 Order Information and Options

<table>
<thead>
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<th>Channel Configurations</th>
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<td>Option -410</td>
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<td>1-channel recording</td>
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</tr>
<tr>
<td>Option -202</td>
<td>Option -415</td>
</tr>
<tr>
<td>2-channel recording</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -203</td>
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</tr>
<tr>
<td>3-channel recording</td>
<td>11.5 TB SSD storage capacity</td>
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<td>Option -204</td>
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<tr>
<td>4-channel recording</td>
<td>15.3 TB SSD storage capacity</td>
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<td>Option -208</td>
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<tr>
<td>8-channel recording</td>
<td>23.0 TB SSD storage capacity</td>
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<tr>
<td>Option -221</td>
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<tr>
<td>1-channel playback</td>
<td>30.7 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -222</td>
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<tr>
<td>2-channel playback</td>
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<tr>
<td>Option -224</td>
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<tr>
<td>4-channel playback</td>
<td>IRIG-B time stamping</td>
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<tr>
<td>Option -228</td>
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<tr>
<td>8-channel playback</td>
<td>28 VDC power supply</td>
</tr>
<tr>
<td></td>
<td>Option -625</td>
</tr>
<tr>
<td></td>
<td>Front-panel removable OS drive</td>
</tr>
</tbody>
</table>

Specifications are subject to change without notice

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Pentek, Inc.  One Park Way  UPPER SADDLE RIVER, NEW JERSEY 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
The Talon® RTX 2786 is a turnkey, RF/IF signal recorder designed to operate under extreme environmental conditions. Housed in a ½ ATR chassis, the RTX 2786 leverages Pentek’s 3U VPX SDR modules to provide a rugged recording system with up to four 16-bit, 200 MHz A/D converters with built-in digital downconversion capabilities.

Optionally, the RTX 2786 provides one 800 MHz, 16-bit D/A converter with a digital upconverter for signal playback or waveform generation. As shown in the block diagram below, the maximum number of record channels with this option is three.

The RTX2786 can record and play back analog signals with bandwidths ranging from a few kHz up to 80 MHz, either as baseband signals or as IF signals with center frequencies tunable across a 700 MHz range.

The RTX 2786 uses conduction cooling to draw heat from the system components allowing it to operate in reduced air environments. It includes 1.92 TB of solid-state data storage, that allows it to operate with no degradation under conditions of extreme shock and vibration. The system is hermetically sealed and provides five D38999 connectors for power and I/O. Four SMA connectors are used for analog I/O.

The recorder includes a graphical user interface for quick and simple out-of-the-box operation. It also includes a user API (Application Programming Interface) to easily integrate the system into the user’s application.

### Features
- Multiband recording and playback system
- ½ ATR 3U VPX chassis
- Designed to MIL-STD-704F, 810F and 461F
- Windows® 7 Professional workstation with high performance Intel® Core™ i7 processor
- 200 MHz 16-bit A/Ds for recording up to four channels
- 800 MHz 16-bit D/A for playback of one channel
- 80 MHz recording and playback signal bandwidths
- Capable of record/playback of IF frequencies to 700 MHz
- Real-time sustained recording rates of up to 500 MB/sec
- 1.92 TB of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5 and 6
- SystemFlow® GUI with signal viewer analysis tool which includes a virtual oscilloscope and spectrum analyzer
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.
Model RTX 2786
200 MS/sec RF/IF Extreme 3U VPX Recorder

➤ SystemFlow Graphical User Interface

![SystemFlow Graphical User Interface](image1)

SystemFlow Recorder Interface
The RTX 2786 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface
The RTX 2786 Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

![SystemFlow Hardware Configuration Interface](image2)

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

![SystemFlow Signal Viewer](image3)
Model RTX 2786
200 MS/sec RF/IF Extreme 3U VPX Recorder

Specifications

**Ruggedized Computer**

**Operating System:** Windows 7 Professional  
**Processor:** Intel Core i7 processor  
**SDRAM:** 4 GB

**I/O Connections**

**Connectors:** D38999 circular  
**Ethernet:** Dual 1 GbE  
**Serial:** Dual RS-232/422/485  
**USB:** Four USB 2.0  
**Video:** Hi-Res VGA  
**Audio:** In/Out Stereo  
**Switch:** Reboot

**RAID**

**Storage:** 1.92 TB  
**Storage Type:** Internal SSDs

**Analog Signal Input**

**Input Type:** Transformer-coupled  
**Connectors:** Bulkhead SMA female  
**Full Scale Input:** +8 dBm into 50 ohms  
**Transformer Type:** Coil Craft WBC4-6TLB  
**3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

**Type:** Texas Instruments ADS5485  
**Sample Rate (f_s):** 10 MHz to 200 MHz  
**Resolution:** 16 bits  
**A/D Record Bandwidth:** f_s/2 = Nyquist bandwidth  
**Anti-Aliasing Filters:** External, user-supplied

**Digital Downconverter**

**Type:** Virtex-6 FPGA, Pentek DDC IP Core  
**Decimation (D):** 2 to 65,536  
**IF Center Frequency Tuning:** DC to f_s, 32 bits  
**DDC Usable Bandwidth:** 0.8*f_s/D

**Analog Signal Output**

**Output Type:** Transformer-coupled  
**Connectors:** Bulkhead SMA female  
**Full Scale Output:** +4 dBm into 50 ohms  
**3 dB Passband:** 300 kHz to 700 MHz

**Digital Upconverter and D/As**

**Type:** TI DAC5688 and FPGA interpolation IP core  
**Overall Interpolation:** 2x to 524,288x in two stages of 2x to 256x and one stage of 2x, 4x, or 8x  
**Output Bandwidth:** 200 MHz maximum  
**Output IF Center Frequency:** Up to 400 MHz  
**Output Sampling Rate:** 800 MHz maximum  
**Resolution:** 16 bits

**Sample Clock Selections:**

- On-board programmable VCXO  
- External 10 MHz reference for phase-locking VCXO  
- External direct sample clock

**External Clock Input**

**Connector:** Bulkhead female SMA connector  
**Clock Input Type:** 10 MHz reference to lock VCXO or direct input sample clock  
**Clock Signal:** Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 200 MHz

**Physical and Environmental**

**Size:** 7.1” W x 16.5” D x 8.1” H  
**Weight:** 40 lb  
**Environmental:** MIL-STD-810F  
**EMC:** MIL-STD-461F - CE101, CE102, CS101, RE101, RE102, and RS101  
**Operating Temperature:** -40°C to +55°C  
**Cooling Options:** Conduction, to cold plate  
**Power Requirements:** 24 to 32 VDC, per MIL-STD-704F with 50 msec transient holdup

---

### Model RTX 2786 Order Information and Options

#### Recording/Playback Options

**Option -201**

- One-channel recording  
- One-channel playback

**Option -202**

- Two-channel recording  
- One-channel playback

**Option -203**

- Three-channel recording  
- One-channel playback

**Option -204**

- Four-channel recording  
- No playback

Contact Pentek for compatible Option combinations  
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

The Talon RTR 2750 is a turnkey recording system that provides phase-coherent recording of 16 independent input channels. Each input channel includes a 250 MHz 16-bit A/D and an FPGA-based digital down-converter with programmable decimations from 2-32768, thereby providing the ability to capture RF signals with bandwidths up to 100 MHz.

With options for AC- or DC-coupled input channels, RF signals up to 700 MHz in frequency can be sampled and streamed to disk in real-time at sustained aggregate recording rates up to 8 GB/sec in a 4U rackmount solution.

Designed to operate under conditions of vibration and extended operating temperatures, the RTR 2750 is ideal for military, airborne and field applications that require a rugged system. The hot-swappable solid state storage drives provide the highest level of performance under harsh conditions and allow for quick removal of mission-critical data.

A/D sampling rates, DDC decimations and trigger settings are among the selectable system parameters, providing a system that is simple to configure and operate.

An optional GPS time and position stamping facility allows the user to time-stamp each acquisition as well as track the location of a system in motion.

SystemFlow Software

The Talon RTR 2750 includes Pentek’s SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. User configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured setups with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor signals prior to, during, and after a recording session. These tools include a virtual oscilloscope, a virtual spectrum analyzer and a spectrogram display.

For users who wish to create a custom user interface or to integrate the Talon recording system into a larger application, a C-callable API is also provided as part of SystemFlow. Source code and examples are supplied to allow for a quick and simple integration effort.

Built on a Windows 7 Professional workstation, the RTR 2750 allows the user to install post-processing and analysis tools directly onto the recording system. The RTR 2750 records data to the native NTFS file system, providing immediate access to the recorded data; no file conversion is required.

Data can be off-loaded through rear-access gigabit Ethernet ports or USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive. Dual 10 or 40 gigabit Ethernet cards can be added to the system to provide an even faster offload facility.

Rugged and Flexible Architecture

The RTR 2750 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

The RTR 2750 includes as many as 32 hot-swappable SSDs to provide flexible storage capacities up to 61 TB. The 2.5-inch SSDs can be easily removed or exchanged during a mission to retrieve recorded data. Multiple RAID levels, including 0, 1, 5, and 6 provide a choice for the required level of redundancy.

Features

- Sixteen 250 MHz 16-bit A/Ds
- Sixteen independently-configurable DDC decimations ranging from 2 to 32768
- Sixteen independently-configurable DDC tuning frequencies
- Capable of recording RF frequencies to 700 MHz
- Capable of recording signals with bandwidths to 100 MHz
- 8 GB/s real-time aggregate recording rate
- 4U 19-inch rugged rackmount PC server chassis
- Windows 7 Professional workstation with high-performance Intel Core i7 processor
- Front panel removable-SSD drives
- Up to 61 terabytes of storage to NTFS RAID disk array
- Multiple RAID levels of 0, 1, 5 and 6
- SystemFlow GUI with signal viewer analysis tool
- Optional GPS time and position stamping

Contact factory for options, number and type of analog channels, recording rates, and disk capacity.
Model RTR 2750  
250 MS/sec RF/IF Rugged Rackmount Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Recorder Interface
The RTR 2750 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface
The RTR 2750 Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

➤

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field. ➤
Specifications

PC Workstation (standard configuration)
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 16 GB
RAID
  Storage: 15.3, 30.7 or 61.4 TB
  Supported Levels: 0, 1, 5 and 6

Analog Recording Inputs
Analog Signal Inputs
  Connector Type: Rear-panel female MMCX connectors
  Input Type: Transformer-coupled, optional DC-coupled
  Full-Scale Input: +4 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz
  Anti-Aliasing Filters: External, user-supplied
A/D Converters
  Type: Texas Instruments ADS42LB69
  Sampling Rate ($f_s$): User selectable, 10 MHz to 250 MHz
  Resolution: 16 bits
  SNR: 73.2 dBFS
  SFDR: 87 dBc (HD2 and HD3)
  100 dBc (Non HD2 and HD3)

Digital Downconverters
  Type: Virtex-7 FPGA Pentek DDC IP Core
  Decimation (D): User selectable 2 to 32768
  IF Center Frequency Tuning: User selectable, 32-bit resolution
  DDC Usable Bandwidth: 0.8*$f_s$/D, factory-supplied
  DDC coefficient tables

Clock and Trigger
A/D Clock
  Clock Sources: Selectable from onboard programmable VCM or external clocks
External Clocks
  Connector Type: Rear panel female MMCX connector
  Input Type: Transformer-coupled
  Full-scale Input: 0 to +10 dBm
Trigger
  Connector Type: Rear panel female MMCX connector
  Input Type: LVTTL

Physical and Environmental
Dimensions
  4U Short Chassis: 19” W x 21” D x 7” H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTR 2750 Ordering Information and Options

<table>
<thead>
<tr>
<th>Storage Options</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -420</td>
<td>15.3 TB SSD total storage, 960 GB per channel</td>
</tr>
<tr>
<td>Option -430</td>
<td>30.7 TB SSD total storage, 1.92 TB per channel</td>
</tr>
<tr>
<td>Option -461</td>
<td>61.4 TB SSD total storage, 3.84 TB per channel</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>General Options (append to all options)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>Option -264</td>
<td>IRIG-B time stamping</td>
</tr>
<tr>
<td>Option -004</td>
<td>D-C coupled inputs</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
**General Information**

The Talon® RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides aggregate recording rates up to 1.6 GB/sec.

The RTS 2707 uses Pentek’s high-powered Virtex-6-based Cobalt® modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

**SystemFlow Software**

The RTS 2707 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTS 2706 allows the user to install post processing and analysis tools to operate on the recorded data. The RTS 2706 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet ports or USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

**Flexible Architecture**

The RTS 2707 is configured in a 4U 19” rack-mountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

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**Features**

- Complete multiband recording and playback system
- 4U 19-inch industrial rack-mount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® CoreTM i7 processor
- 500 MHz 12-bit A/Ds or 400 MHz 14-bit A/Ds
- 800 MHz 16-bit D/A
- 80 MHz record and playback signal bandwidths
- Capable of record/playback of IF frequencies to 700 MHz
- Real-time aggregate recording rates of up to 1.6 GB/sec
- Up to 100 terabytes storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- DDC decimation and DUC interpolation range from 2 to 65,536
- Optional GPS time and position stamping

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Contact factory for options, number and type of analog channels, recording rates, and disk capacity.
SystemFlow Recorder Interface

The RTS 2707 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTS 2707 Configure screens provide a simple and intuitive means for setting up the system parameters. The input channel configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
 specifications

**PC Workstation (standard configuration)**
- **Operating System**: Windows 7 Professional
- **Processor**: Intel Core i7 processor
- **Clock Speed**: 3.0 GHz or higher
- **SDRAM**: 8 GB
- **RAID**
  - Storage: 8–100 TB
  - Supported RAID Levels: 0, 1, 5, 6, 10 and 50

**Analog Recording Inputs**
- **Analog Signal Inputs**
  - **Input Type**: Transformer-coupled, rear panel female SSMC connectors
  - **Transformer Type**: Coil Craft WBC4-6TLB
  - **Full Scale Input**: +5 dBm into 50 ohms
  - **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters**
- **Type**: Texas Instruments AD55463 or AD55474 (Option -014)
- **Sampling Rate** ($f_s$): 20 MHz to 500 MHz or 20 MHz to 400 MHz (Option -014)
- **Resolution**: 12 bits or 14 bits (Option -014)
- **A/D Record Bandwidth**: $f_s/2 = $ Nyquist bandwidth
- **Anti-Aliasing Filters**: External, user-supplied

**Digital Downconverter**
- **Type**: Virtex-6 FPGA, Pentek DDC IP Core
- **Decimation** ($D$): 2 to 65,536
- **IF Center Frequency Tuning**: DC to $f_s$, 32 bits
- **DDC Usable Bandwidth**: $0.8*f_s/D$

**Analog Playback Outputs**
- **Output Type**: Transformer-coupled, rear panel female SSMC connectors
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**Digital Upconverter and D/A**
- **Type**: TI DAC5688 and Pentek-installed interpolation IP core
- **Interpolation**: 2 to 65,536
- **Input Data Rate to DAC5688**: 250 MS/sec max.
- **Output IF**: 250 MHz max.
- **Output Sampling Rate**: 800 MHz max.
- **Resolution**: 16 bits
- **Bandwidth Range**: Matches recording bandwidths

**Clock Sources**: Selectable from onboard programmable or external clocks

**External Clock**
- **Type**: Female SSMC connector, sine wave, 0 to +12 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz divider input clock or PLL system reference

**Internal Clock**
- **Type**: Programmable VCXO from 10 to 810 MHz

**Physical and Environmental**
- **Size**: 19" W x 26" D x 7" H
- **Weight**: 60-85 lb
- **Operating Temp**: +5° to +45° C
- **Storage Temp**: –40° to +85° C
- **Relative Humidity**: 5 to 95%, non-condensing
- **Power Requirements**: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

### Model RTS 2707 Ordering Information and Options

#### Channel Configurations
- **Option -201**: 1-channel recording
- **Option -202**: 2-channel recording
- **Option -204**: 4-channel recording
- **Option -221**: 1-channel playback
- **Option -222**: 2-channel playback

#### Storage Options
- **Option -416**: 8.0 TB HDD storage capacity
- **Option -421**: 16.0 TB HDD storage capacity
- **Option -423**: 20.0 TB HDD storage capacity
- **Option -439**: 30.0 TB HDD storage capacity
- **Option -450**: 45.0 TB HDD storage capacity
- **Option -460**: 60.0 TB HDD storage capacity
- **Option -480**: 100.0 TB HDD storage capacity

**Note**: Options -450 and -460 require a 5U Chassis; Option -480 requires a 6U chassis

**General Options** (append to all options)
- **Option -014**: 400 MHz, 14-bit A/Ds
- **Option -261**: GPS time & position stamping
- **Option -264**: IRIG-B time stamping

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
**General Information**

The Talon® RTR 2727 is a turnkey, multi-band recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2727 provides aggregate recording rates of up to 2.4 GB/sec in a two-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2727 is supplied in a small footprint portable package measuring only 16.9” W x 9.5” D x 13.4” H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel® Core™ i7 processor a high-resolution 17” LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2727 are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

Optional GPS time and position stamping allows the user to record this critical signal information.

**SystemFlow Software**

Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2727 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2727 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded through two 1 Gb Ethernet ports, eight USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

**Rugged & Flexible Architecture**

The RTR 2727 is configured in a portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass.

Using shock- and vibration-resistant SSDs, the RTR 2727 is designed to operate reliably as a portable field instrument.

The hot-swappable SSDs provide storage capacities of up to 7.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0,1,5, and 6 provide a choice for the required level of redundancy.

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**Features**

- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.9” W x 9.5” D x 13.4” H
- Lightweight: approximately 30 pounds
- Rugged aluminum alloy chassis
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 500 MHz 12-bit A/Ds or 400 MHz 14-bit A/Ds
- 800 MHz 16-bit D/A
- 200 MHz recording and playback signal bandwidths
- Recording and playback of IF signals up to 700 MHz
- SFDR > 70 dBFS
- Real-time aggregate recording rates up to 2.4 GB/sec
- Up to of 7.6 TB storage with hot-swappable SSD drives
- NTFS file format
- SystemFlow® GUI with Signal Viewer analysis tool
- File headers include time stamping and recording parameters
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom
- Optional GPS time and position stamping
- Complete high-performance Windows® workstation

**Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.**
**SystemView Graphical User Interface**

The RTR 2727 GDI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, playback a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

**SystemFlow Recorder Interface**

The RTR 2727 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, playback a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

**SystemFlow Hardware Configuration Interface**

The RTR 2727’s Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Recorder Interface**

The RTR 2727's Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Model RTR 2727 500 MS/sec RF/IF Rugged Portable Recorder

Specifications

PC Workstation (standard configuration)
- Operating System: 64-bit Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 2.0 GHz or higher
- Operating System Drive: 128 GB SSD
- SDRAM: 8 GB
- Monitor: Built-in 17" high-resolution LCD (1440 x 900 pixels, 200 nits)
- RAID
  - Total Storage: 1.9, 3.8 or 7.6 TB
  - Supported RAID Levels: 0, 1, 5, and 6
  - Drive Bays: Hot-swap, removable, rear panel
- USB 2.0 Ports: Eight on left side, two on front panel
- USB 3.0 Ports: Two on left side
- 1 Gb Ethernet Port: Two on left side
- eSATA 3 Ports: Two on left side
- Aux Video Output: 15-pin VGA on left side

Analog Recording Inputs
- Analog Signal Inputs
  - Quantity: 1 or 2
  - Input Type: Transformer-coupled, female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +5 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz
- A/D Converters
  - Type: Texas Instruments ADS5463 or ADS5474 (Option -014)
  - Sampling Rate (f_s): 20 MHz to 500 MHz or 20 MHz to 400 MHz (Option -014)
  - Resolution: 12 bits or 14 bits (Option -014)
  - A/D Record Bandwidth: f_s/2 = Nyquist bandwidth
  - Anti-Aliasing Filters: External, user-supplied
- Digital Downconverter
  - Type: Virtex-6 FPGA Pentek DDC IP Core
  - Decimation (D): 2 to 65,536
  - DDC Usable Bandwidth: 0.8*f_s/D

Bandwidth Range: 5 kHz to 160 MHz at f_s = 400 MHz

Analog Playback Output
- Analog Signal Outputs
  - Quantity: 1
  - Output Type: Transformer-coupled, female SSMC connectors
  - Full Scale Output: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter and D/A
- Output Signal: Analog, real or quadrature
  - Type: TI DAC5688 and Pentek-installed interpolation IP core
- Interpolation: 2 to 65,536
- Input Data Rate to DAC5688: 250 MS/sec max.
- Output Sampling Rate: 800 MHz, max.
- Output IF: 250 MHz, max.
- D/A Resolution: 16 bits
- Bandwidth Range: Matches recording bandwidths

Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clock
- Type: Female SSMC connector, sine wave, 0 to +12 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz divider input clock or PLL system reference

Internal Clock
- Type: Programmable VCXO from 10 to 810 MHz

Physical and Environmental
- Dimensions: 16.9” W x 9.5” D x 13.4” H
- Weight: 30 lb, approximately
- Power: 90 to 265 VAC, 50 - 60 Hz
- Operating Temp: 5° to +45° C
- Storage Temp: –40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>-201</td>
<td>1-channel recording</td>
</tr>
<tr>
<td>-202</td>
<td>2-channel recording</td>
</tr>
<tr>
<td>-204</td>
<td>4-channel recording</td>
</tr>
<tr>
<td>-221</td>
<td>1-channel playback</td>
</tr>
<tr>
<td>-222</td>
<td>2-channel playback</td>
</tr>
</tbody>
</table>

Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-405</td>
<td>1.9 TB SSD storage capacity</td>
</tr>
<tr>
<td>-410</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>-415</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

General Options (append to all options)

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-014</td>
<td>400 MHz, 14-bit A/D</td>
</tr>
<tr>
<td>-261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>-264</td>
<td>IRIG-B time stamping</td>
</tr>
</tbody>
</table>

Model RTR 2727 Ordering Information and Options

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
Model RTR 2727A

500 MS/sec RF/IF Rugged Portable Recorder

General Information

The Talon® RTR 2727A is a turnkey, multi-band recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2727A provides aggregate recording rates of up to 4.0 GB/sec in a two-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2727A is supplied in a small footprint portable package measuring only 16.0" W x 6.9" D x 13.0" H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17” LCD monitor, and up to 61.4 TB of SSD storage.

At the heart of the RTR 2727A are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

The GUI provides a very simple interface for system setup. This includes pull-down selections for a handful of parameters, a checkbox to enable/disable the DDC and a data-entry field for the sample rate. Once set up, the GUI provides the ability to save profiles that can be reloaded at the click of a button.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2727A allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2727A records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double-layer DVD±R/RW drive.

Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

Rugged Chassis with SSD Storage

The RTR 2727A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 1, 5, and 6, provide a choice for the required level of redundancy.

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.

Model RTR 2727A
Model RTR 2727A
500 MS/sec RF/IF Rugged Portable Recorder

➤ SystemView Graphical User Interface

![SystemView Graphical User Interface](image1)

**SystemFlow Recorder Interface**

The RTR 2727A GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, playback a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

![SystemFlow Recorder Interface](image2)

**SystemFlow Hardware Configuration Interface**

The RTR 2727A’s Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

![SystemFlow Hardware Configuration Interface](image3)

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

![SystemFlow Signal Viewer](image4)

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

➤
Model RTR 2727A 500 MS/sec RF/IF Rugged Portable Recorder

Specifications

PC Workstation (standard configuration)
Operating System: 64-bit Windows workstation
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
Operating System Drive: 128 GB SSD
SDRAM: 8 GB
Monitor: Built-in 17.3” high-resolution LCD, 1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface
Brightness: 300 cd/m²; Contrast ratio: 400:1 typical

RAID
Total Storage: 3.8 – 60.4 TB
Supported RAID Levels: 0, 5 and 6
Drive Bays: Hot-swap, removable, side panel
USB 2.0 Ports: Four on left side, two on front panel
USB 3.0 Ports: Two on left side
1 Gb Ethernet Ports: Two on left side
Aux Video Output: 15-pin VGA on left side

Analog Signal Inputs
Connectors: 1 or 2, transformer-coupled, female SSMC
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: ±5 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5463 or ADS5474 (Option -014)
Sampling Rate (fₛ): 20 MHz to 500 MHz or 20 MHz to 400 MHz (Option -014)
Resolution: 12 bits or 14 bits (Option -014)
A/D Record Bandwidth: fₛ/2 = Nyquist bandwidth
Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
Type: Virtex-6 FPGA Pentek DDC IP Core
Decimation (D): 2 to 65,536
DDC Usable Bandwidth: 0.8*fₛ/D

Analog Signal Output
Connector: Transformer-coupled, female SSMC
Full Scale Output: ±4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter and D/A
Output Signal: Analog, real or quadrature
Type: TI DAC5688 and Pentek-installed interpolation IP core
Interpolation: 2 to 65,536
Input Data Rate to DAC5688: 250 MS/sec max.
Output Sampling Rate: 800 MHz, max.
Output IF: 250 MHz, max.
D/A Resolution: 16 bits

Bandwidth Range: Matches recording bandwidths
Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks
External Clock
Type: Female SSMC connector, sine wave, 0 to +12 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz divider input clock or PLL system reference

Internal Clock
Type: Programmable VCXO from 10 to 810 MHz

Optional DC Power supply
Voltage: 10 to 36 VDC
Input Current: 42 to 26 A (39 A at 24 VDC)
Inrush Current: 100 A at 24 VDC
Temperature Range: Oper.: 0° to 50° C, Store: –40° to 80° C
Efficiency: >80% typical at 24 V full load
Power Good Signal: On delay 100 to 500 msec
OverPower Protection: 110% to 160%
Remote Control: On/Off
Safety: Meets UL, TUV, CB specifications

Physical and Environmental
Size: 16.0” W x 6.9” D x 13.0” H
Weight: 30 lb max.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 30 g max. (11 msec, half-sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
20 to 500 Hz: 1.4 g peak acceleration
Non-operating Vibration: 5 to 500 Hz: 2.06 g RMS
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Specifications subject to change without notice
Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Model RTR 2727A Ordering Information and Options

Channel Configurations
Option -201 1-Channel Recording
Option -202 2-Channel Recording
Option -204 4-Channel Recording
Option -221 1-Channel Playback
Option -222 2-Channel Playback

Storage Options
Option -410 3.8 TB SSD Storage
Option -415 7.6 TB SSD Storage
Option -420 15.3 TB SSD Storage
Option -430 30.7 TB SSD Storage
Option -460 61.4 TB SSD Storage

Additional Options
Option -014 400 MHz, 14-bit A/Ds
Option -261 GPS Time & Position Stamping
Option -264 IRIG-B Time Stamping
Option -285 RAID 5 Configuration
Option -286 RAID 6 Configuration
Option -309 16 GB System Memory
Option -311 64 GB System Memory
Option -625 Removable Operating System Drive
Option -681 10 to 36 VDC Power Supply

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTR 2747 is a turnkey, multiband record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTR 2747 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (Solid-State Drive) storage, the RTR 2747 can be configured to stream data to and from disk at aggregate rates as high as 4.0 GB/sec.

The RTR 2747 uses Pentek’s high-powered Virtex-6-based Cobalt® boards, that provide flexibility in channel count with optional digital downconversion and upconversion capabilities.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates, and DUC interpolations are among the selectable system parameters, that provide a fully programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

The RTR 2747 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and configured and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2747 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2747 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded through two rear-access gigabit Ethernet ports or two USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2747 performs well in ground, shipborne and airborne environments. The hot-swappable SSDs provide storage capacity of up to 46 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2747 is configured in a 4U 19" rack-mountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

Features

- Designed to operate under conditions of shock and vibration
- 4U 19-inch rugged rackmount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 500 MHz 12-bit A/Ds or 400 MHz 14-bit A/Ds
- 800 MHz 16-bit D/As
- 200 MHz record and playback signal bandwidths
- Recording and playback of IF signals up to 700 MHz
- Real-time aggregate recording rates of up to 4.0 GB/sec
- Up to 46 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- NTFS file format
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Contact factory for options, number and type of analog channels, recording rates, and disk capacity.
Model RTR 2747  
500 MS/sec RF/IF Rugged Rackmount Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Recorder Interface
The RTR 2747 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface
The RTR 2747 Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field. ➤
Model RTR 2747  500 MS/sec RF/IF Rugged Rackmount Recorder

Specifications

PC Workstation (standard configuration)
- Operating System: 64-bit Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 2.0 GHz or higher
- SDRAM: 8 GB
- RAID
  - Storage: 3.8, 7.6, 15.3, 30.7 or 46 TB
  - Supported Levels: 0, 1, 5, 6, 10 and 50

Analog Recording Inputs
- Analog Signal Inputs
  - Input Type: Transformer-coupled, front panel female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +5 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments AD55463 or AD55474 (Option -014)
- Sampling Rate ($f_s$): 20 MHz to 500 MHz or 20 MHz to 400 MHz (Option -014)
- Resolution: 12 bits or 14 bits (Option -014)
- A/D Record Bandwidth: $f_s/2 = Nyquist$ bandwidth
- Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
- Type: Virtex-6 FPGA, Pentek DDC IP Core
- Decimation(D): 2 to 65,536
- IF Center Frequency Tuning: DC to $f_s/32$ bits
- DDC Usable Bandwidth: $0.8f_s/D$

Analog Playback Outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter and D/A
- Type: TI DAC5688 and Pentek-installed interpolation IP core
- Interpolation: 2 to 65,536
- Input Data Rate to DAC5688: 250 MS/sec max.
- Output IF: 250 MHz max.
- Output Signal: Analog, real or quadrature
- Output Sampling Rate: 800 MHz max.
- Resolution: 16 bits

Bandwidth Range: Matches recording bandwidth

Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clock
- Type: Female SSMC connector, sine wave, 0 to +12 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz divider input clock or PLL system reference

Internal Clock
- Type: Programmable VCXO from 10 to 810 MHz

Physical and Environmental

Dimensions
- 4U Short Chassis: 19” W x 21” D x 7” H
- Weight: 50 lb, approx.
- Operating Temp: 0° to +50° C
- Storage Temp: −40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Specifications subject to change without notice
Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Model RTR 2747 Ordering Information and Options

### Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-201</td>
<td>1-channel recording</td>
</tr>
<tr>
<td>-202</td>
<td>2-channel recording</td>
</tr>
<tr>
<td>-204</td>
<td>4-channel recording</td>
</tr>
<tr>
<td>-208</td>
<td>8-channel recording</td>
</tr>
<tr>
<td>-221</td>
<td>1-channel playback</td>
</tr>
<tr>
<td>-222</td>
<td>2-channel playback</td>
</tr>
</tbody>
</table>

### Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-410</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>-415</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>-420</td>
<td>15.3 TB SSD storage capacity</td>
</tr>
<tr>
<td>-430</td>
<td>30.7 TB SSD storage capacity</td>
</tr>
<tr>
<td>-440</td>
<td>46.0 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

Note: Options -430 and -440 require a 26-inch deep chassis

### General Options (append to all options)

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-014</td>
<td>400 MHz, 14-bit A/Ds</td>
</tr>
<tr>
<td>-261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>-264</td>
<td>IRIG-B time stamping</td>
</tr>
</tbody>
</table>

Specifications subject to change without notice

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201 818-5900  Fax: 201 818-5904  Email: info@pentek.com  www.pentek.com
**General Information**

The Talon® RTX 2767 is a turnkey, multi-band record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2767 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (Solid-State Drive) storage, the RTX 2767 can be configured to stream data to and from disk at rates as high as 4.0 GB/sec.

The RTX 2767 uses Pentek’s high-powered Virtex-6-based Cobalt® boards that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Optional GPS time and position stamping allows the user to record this critical signal information.

**SystemFlow Software**

The RTX 2767 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTX 2767 allows the user to install post processing and analysis tools to operate on the recorded data. The RTX 2767 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

**Rugged Mil-Spec Chassis**

The Talon RTX 2767 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.

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**Features**

- Designed to meet MIL-STD-810 shock and vibration
- Designed to meet EMC/EMI per MIL-STD-461 EMC
- 4U 19-inch rugged rackmount PC server chassis, 22” deep
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- 500 MHz 12-bit A/Ds or 400 MHz 14-bit A/Ds
- 800 MHz 16-bit D/A
- Real-time aggregate recording rates of up to 4.0 GB/sec
- 200 MHz max. record and playback signal bandwidths
- Capable of record/playback of IF frequencies to 700 MHz
- Up to four front-panel removable QuickPac SSD drive canisters with eight drives each
- Up to 30 terabytes of storage to NTFS RAID disk array
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

---

**Model RTX 2767**

500 MS/sec RF/IF Extreme Rackmount Recorder
SystemFlow Recorder Interface

The RTX 2767 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

SystemFlow Hardware Configuration Interface

The RTS 2767 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.
Specifications

PC Workstation (standard configuration)
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB
Data Storage
Style: Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
Location: Front panel
Capacity: Up to 30 TB
Number of Drives: Up to 32 total
Supported RAID Levels: 0, 1, 5 and 6

Analog Signal Inputs

Analog Recording Inputs
Connector Type: Rear-panel female SMA connectors
Input Type: Transformer-coupled
Full Scale Input: +5 dBM into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5463 or ADS5474 (Option -014)
Sample Rate (f_s): 20 MHz to 500 MHz or 20 MHz to 400 MHz (Option -014)
Resolution: 12 bits or 14 bits (Option -014)
A/D Record Bandwidth: f_s/2 = Nyquist bandwidth
Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
Type: Virtex-6 FPGA, Pentek DDC IP Core
Decimation (D): 2 to 65,536
IF Center Frequency Tuning: DC to f_s, 32 bits
Virtex-6 FPGA, Pentek interpolation IP core
Decimation (D): 2 to 65,536
IF Center Frequency Tuning: DC to f_s, 32 bits
D/A Converters
Type: Texas Instruments DAC5688 or DAC3484, depending on option set
Sample Rate: f_s/2 = Nyquist bandwidth
Resolution: 16 bits
A/D Record Bandwidth: f_s/2 = Nyquist bandwidth

Sample and Reference Clocks
External Sample Clock: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms 800 MHz or 1.25 GHz, common to all D/As
VCXO Sample Clock: Programmable, up to 1.25 GHz, phase-locked to 10 MHz reference, common to all D/As
Reference Clock: Sine wave, 0 to +10 dBm, A-C coupled, 50 ohms, 10 MHz, used for phase-locking the VCXO
Connector Type: Rear panel female SMA connector for external sample or reference clock input

External Trigger
Number: One common trigger for all output channels
Input Level: LVTTTL with selectable rising or falling edge
Connector Type: Rear panel female SMA connector

Physical and Environmental
Dimensions: 19” W x 22” D x 7” H
Weight: 50 lb, approx.
Operating Temp: -20° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 10% to 95%, non-condensing
Operating Shock: Designed to MIL-STD 810F, method 514.5, procedure I and VI
Operating Vibration: Designed to MIL-STD 810F, method 514.5, procedure I
EMI/EMC: Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS102, RS103
Input Power: 85 to 264 VAC, 47–400 Hz, 600 W max.

Input Level: LVTTTL with selectable rising or falling edge
Connector Type: Rear panel female SMA connector
Analog Playback Output Channels
Analog Signal Outputs
Output Type: Rear-panel female SSMC connectors
Full Scale Output: +4 dBM into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
D/A Converters
Type: Texas Instruments DAC5688 or DAC3484, depending on option set

Sample and Reference Clocks
External Sample Clock: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms 800 MHz or 1.25 GHz, common to all D/As
VCXO Sample Clock: Programmable, up to 1.25 GHz, phase-locked to 10 MHz reference, common to all D/As
Reference Clock: Sine wave, 0 to +10 dBm, A-C coupled, 50 ohms, 10 MHz, used for phase-locking the VCXO
Connector Type: Rear panel female SMA connector for external sample or reference clock input

External Trigger
Number: One common trigger for all output channels
Input Level: LVTTTL with selectable rising or falling edge
Connector Type: Rear panel female SMA connector

Specifications are subject to change without notice

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
<th>Max. Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -410</td>
<td>3.8 TB SSD storage</td>
<td>4.0 GB/sec</td>
</tr>
<tr>
<td>Option -415</td>
<td>7.6 TB SSD storage</td>
<td>4.0 GB/sec</td>
</tr>
<tr>
<td>Option -418</td>
<td>11.5 TB SSD storage</td>
<td>4.0 GB/sec</td>
</tr>
<tr>
<td>Option -420</td>
<td>15.3 TB SSD storage</td>
<td></td>
</tr>
<tr>
<td>Option -425</td>
<td>23.0 TB SSD storage</td>
<td></td>
</tr>
<tr>
<td>Option -430</td>
<td>30.7 TB SSD storage</td>
<td></td>
</tr>
</tbody>
</table>

General Options (append to all options)

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -014</td>
<td>400 MHz 14-bit A/Ds</td>
</tr>
<tr>
<td>Option -261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>Option -264</td>
<td>IRIG-B time stamping</td>
</tr>
<tr>
<td>Option -680</td>
<td>28 VDC power supply</td>
</tr>
<tr>
<td>Option -625</td>
<td>Front-panel removable OS drive</td>
</tr>
</tbody>
</table>
Model RTR 2728

General Information

The Talon® RTR 2728 is a turnkey, multi-band recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2728 provides recording rates of up to 2.4 GB/sec and is ideal for the user who requires portability and solid performance in a compact recording system.

The RTR 2728 is supplied in a small footprint portable package measuring only 16.9” W x 9.5” D x 13.4” H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17” LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2728 are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

GPS time and position stamping is optionally available.

SystemFlow Software

Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2728 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2728 records data to the native NTFS file format, providing immediate access to the recorded data.

Data can be off-loaded through two 1 Gb Ethernet ports, eight USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged & Flexible Architecture

The RTR 2728 is configured in a portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using shock- and vibration-resistant SSDs, the RTR 2728 is designed to operate reliably as a portable field instrument.

The hot-swappable SSDs provide storage capacities of up to 7.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels including 0, 1, 5, and 6 provide a choice for the required level of redundancy.

Features

- Portable system measuring 16.9” W x 9.5” D x 13.4” H
- Lightweight: approximately 30 pounds
- Rugged aluminum alloy chassis
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 1 GHz 12-bit A/D
- 1 GHz 16-bit D/A
- 400 MHz recording and playback signal bandwidths
- Recording of IF signals up to 2 GHz
- Real-time aggregate recording rates up to 2.4 GB/sec
- Up to 7.6 TB storage with hot-swappable SSD drives
- NTFS file format
- Complete high-performance Windows® workstation with Intel® Core™ i7 processor
- SystemFlow® GUI with Signal Viewer analysis tool
- File headers include time stamping and recording parameters
- Ideal for communications, radar, wireless, SIGINT, telecom and satcom
- Optional GPS time and position stamping

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.
SystemView Graphical User Interface

SystemFlow Recorder Interface

The RTR 2728 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

SystemFlow Hardware Configuration Interface

The RTR 2728’s Configure screens provide a simple and intuitive means for setting up the system parameters. The ADC configuration screen shown here, allows user entries for gate/trigger mode, gate/trigger polarity, and sync source. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. This viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Specifications

**PC Workstation (standard configuration)**
- **Operating System:** 64-bit Windows 7 Professional
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or higher
- **Operating System Drive:** 128 GB SSD
- **SDRAM:** 8 GB
- **Monitor:** Built-in 17” high-resolution LCD (1440 x 900 pixels, 200 nits)
- **RAID**
  - **Total Storage:** 1.9, 3.8 or 7.6 TB
  - **Supported RAID Levels:** 0, 1, 5, and 6
  - **Drive Bays:** Hot-swap, removable, rear panel
- **USB 2.0 Ports:** Eight on left side, two on front panel
- **USB 3.0 Ports:** Two on left side
- **1 Gb Ethernet Port:** Two on left side
- **eSATA 3 Ports:** Two on left side
- **Aux Video Output:** 15-pin VGA on left side

**Analog Recording Inputs**
- **Analog Signal Inputs**
  - **Quantity:** 1
  - **Input Type:** Transformer-coupled, female SSMC connector
  - **Transformer Type:** Macom ETC1-1-13TR
  - **Full Scale Input:** +10 dBm into 50 ohms
  - **3 dB Passband:** 5 MHz to 2 GHz
- **A/D Converter**
  - **Type:** Texas Instruments ADIS5400
  - **Sampling Rate (fs):** 100 MHz to 1 GHz
  - **Resolution:** 12 bits
  - **A/D Record Bandwidth:** fs/2 = Nyquist bandwidth
  - **Anti-Aliasing Filters:** External, user-supplied

**Analog Playback Output**
- **Analog Signal Outputs**
  - **Quantity:** 1
  - **Output Type:** Transformer-coupled, female SSMC connector
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

**D/A Converter**
- **Type:** TI DAC5681Z
- **Interpolation:** 1x, 2x or 4x
- **Input Data Rate to DAC5681Z:** 500 MS/sec max.
- **Output Sampling Rate:** 1 GHz, max.
- **Output IF:** 700 MHz, max.
- **D/A Resolution:** 16 bits

**Clock Sources:** Selectable from onboard programmable VCXO or external clock

**Physical and Environmental**
- **Dimensions:** 16.9” W x 9.5” D x 13.4” H
- **Weight:** 30 lb, approximately
- **Power:** 90 to 265 VAC, 50 - 60 Hz
- **Operating Temp:** 5° to +45° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 15 g max. (11 msec, half sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

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**Model RTR 2728 Ordering Information and Options**

<table>
<thead>
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<th>Channel Configurations</th>
<th>Storage Options</th>
</tr>
</thead>
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<td><strong>Option -405</strong></td>
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<tr>
<td>1-channel recording</td>
<td>1.9 TB SSD storage capacity</td>
</tr>
<tr>
<td><strong>Option -202</strong></td>
<td><strong>Option -410</strong></td>
</tr>
<tr>
<td>2-channel recording</td>
<td>3.8 TB SSD storage capacity</td>
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<tr>
<td><strong>Option -221</strong></td>
<td><strong>Option -415</strong></td>
</tr>
<tr>
<td>1-channel playback</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td><strong>Option -222</strong></td>
<td><strong>General Options (append to all options)</strong></td>
</tr>
<tr>
<td>2-channel playback</td>
<td><strong>Option -261</strong></td>
</tr>
<tr>
<td></td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td></td>
<td><strong>Option -264</strong></td>
</tr>
<tr>
<td></td>
<td>IRIG-B time stamping</td>
</tr>
</tbody>
</table>

**Contact Pentek for compatible Option combinations**

**Specifications subject to change without notice**
Features

- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 1 GHz 12-bit A/D
- 1 GHz 16-bit D/A
- 400 MHz recording and playback signal bandwidths
- Recording and playback of IF signals up to 2 GHz
- Real-time aggregate recording rates up to 4.0 GB/sec
- Windows® workstation with high performance Intel® Core™ i7 processor
- Up to 61 terabytes of SSD storage to NTFS RAID solid state disk array
- SystemFlow® GUI with Signal Viewer analysis tool
- Optional file headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Optional 10–36 VDC power supply

Contact the factory for options, for number and type of analog channels, recording rates, and disk capacity.

General Information

The Talon® RTR 2728A is a turnkey, multi-band recording and playback system that allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2728A provides recording rates of up to 4.0 GB/sec and is ideal for the user who requires portability and solid performance in a compact recording system.

The RTR 2728A is supplied in a small-footprint portable package measuring only 16.0” W x 6.9” D x 13.0” H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17” LCD monitor, and up to 61.4 TB of SSD storage.

At the heart of the RTR 2728A are Pentek Cobalt® Series Virtex-6 software radio boards featuring A/D and D/A converters. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

Included in this system is the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2728A allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2728A records data to the native NTFS file format, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

Rugged Chassis with SSD Storage

The RTR 2728A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.
SystemView Graphical User Interface

The Model RTR 2728A features a Graphical User Interface (GUI) that includes SystemView, which provides a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. This viewer can also be used to inspect and analyze the recorded files after the recording is complete.

SystemFlow Recorder Interface

The RTR 2728A GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

SystemFlow Hardware Configuration Interface

The RTR 2728A’s Configure screens provide a simple and intuitive means for setting up the system parameters. The ADC configuration screen shown here, allows user entries for gate/trigger mode, gate/trigger polarity, and sync source. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. This viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
### Specifications

**PC Workstation (standard configuration)**  
*Operating System:* 64-bit Windows workstation  
*Processor:* Intel Core i7 processor  
*Clock Speed:* 3.0 GHz or higher  
*Operating System Drive:* 128 GB SSD  
*SDRAM:* 8 GB  
*Monitor:* Built-in 17.3” high-resolution LCD,  
  1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface  
  Brightness: 300 cd/m²; Contrast ratio: 400:1 typical  
*RAID*  
  - **Total Storage:** 3.8 – 61.4 TB  
  - **Supported RAID Levels:** 0, 5 and 6  
*USB 2.0 Ports:* Four on left side, two on front panel  
*USB 3.0 Ports:* Two on left side  
*1 Gb Ethernet Ports:* Two on left side  
*Aux Video Output:* 15-pin VGA on left side  

### Analog Signal Input
  - **Connector:** Transformer-coupled, female SSMC  
  - **Transformer Type:** Macom ETC1-1-13TR  
  - **Full Scale Input:** +10 dBm into 50 ohms  
  - **3 dB Passband:** 5 MHz to 2 GHz  

### A/D Converter
  - **Type:** Texas Instruments ADS5400  
  - **Sampling Rate** ($f_s$): 100 MHz to 1 GHz  
  - **Resolution:** 12 bits  
  - **A/D Record Bandwidth:** $f_s/2 = \text{Nyquist bandwidth}$  
  - **Anti-Aliasing Filters:** External, user-supplied  

### Analog Signal Output
  - **Connector:** Transformer-coupled, female SSMC  
  - **Full Scale Output:** +4 dBm into 50 ohms  
  - **3 dB Passband:** 300 kHz to 700 MHz  

### D/A Converter
  - **Type:** TI DAC5681Z  
  - **Interpolation:** 1x, 2x or 4x  
  - **Input Data Rate to DAC5681Z:** 500 MS/sec max.  
  - **Output Sampling Rate:** 1 GHz, max.  
  - **Output IF:** 700 MHz, max.  
  - **D/A Resolution:** 16 bits  
  - **Clock Sources:** Selectable from onboard programmable VCXO or external clock  

### External Clock
  - **Type:** Female SSMC connector, sine wave, 0 to +10 dBm,  
  AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz input clock or 10 MHz system reference  

### Internal Clock
  - **Type:** Programmable VCXO  
  - **VCXO Frequency Ranges:** 100 to 945 MHz, 970 MHz to 1 GHz  

### Optional DC Power supply
  - **Voltage:** 10 to 36 VDC  
  - **Input Current:** 42 to 26 A (39 A at 24 VDC)  
  - **Inrush Current:** 100 A at 24 VDC  
  - **Temperature Range:** Oper.: 0° to 50° C, Store: −0° to 80° C  
  - **Efficiency:** >80% typical at 24 V full load  
  - **Power Good Signal:** On delay 100 to 500 msec  
  - **Remote Control:** On/Off  
  - **Safety:** Meets UL, TUV, CB specifications  

### Physical and Environmental
  - **Size:** 16.0” W x 6.9” D x 13.0” H  
  - **Weight:** 30 lb max.  
  - **Operating Temp:** 0° to +50° C  
  - **Storage Temp:** −40° to +85° C  
  - **Relative Humidity:** 5 to 95%, non-condensing  
  - **Operating Shock:** 30 g max. (11 msec, half-sine wave)  
  - **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak,  
  20 to 500 Hz: 1.4 g peak acceleration  
  - **Non-operating Vibration:** 5 to 500 Hz: 2.06 g RMS  
  - **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

### Model RTR 2728A Ordering Information and Options

#### Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -201</td>
<td>1-Channel Recording</td>
</tr>
<tr>
<td>Option -202</td>
<td>2-Channel Recording</td>
</tr>
<tr>
<td>Option -221</td>
<td>1-Channel Playback</td>
</tr>
<tr>
<td>Option -222</td>
<td>2-Channel Playback</td>
</tr>
</tbody>
</table>

#### Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -410</td>
<td>3.8 TB SSD Storage</td>
</tr>
<tr>
<td>Option -415</td>
<td>7.6 TB SSD Storage</td>
</tr>
<tr>
<td>Option -420</td>
<td>15.3 TB SSD Storage</td>
</tr>
<tr>
<td>Option -430</td>
<td>30.7 TB SSD Storage</td>
</tr>
<tr>
<td>Option -460</td>
<td>61.4 TB SSD Storage</td>
</tr>
</tbody>
</table>

#### Additional Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -261</td>
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<tr>
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<tr>
<td>Option -309</td>
<td>16 GB System Memory</td>
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<td>Option -311</td>
<td>64 GB System Memory</td>
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<tr>
<td>Option -625</td>
<td>Removable Operating System Drive</td>
</tr>
<tr>
<td>Option -681</td>
<td>10 to 36 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations  
Storage and Channel-count Options may change, contact Pentek for the latest information
General Information

The Talon® RTR 2748 is a turnkey recording and playback system that allows users to record and reproduce signals with bandwidths up to 500 MHz. The RTR 2748 can be configured as a one- or two-channel system to provide real-time recording and playback rates up to 4.0 GB/sec to an array of solid-state drives.

The RTR 2748 uses Pentek’s high-powered Virtex-6-based Cobalt® boards that provide the data streaming engine for the high-speed A/D converters.

A built-in synchronization module is provided to allow for multichannel phase-coherent operation.

GPS time and position stamping is optionally available.

SystemFlow Software

The RTR 2748 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Features

- Designed to operate under conditions of shock and vibration
- Recording of IF signals up to 2 GHz
- 1 GHz 12-bit A/Ds
- 1 GHz 16-bit D/A
- 400 MHz recording and playback signal bandwidths
- Real-time aggregate recording rates up to 4.0 GB/sec
- 4U 19-inch rugged rackmount PC server chassis
- Available in 21” deep 24-bay rackmount chassis or 26” deep 40-bay rackmount chassis
- Up to 46 terabytes of SSD storage to NTFS RAID solid state disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- Complete high-performance Windows® workstation with Intel® Core™ i7 processor
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Built on a Windows 7 Professional workstation, the RTR 2748 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2748 records data to the native NTFS file system that provides immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports, six USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2748 performs well in ground, shipborne and airborne environments. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Available in a 21” deep, 24-bay chassis or a 26” deep, 40-bay chassis, the system can be populated with SSD storage up to 46 TB.

The RTR 2748 is configured in a rugged rackmount chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10, and 50 provide a choice for the required level of redundancy.

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.
Model RTR 2748

1 GS/sec RF/IF Rugged Rackmount Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Recorder Interface
The RTR 2748 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface
The RTR 2748 Configure screens provide a simple and intuitive means for setting up the system parameters. The A/D configuration screen shown here, allows user entries for gate/trigger mode, gate/trigger polarity, and trigger source. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

➤
Specifications

PC Workstation (standard configuration)
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB
RAID
Storage: 3.8, 7.6, 15.3, 30.7 or 46.0 TB
Drive Type: SATA III SSDs
Supported RAID Levels: 0, 1, 5, 6, 10 and 50

Analog Recording Input
Input Type: Transformer-coupled, female SSMC connector
Transformer Type: Macom ETC1-1-13TR
Full Scale Input: +10 dBm into 50 ohms
3 dB Passband: 5 MHz to 2 GHz
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate (f_s): 100 MHz to 1 GHz
Resolution: 12 bits
A/D Record Bandwidth: f_s/2 = Nyquist bandwidth
Anti-Aliasing Filters: External, user-supplied

Analog Playback Output
Output Type: Transformer-coupled, female SSMC connector
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
D/A Converter
Type: TI DAC5681Z
Interpolation: 1x, 2x or 4x
Input Data Rate to DAC5681Z: 500 MS/sec max.
Output Sampling Rate: 1 GHz, max.
Output IF: 700 MHz, max.
D/A Resolution: 16 bits
Clock Sources: Selectable from onboard programmable VCXO or external clock
External Clock
Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz input clock or 10 MHz system reference
Internal Clock
Type: Programmable VCXO
VCXO Frequency Ranges: 100 to 945 MHz, 970 MHz to 1 GHz

Physical and Environmental
Size
Width: 19”
Height: 7”
Depth: 21” (24-drive chassis)
Depth: 26” (40-drive chassis)
Weight: 60-85 lb
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
20 to 500 Hz: 1.4 g peak acceleration
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Channel Configurations
- Option -201: 1-channel recording
- Option -202: 2-channel recording
- Option -221: 1-channel playback
- Option -222: 2-channel playback

Storage Options
- Option -410: 3.8 TB SSD storage capacity
- Option -415: 7.6 TB SSD storage capacity
- Option -420: 15.3 TB SSD storage capacity
- Option -430: 30.7 TB SSD storage capacity
- Option -440: 46.0 TB SSD storage capacity

General Options (append to all options)
- Option -261: GPS time & position stamping
- Option -264: IRIG-B time stamping

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTX 2768 is a turnkey recording and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2768 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/As and SSD (Solid-State Drive) storage, the RTX 2768 can be configured to stream data to and from disk at rates as high as 4.0 GB/sec.

The RTX 2768 uses Pentek’s high-powered Virtex-6-based Cobalt® boards that provide the data-streaming engine for the high-speed A/D and D/A converters. This system allows users to record and reproduce signals with bandwidths up to 400 MHz.

A built-in synchronization module is provided to allow for multichannel phase-coherent operation.

Optional GPS time and position stamping allows the user to record this critical signal information.

SystemFlow Software

The RTX 2768 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTX 2768 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2768 records data to the native NTFS file system that provides immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

Rugged Mil-Spec Chassis

The Talon RTX 2768 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.
SystemFlow Graphical User Interface

SystemFlow Recorder Interface

The RTX 2768 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTX 2768 Configure screens provide a simple and intuitive means for setting up the system parameters. The A/D configuration screen shown here, allows user entries for gate/trigger mode, gate/trigger polarity, and trigger source. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
## Specifications

### PC Workstation (standard configuration)
- **Operating System:** Windows 7 Professional
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or higher
- **SDRAM:** 8 GB

### Data Storage
- **Style:** Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
- **Location:** Front panel
- **Capacity:** Up to 30 TB
- **Number of Drives:** Up to 32 total
- **Supported RAID Levels:** 0, 1, 5 and 6

### Analog Recording Input Channels
- **Analog Signal Inputs**
  - **Connector Type:** Rear-panel female SMA connectors
  - **Input Type:** Transformer-coupled
  - **Full Scale Input:** +10 dBm into 50 ohms
  - **3 dB Passband:** 5 MHz to 2 GHz

### A/D Converters
- **Type:** Texas Instruments ADS5400
- **Sample Rate \( f_s \):** 100 MHz to 1 GHz
- **Resolution:** 12 bits
- **A/D Record Bandwidth:** \( f_s/2 \) = Nyquist bandwidth
- **Anti-Aliasing Filters:** External, user-supplied

### Sample and Reference Clocks
- **External Sample Clock:** Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms 100 MHz to 1 GHz, common to both A/Ds
- **VCXO Sample Clock:** Programmable, 10 to 1000 MHz, phase-locked to 10 MHz reference, common to both A/Ds
- **Reference Clock:** Sine wave, 0 to +10 dBm, A-C coupled, 50 ohms, 10 MHz, used for phase-locking the VCXO
- **Connector Type:** Rear panel female SMA connector for external sample or reference clock input

### External Trigger
- **Number:** One common trigger for both input channels
- **Input Level:** LVTTL with selectable rising or falling edge
- **Connector Type:** Rear panel female SMA connector

### Analog Playback Output Channels
- **Analog Signal Outputs**
  - **Output Type:** Rear-panel female SSMC connectors
  - **Full Scale Output:** +4 dBm into 50 ohms
  - **3 dB Passband:** 300 kHz to 700 MHz

### D/A Converters
- **Type:** Texas Instruments DAC5681Z
- **Output Sampling Rate:** 1 GHz, max.
- **Resolution:** 16 bits
- **Input Sample Data Rate:** 500 MS/sec max.
- **Output IF:** 700 MHz, max.
- **Interpolation:** 1x, 2x or 4x

### Sample and Reference Clocks
- **External Sample Clock:** Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms 100 MHz to 1 GHz, common to both A/Ds
- **VCXO Sample Clock:** Programmable, 100 to 945 MHz, 970 MHz to 1 GHz, phase-locked to 10 MHz reference, common to all D/A's
- **Reference Clock:** Sine wave, 0 to +10 dBm, A-C coupled, 50 ohms, 10 MHz, used for phase-locking the VCXO
- **Connector Type:** Rear panel female SMA connector for external sample or reference clock input

### External Trigger
- **Number:** One common trigger for both output channels
- **Input Level:** LVTTL with selectable rising or falling edge
- **Connector Type:** Rear panel female SMA connector

### Physical and Environmental
- **Dimensions:** 19” W x 22” D x 7” H
- **Weight:** 50 lb, approx.
- **Operating Temp:** –20° to +50° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 10% to 95%, non-condensing
- **Operating Shock:** Designed to MIL-STD 810F, method 514.5, procedures I and VI
- **Operating Vibration:** Designed to MIL-STD 810F, method 514.5, procedure I
- **EMI/EMC:** Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS103
- **Input Power:** 85 to 264 VAC, 47–400 Hz, 600 W max.

## Model RTX 2768 Order Information and Options

### Channel Configurations
- **Option -201:** 1-channel recording
- **Option -202:** 2-channel recording
- **Option -221:** 1-channel playback
- **Option -222:** 2-channel playback

### Storage Options
- **Option -240:** 15.3 TB SSD storage
- **Option -245:** 23.0 TB SSD storage
- **Option -240:** 30.7 TB SSD storage

### General Options (append to all options)
- **Option -261:** GPS time & position stamping
- **Option -264:** IRIG-B time stamping
- **Option -680:** 28 VDC power supply
- **Option -625:** Front-panel removable OS drive

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
**General Information**

The Talon® RTR 2729A is a turnkey system that allows users to record very high-bandwidth signals in a lightweight and rugged portable package. Equipped with a 3.6 GHz 12-bit A/D converter and user-programmable DDC (digital downconverter) the RTR 2729A is capable of capturing RF/IF signals with bandwidths as high as 360 MHz continuously for over four hours.

The RTR 2729A is supplied in a small-footprint portable package measuring only 16.0” W x 6.9” D x 13.0” H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17” LCD monitor and up to 61.4 TB of SSD storage.

The RTR 2729A uses a high-powered Pentek Virtex-7-based Onyx® board that includes a PCIe Gen. 3 engine to provide data streaming for the high-speed A/D converter. Coupled with a high-performance PCIe Gen. 3 SATA III RAID controller, the RTR 2729A is capable of streaming contiguous data to disk in real-time at rates up to 4.0 GB/sec.

The RTR 2729A can operate as a single-channel 3.6 GHz or a two-channel 1.8 GHz recorder. The channel mode operation, sample rate, DDC settings, packing modes and trigger settings are controllable via the built-in SystemFlow GUI (Graphical User Interface).

An optional GPS receiver and timing card can be added to the system to provide precise time and position stamping of the recorded data.

**SystemFlow Software**

The RTR 2729A includes Pentek’s SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

The GUI provides a very simple interface for system setup. This includes pull-down selections for a handful of parameters, a checkbox to enable/disable the DDC and a data-entry field for the sample rate. Once set up, the GUI provides the ability to save profiles that can be reloaded at the click of a button.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2729A allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2729A records data in the native NTFS file system for immediate access to the data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive. Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

**Rugged Chassis with SSD Storage**

The RTR 2729A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.
Model RTR 2729A
3.6 GS/sec Ultra Wideband RF/IF Rugged Portable Recorder

➤ SystemFlow Graphical User Interface

![SystemFlow Graphical User Interface](image1)

**SystemFlow Recorder Interface**

The RTR 2729A GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

![SystemFlow Hardware Configuration Interface](image2)

**SystemFlow Hardware Configuration Interface**

The RTR 2729A Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, sampling frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

![SystemFlow Signal Viewer](image3)

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field. ➤
Model RTR 2729A Specifications

**PC Workstation (standard configuration)**
- **Operating System:** 64-bit Windows workstation
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or higher
- **Operating System Drive:** 128 GB SSD
- **SDRAM:** 8 GB

**Monitor:**
- Built-in 17.3” high-resolution LCD,
  - 1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface
  - Brightness: 300 cd/m²; Contrast ratio: 400:1 typical

**RAID**
- **Total Storage:** 7.6 – 61.4 TB
- **Supported RAID Levels:** 0, 5 and 6
- **Drive Bays:** Hot-swap, removable, side panel
- **USB 2.0 Ports:** Four on left side, two on front panel
- **USB 3.0 Ports:** Two on left side
- **1 Gb Ethernet Ports:** Two on left side
- **Aux. Video Output:** 15-pin VGA on left side

**Analog Signal Inputs**
- **Connectors:** Two side panel SSMC connectors, In 1 & In 2
- **Input Type:** Single-ended, non-inverting
- **Full Scale Input:** +4 dBm into 50 ohms
- **Coupling:** Transformer-coupled
- **Input Transformers**
- **Bandwidth:** 4.5 kHz to 3.0 GHz

**A/D Converters**
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate**
  - Single-channel mode: 500 MHz to 3.6 GHz
  - Dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Maximum Usable Input Frequency**
  - Single-channel mode: 1.75 GHz
  - Dual-channel mode: 2.8 GHz
- **Anti-Aliasing Filters:** External, user-supplied

**Digital Downconverters**
- **Modes:** One or two channels, programmable
- **Supported Sample Rate (f_s):**
  - One-channel mode: 3.6 GHz
  - Two-channel mode: 1.8 GHz
- **Decimation Range (D):**
  - One-channel mode: 8x, 16x, 32x, bypass
  - Two-channel mode: 4x, 8x, 16x, bypass
- **DDC Usable Bandwidth:** 0.8* f_s / D

**Sampling Clock Source:**
- Internal fixed-frequency or programmable oscillator (selectable by option);
  - in single-channel mode, the sample rate is 2x the clock frequency;
  - in dual-channel mode, the sample rate equals the clock frequency

**Frequency Reference:** Accepts external 10 MHz reference at 0 to +4 dBm to phase-lock the clock oscillator

**Optional DC Power supply**
- **Voltage:** 10 to 36 VDC
- **Input Current:** 42 to 26 A (39 A at 24 VDC)
- **Inrush Current:** 100 A at 24 VDC
- **Temperature Range:** Oper.: 0° to 50° C, Store: -0° to 80° C
- **Efficiency:** >80% typical at 24 V full load
- **OverPower Protection:** 110% to 160%
- **Remote Control:** On/Off

**Physical and Environmental**
- **Size:** 16.0” W x 6.9” D x 13.0” H
- **Weight:** 30 lb max.
- **Operating Temp:** 0° to +50° C
- **Storage Temp:** -40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 30 g max. (11 msec, half-sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
- **Non-operating Vibration:** 5 to 500 Hz: 2.06 g RMS
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

**Sample Clock Options**
- **Option -910** User-Programmable Sample Clock
- **Option -911** 1.5 / 3.0 GHz sample clock
- **Option -912** 1.6 / 3.2 GHz sample clock
- **Option -915** 1.8 / 3.6 GHz sample clock
- **Note:** Custom fixed-frequency sample clocks available upon request.

**Storage Options**
- **Option -415** 7.6 TB SSD Storage
- **Option -420** 15.3 TB SSD Storage
- **Option -430** 30.7 TB SSD Storage
- **Option -460** 61.4 TB SSD Storage

**Addition Options**
- **Option -261** GPS Time & Position Stamping
- **Option -264** IRIG-B Time Stamping
- **Option -285** RAID 5 Configuration
- **Option -286** RAID 6 Configuration
- **Option -309** 16 GB System Memory
- **Option -311** 64 GB System Memory
- **Option -625** Removable Operating System Drive
- **Option -681** 10 to 36 VDC Power Supply

**Contact Pentek for compatible Option combinations**

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information
The Talon® RTR 2749 is a turnkey system, used for recording high-bandwidth signals. The RTR 2749 uses 12-bit, 3.6 GHz A/D converters. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit- or 16-bit-wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word). A high-speed RAID array provides a maximum streaming recording rate to disk of 4.8 GB/sec.

The RTR 2749 uses Pentek’s high-powered Virtex-7-based Onyx® boards that provide the data streaming engine for the high-speed A/D converters. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system.

Optional GPS time and position stamping allows the user to capture this critical information in the header of each data file.

SystemFlow Software
The RTR 2749 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope and a virtual spectrum analyzer.

Built on a Windows 7 Professional workstation, the RTR 2749 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2749 records data to the native NTFS file system that provides immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports, six USB 2.0 ports or two eSATA ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture
Because SSDs operate reliably under conditions of vibration and shock, the RTR 2749 performs well in ground, shipborne and airborne environments. The hot-swappable SSDs provide storage capacity of up to 46 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2749 is configured in a 4U 19” rugged rackmount chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50 provide a choice for the required level of redundancy.

Contact factory for options, for number and type of analog channels, recording rates, and disk capacity.

Model RTR 2749
3.6 GS/sec Ultra Wideband RF/IF Rugged Rackmount Recorder

Features
- Designed to operate under conditions of shock and vibration
- Sample rates up to 3.6 GHz in single-channel mode
- Sample rates up to 1.8 GHz in dual-channel mode
- Capable of recording RF/IF frequencies to 1.75 GHz in single-channel mode
- Capable of recording RF/IF frequencies to 2.8 GHz in dual-channel mode
- 12-bit A/D, with 16- and 8-bit packing modes
- Real-time aggregate recording rates of up to 4.8 GB/sec
- 4U 19-inch rugged rackmount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- Up to 46 terabytes of SSD storage to NTFS RAID solid state disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- N+1 redundant power supply
- SystemFlow® GUI with signal viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
Model RTR 2749  
3.6 GS/sec Ultra Wideband RF/IF Rugged Rackmount Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Recorder Interface

The RTR 2749 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTR 2749 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, sampling frequency, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

➤ SystemFlow Signal Viewer

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Model RTR 2749 Specifications

PC Workstation (standard configuration)
- Operating System: Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 2.0 GHz or higher
- SDRAM: 8 GB
- RAID
  - Storage: 7.6, 15.3, 30.7 or 46.0 TB
  - Drive Type: SATA III SSDs
  - Supported RAID Levels: 0, 1, 5, 6, 10 and 50

Analog Signal Inputs
- Connectors: Two rear panel SSMC connectors, In 1 & In 2
- Input Type: Single-ended, non-inverting
- Full Scale Input: +4 dBm into 50 ohms
- Coupling: Transformer-coupled
- Analog Input Transformers
- Bandwidth: 4.5 kHz to 3.0 GHz

A/D Converters
- Type: Texas Instruments ADC12D1800
- Sampling Rate:
  - Single-channel mode: 500 MHz to 3.6 GHz
  - Dual-channel mode: 150 MHz to 1.8 GHz
- Resolution: 12 bits
- Maximum Usable Input Frequency
  - Single-channel mode: 1.75 GHz
  - Dual-channel mode: 2.8 GHz
- Anti-Aliasing Filters: External, user-supplied

Digital Downconverters
- Modes: One or two channels, programmable
- Supported Sample Rate ($f_s$):
  - One-channel mode: 3.6 GHz
  - Two-channel mode: 1.8 GHz
- Decimation Range ($D$):
  - One-channel mode: 8x, 16x, 32x, bypass
  - Two-channel mode: 4x, 8x, 16x, bypass
- Usable Output Bandwidth: $0.8f_s/D$
- Sampling Clock Source: Internal fixed-frequency or programmable oscillator (selectable by option);
  in single-channel mode, the sample rate is 2x the clock frequency;
  in dual-channel mode, the sample rate equals the clock frequency
- Frequency Reference: Accepts external 10 MHz reference at
  0 to +4 dBm to phase-lock the clock oscillator

Physical and Environmental
- Size: 19” W x 26” D x 7” H
- Weight: 60-85 lb
- Operating Temp: 0° to +50° C
- Storage Temp: –40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Sample Clock Options

<table>
<thead>
<tr>
<th>Option  -910</th>
<th>User-Programmable Sample Clock</th>
</tr>
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<tbody>
<tr>
<td></td>
<td>Dual-channel mode sample clock range</td>
</tr>
<tr>
<td></td>
<td>150 MHz – 945 MHz</td>
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<tr>
<td></td>
<td>970 MHz – 1134 MHz</td>
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<td>1213 MHz – 1417.5 MHz</td>
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<tr>
<td></td>
<td>Single-channel mode sample clock range</td>
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<td></td>
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</thead>
<tbody>
<tr>
<td></td>
<td>1.6 / 3.2 GHz sample clock</td>
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</table>

Custom fixed-frequency sample clocks available upon request.

Storage Options

<table>
<thead>
<tr>
<th>Option  -415</th>
<th>7.6 TB SSD storage capacity</th>
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</thead>
<tbody>
<tr>
<td>Option  -420</td>
<td>15.3 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option  -430</td>
<td>30.7 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option  -440</td>
<td>46.0 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

Note: Options -430 and 440 require a 26-inch deep chassis

General Options (append to all options)

<table>
<thead>
<tr>
<th>Option  -261</th>
<th>GPS time &amp; position stamping</th>
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</thead>
<tbody>
<tr>
<td>Option  -264</td>
<td>IRIG-B time stamping</td>
</tr>
</tbody>
</table>

Model RTR 2749 Ordering Information and Options

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
Model RTX 2769  
3.6 GS/sec Ultra Wideband Extreme Rackmount Recorder

➤ SystemFlow Graphical User Interface

![SystemFlow Graphical User Interface](image)

The RTX 2769 GUI provides the user with a control interface for the recording system. It includes Configuration, Record and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Recorder Interface

The RTX 2769 GUI provides the user with a control interface for the recording system. It includes Configuration, Record and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTX 2769 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, sampling frequency, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Recorder Interface

The RTX 2769 GUI provides the user with a control interface for the recording system. It includes Configuration, Record and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.
Specifications

PC Workstation (standard configuration)
- **Operating System:** Windows 7 Professional
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or higher
- **SDRAM:** 8 GB

Data Storage
- **Style:** Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
- **Location:** Front panel
- **Capacity:** Up to 61 TB
- **Number of Drives:** Up to 32 total
- **Supported RAID Levels:** 0, 1, 5 and 6

Analog Recording Input Channels

Analog Signal Inputs
- **Connector Type:** Rear-panel female SMA connectors
- **Input Type:** Transformer-coupled
- **Full Scale Input:** +4 dBm into 50 ohms
- **Input Transformers**
  - **3 dB Passband:** 4.5 kHz to 3.0 GHz

A/D Converters
- **Type:** Texas Instruments ADC12D1800
- **Sampling Rate:**
  - Single-channel mode: 500 MHz to 3.6 GHz
  - Dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution:** 12 bits
- **Maximum Usable Input Frequency**
  - Single-channel mode: 1.75 GHz
  - Dual-channel mode: 2.8 GHz
- **Full Scale Input:** +2 dBm to +4 dBm, programmable

Digital Downconverters
- **Modes:** One or two channels, programmable
- **Supported Sample Rate ($f_s$):**
  - One-channel mode: 3.6 GHz
  - Two-channel mode: 1.8 GHz
- **Decimation Range (D):**
  - One-channel mode: 8x, 16x, 32x, bypass
  - Two-channel mode: 4x, 8x, 16x, bypass
- **DDC Usable Bandwidth:** $0.8 \times f_s / D$

Sample and Reference Clocks
- **Sample Clock Source:** Internal fixed-frequency or programmable oscillator (selectable by Option number); in single-channel mode, the sample rate is $2x$ the clock frequency; in dual-channel mode, the sample rate equals the clock frequency
- **Reference Clock:** External 10 MHz reference at 0 to +4 dBm to phase-lock the clock oscillator
- **Connector Type:** Rear-panel female SMA connector

External Trigger
- **Number:** One common trigger for both channels
- **Input Level:** LVTTL with selectable rising or falling edge
- **Connector Type:** Rear-panel female SMA connector

Physical and Environmental
- **Dimensions:** 19" W x 22” D x 7” H
- **Weight:** 50 lb, approx.
- **Operating Temp:** -20° to +50° C
- **Storage Temp:** -40° to +85° C
- **Relative Humidity:** 10% to 95%, non-condensing
- **Operating Shock:** Designed to MIL-STD 810F, method 514.5, procedures I and VI
- **Operating Vibration:** Designed to MIL-STD 810F, method 514.5, procedure I
- **EMI/EMC:** Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS103
- **Input Power:** 85 to 264 VAC, 47– 400 Hz, 600 W max.

Model RTX 2769 Order Information and Options

Sample Clock Options

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<td>1.6 / 3.2 GHz sample clock</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option -915</th>
<th>Fixed-frequency clock</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1.8 / 3.6 GHz sample clock</td>
</tr>
</tbody>
</table>

Sample rates are set up for dual-channel mode first and single-channel mode second: e.g. 1.5 / 3.0 is 1.5 in dual-channel mode and 3.0 in single-channel mode.

Storage Options

<table>
<thead>
<tr>
<th>Option -410</th>
<th>3.8 TB SSD storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -415</td>
<td>7.6 TB SSD storage</td>
</tr>
<tr>
<td>Option -420</td>
<td>15.3 TB SSD storage</td>
</tr>
<tr>
<td>Option -430</td>
<td>30.7 TB SSD storage</td>
</tr>
<tr>
<td>Option -460</td>
<td>61.0 TB SSD storage</td>
</tr>
</tbody>
</table>

General Options

<table>
<thead>
<tr>
<th>Option -261</th>
<th>GPS time &amp; position stamping</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -264</td>
<td>IRIG-B time stamping</td>
</tr>
<tr>
<td>Option -680</td>
<td>28 VDC power supply</td>
</tr>
<tr>
<td>Option -625</td>
<td>Front-panel removable OS drive</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
**General Information**

The Talon® RTR 2613 combines Pentek’s Sentinel Intelligent Signal Scanning software with real-time recording in a lightweight, portable and rugged package. The RTR 2613 provides SIGINT engineers the ability to scan the 3 GHz spectrum for signals of interest and monitor or record bandwidths up to 40 MHz wide once a signal band of interest is detected.

A spectral scan facility allows the user to sweep the spectrum at 30 GHz/sec, while threshold detection allows the system to automatically lock onto and record signal bands. Scan results are displayed in a waterfall plot and can also be recorded to allow users to look back at some earlier spectral activity.

Once a signal of interest is detected, the real-time recorder can capture and store up to 61.4 terabytes of data to disk, allowing users to store days’-worth of data.

**Hardware Features**

The Pentek Model 78621 Cobalt board transceiver serves as the engine of the RTR 2613 and is coupled with a 3 GHz tuner to provide excellent dynamic range across the entire spectrum. The 200 MHz 16-bit A/D board provides 86 dB of spurious-free dynamic range and 75 dB of SNR.

The FPGA-based DDC with selectable decimations up to 64 k provides exceptional processing gain while allowing users to zoom into communications signals of varying bandwidths.

The RTR 2613 is supplied in a small footprint portable package measuring only 16.0” W x 6.9” D x 13.0” H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17 in. LCD monitor, and up to 61.4 TB of SSD storage.

An optional GPS receiver and built-in PLLs allow all devices in the RF chain to be locked in phase and correlated to GPS time. GPS position information can optionally be recorded, allowing the recorder’s position to be tracked while acquiring RF signals.

**Sentinel Features**

Pentek’s Sentinel™ recorders add intelligent signal monitoring and detection for Talon real-time recording systems. The intuitive GUI allows users to monitor the entire spectrum or select a region of interest, while a selectable resolution bandwidth allows the user to trade sweep rate for a finer resolution and better dynamic range. Scan settings can be saved as profiles to allow for quick setup in the field.

RF energy in each band of the scan is detected and presented in a waterfall display. Any RF band can be selected for real-time monitoring or recording. In addition to manually selecting a band for recording, a recording can be automatically started by configuring signal strength threshold levels to trigger a recording.

The Sentinel hardware resources are controlled through enhancements to Talon’s SystemFlow™ software package that includes a virtual oscilloscope, virtual spectrum analyzer and spectrogram displays. These provide a complete suite of analysis tools to compliment the Sentinel hardware resources.

---

**New! New! New! New! New!**

- Search and capture system using Pentek’s Sentinel™ Intelligent Signal Scanner
- Captures RF signals up to 3 GHz
- Capture and scan bandwidths up to 40 MHz
- 30 GHz/sec scan rate
- Selectable threshold triggered or manual record modes
- 16-bit A/D with 75 dB SNR & 86 dB SFDR
- Built-in DDC with selectable decimation range from 2 to 65,536
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Storage capacities to 61.4 TB
- RAID levels 0, 5, and 6
- Windows® workstation with Intel Core™ i7 processor
- Optional RF upconversion
- SystemFlow GUI with virtual oscilloscope, spectrum analyzer and spectrogram displays
Graphical User Interface

RF Scanner GUI
An RF Scanner GUI allows complete control of the system through a single interface. Start and stop frequencies of a scan can be set by the user as well as the resolution bandwidth. All user parameters can be saved as profiles for easy setup in the field.

SystemFlow Recorder Interface
The RTR 2613 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and playback a recorded signal. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion).
Model RTR 2613

Talon 3 GHz RF/IF Sentinel Intelligent Signal Scanning Portable Recorder

➤ SystemFlow Software

The RTR 2613 includes the SystemFlow® Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows workstation, the RTR 2613 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2613 records data to the native NTFS file system providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet ports or USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Specifications

RF Tuner Specifications

RF Tuner Frequency Range: 30 to 3000 MHz
Tuning resolution: 1 kHz
Internal frequency accuracy: ±1.0 ppm (-20 to +60°C)
External Reference Input Frequency: 10 MHz
External Reference Input Level: 0 dBm ±3 dBm
RF input: 50 ohms nominal
Noise figure: 13 dB typical, 16 dB max
Maximum RF input without damage: +15 dBm
In-Band Input IP3: +3 dBm typical, -3 dBm min
In-Band Input IP2: +30 dBm min, +36 dBm typical
IF bandwidth: Nominal 40 MHz bandwidth (3 dB)

IF center frequency: 70 MHz center
Gain: +15 dB nominal above RF input
Gain control: Manual –40 dB range (min)
Image rejection: 65 dB min (> 80 dB typical)
IF rejection: 65 dB min (80 dB typical)
Phase noise at 2.500 MHz:
  1 kHz offset: –75 dBc/Hz typical
  20 kHz offset: –80 dBc/Hz max
  100 kHz offset: –100 dBc/Hz typical
  1 MHz offset: –125 dBc/Hz typical
Internally generated spurious: –100 dBm equivalent RF input typical

Specifications continued on next page ➤
Model RTR 2613

Talon 3 GHz RF/IF Sentinel Intelligent Signal Scanning Portable Recorder

**PC Workstation Specifications**
- **Operating System:** Windows workstation
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.2 GHz or higher
- **SDRAM:** 8 GB
- **RAID:**
  - Storage: 480 GB – 61.4 TB
  - Supported RAID Levels: 0, 5 and 6

**A/D Converter Specifications**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits
- **SNR:** 75 dBf typical at 70 MHz
- **SFDR:** 86 dBc typical at 70 MHz
- **2nd Harmonic:** 95 dBc typical at 70 MHz
- **3rd Harmonic:** 87 dBc typical at 70 MHz
- **Next Worst Harmonic/Spurious:** 90 dBc typical at 70 MHz
- **THD:** 85 dBc typical at 70 MHz
- **SINAD:** 73.7 dBc typical at 70 MHz
- **ENOB:** 12.1 bits typical at 10 MHz

**Digital Downconverter IP Core Specifications**
- **Decimation Range:** 2 to 64 k in two programmable stages of 2 to 256
- **LO Tuning Frequency Resolution:** 32 bits, 0 to \( f_s \)
- **LO SFDR:** >120 dB
- **FIR Filter:** 16-bit coefficients, 24-bit output with user programmable coefficients
- **Default Filter Set:** 80% bandwidth, <0.3 dB passband ripple >100 dB stopband attenuation

**Optional DC Power supply**
- **Voltage:** 10 to 36 VDC
- **Input Current:** 42 to 26 A (39 A at 24 VDC)
- **Inrush Current:** 100 A at 24 VDC
- **Temperature Range:** Oper.: 0° to 50° C, Store: -40° to 80° C
- **Efficiency:** >80% typical at 24 V full load
- **Power Good Signal:** On delay 100 to 500 msec
- **OverPower Protection:** 110% to 160%
- **Remote Control:** On/Off
- **Safety:** Meets UL, TUV, CB specifications

**Physical and Environmental Specifications**
- **Dimensions:** Height: 13.0”
  - Width: 16.0”
  - Depth: 6.9”
- **Weight:** 30 lb max.
- **Operating Temperature:** 0 to +50 deg C
- **Storage Temperature:** -40 to +85 deg C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 30 g max. (11 msec, half-sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak,
  - 20 to 500 Hz: 1.4 g peak acceleration
- **Non-operating Vibration:** 5 to 500 Hz: 2.06 g RMS
- **Power Requirements:** 100 to 240 VAC, 50-60 Hz, ~500 W max.

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**Model RTR 2613 Ordering Information and Options**

<table>
<thead>
<tr>
<th>General Options</th>
<th>Storage Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -261</td>
<td>Option -402: 480 GB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -264</td>
<td>Option -410: 3.8 TB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -285</td>
<td>Option -415: 7.6 TB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -286</td>
<td>Option -420: 15.3 TB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -309</td>
<td>Option -430: 30.7 TB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -311</td>
<td>Option -460: 61.4 TB SSD Storage Capacity</td>
</tr>
<tr>
<td>Option -625</td>
<td>Removable Operating System Drive</td>
</tr>
<tr>
<td>Option -681</td>
<td>10 to 36 VDC Power Supply</td>
</tr>
</tbody>
</table>

**Contact Pentek for compatible Option combinations**

Storage and General Options may change, contact Pentek for the latest information

*Specifications subject to change without notice*
Model RTR 2623

Talon 6 GHz RF/IF Sentinel Intelligent Signal Scanning Portable Recorder

General Information

The Talon® RTR 2623 combines Pentek’s Sentinel Intelligent Signal Scanning software with real-time recording in a lightweight, portable and rugged package. The RTR 2623 provides SIGINT engineers the ability to scan the 6 GHz spectrum for signals of interest and monitor or record bandwidths up to 40 MHz wide once a signal band of interest is detected.

A spectral scan facility allows the user to sweep the spectrum at 30 GHz/sec, while threshold detection allows the system to automatically lock onto and record signal bands. Scan results are displayed in a waterfall plot and can also be recorded to allow users to look back at some earlier spectral activity.

Once a signal of interest is detected, the real-time recorder can capture and store up to 30 terabytes of data to disk, allowing users to store days worth of data.

Hardware Features

The Pentek Model 78621 Cobalt board transceiver serves as the engine of the RTR 2623 and is coupled with a 6 GHz tuner to provide excellent dynamic range across the entire spectrum. The 200 MHz 16-bit A/D board provides 86 dB of spurious-free dynamic range and 74 dB of SNR.

The Virtex-6-based DDC with selectable decimations up to 64 k provides exceptional processing gain while allowing users to zoom into communications signals of varying bandwidths.

The RTR 2623 is supplied in a small footprint portable package measuring only 16.0” W x 6.9” D x 13.0” H and weighing just less than 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor a high-resolution 17 in. LCD monitor, and up to 61.4 TB of SSD storage.

An optional GPS receiver and built-in PLLs allow all devices in the RF chain to be locked in phase and correlated to GPS time. GPS position information can optionally be recorded, allowing the recorder’s position to be tracked while acquiring RF signals.

Sentinel Features

Pentek’s Sentinel™ recorders add intelligent signal monitoring and detection for Talon real-time recording systems. The intuitive GUI allows users to monitor the entire spectrum or select a region of interest, while a selectable resolution bandwidth allows the user to trade sweep rate for a finer resolution and better dynamic range. Scan settings can be saved as profiles to allow for quick setup in the field.

RF energy in each band of the scan is detected and presented in a waterfall display. Any RF band can be selected for real-time monitoring or recording. In addition to manually selecting a band for recording, a recording can be automatically started by configuring signal strength threshold levels to trigger a recording.

The Sentinel hardware resources are controlled through enhancements to Talon’s SystemFlow® software package that includes a Virtual Oscilloscope, Virtual Spectrum Analyzer and Spectrogram displays. These provide a complete suite of analysis tools to compliment the Sentinel hardware resources.

Features

- Search and capture system using Pentek’s Sentinel™ Intelligent Signal Scanner
- Captures RF signals up to 6 GHz
- Capture and scan bandwidths up to 40 MHz
- 30 GHz/sec scan rate
- Selectable threshold triggered or manual record modes
- 16-bit A/D with 75 dB SNR & 87 dB SFDR
- Built-in DDC with selectable decimation range from 2 to 65,536
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Storage capacities to 61 TB
- RAID levels 0, 5, and 6
- Windows workstation with Intel Core™ i7 processor
- Optional RF upconversion
- SystemFlow GUI with virtual Oscilloscope, Spectrum Analyzer and Spectrogram displays
Model RTR 2623
Talon 6 GHz RF/IF Sentinel Intelligent Signal Scanning
Portable Recorder

➤ Graphical User Interface

RF Scanner GUI
An RF Scanner GUI allows complete control of the system through a single interface. Start and stop frequencies of a scan can be set by the user as well as the resolution bandwidth. All user parameters can be saved as profiles for easy setup in the field.

SystemFlow Recorder Interface
The RTR 2623 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded signal. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion).
SystemFlow Software
The RTR 2623 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools, that allow the user to monitor the signal prior to, during, and after a recording session. These tools include virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows 7 Professional workstation, the RTR 2623 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2623 records data to the native NTFS file system providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet ports or USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Specifications

RF Tuner Specifications

RF Tuner Frequency Range: 30 to 6000 MHz  
Tuning resolution: 1 kHz  
Internal frequency accuracy: ±1.0 ppm (-20 to +60°C)  
External Reference Input Frequency: 10 MHz  
External Reference Input Level: 0 dBm ±3 dBm  
RF input: 50 ohms nominal  
Noise figure: 13 dB typical, 16 dB max  
Maximum RF input without damage: +15 dBm  
In-Band Input IP3: +3 dBm typical, -3 dBm min  
In-Band Input IP2: +30 dBm min, +36 dBm typical  
IF bandwidth: Nominal 40 MHz bandwidth (3dB)  

IF center frequency: 70 MHz center  
Gain: +15 dB nominal above RF input  
Gain control: Manual –40 dB range (min)  
Image rejection: 65 dB min (> 80 dB typical)  
IF rejection: 65 dB min (80 dB typical)  
Phase noise at 5000 MHz:  
1 kHz offset: –75 dBc/Hz typical  
20 kHz offset: –80 dBc/Hz max  
100 kHz offset: –100 dBc/Hz typical  
1 MHz offset: –125 dBc/Hz typical  
Internally generated spurious: –100 dBm equivalent RF input typical
Model RTR 2623

Talon 6 GHz RF/IF Sentinel Intelligent Signal Scanning
Portable Recorder

PC Workstation Specifications
- Operating System: Windows workstation
- Processor: Intel Core i7 processor
- Clock Speed: 3.2 GHz or higher
- SDRAM: 8 GB
- RAID:
  - Storage: 1.9 - 61.4 TB
  - Supported RAID Levels: 0, 5 and 6

A/D Converter Specifications
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits
- SNR: 75 dBf typical at 70 MHz
- SFDR: 87 dBc typical at 70 MHz
- 2nd Harmonic: 95 dBc typical at 70 MHz
- 3rd Harmonic: 87 dBc typical at 70 MHz
- Next Worst Harmonic/Spurious: 90 dBc typical at 70 MHz
- THD: 85 dBc typical at 70 MHz
- SINAD: 73.7 dBc typical at 70 MHz
- ENOB: 12.1 bits typical at 10 MHz

Digital Downconverter IP Core Specifications
- Decimation Range: 2 to 64 k in two programmable stages of 2 to 256
- LO Tuning Frequency Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- FIR Filter: 16-bit coefficients, 24-bit output with user programmable coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple >100 dB stopband attenuation

Optional DC Power Supply
- Voltage: 10 to 36 VDC
- Input Current: 42 to 26 A (39 A at 24 VDC)
- Inrush Current: 100 A at 24 VDC
- Temperature Range: Oper.: 0° to 50° C, Store: -0° to 80° C
- Efficiency: >80% typical at 24 V full load
- Power Good Signal: On delay 100 to 500 msec
- OverPower Protection: 110% to 160%
- Remote Control: On/Off
- Safety: Meets UL, TUV, CB specifications

Physical and Environmental Specifications
- Dimensions: Height: 13.0”
  Width: 16.0”
  Depth: 6.9”
- Weight: 30 lb max,
- Operating Temperature: 0 to +50 deg C
- Storage Temperature: -40 to +85 deg C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 30 g max. (11 msec, half-sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
- Non-operating Vibration: 5 to 500 Hz: 2.06 g RMS
- Power Requirements: 100 to 240 VAC, 50-60 Hz, ~500 W max.

Model RTR 2623 Ordering Information and Options

<table>
<thead>
<tr>
<th>General Options</th>
<th>Storage Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -261</td>
<td>Option -405 1.9 TB HDD Storage Capacity</td>
</tr>
<tr>
<td>Option -264</td>
<td>Option -410 3.8 TB HDD Storage Capacity</td>
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<tr>
<td>Option -285</td>
<td>Option -415 7.6 TB HDD Storage Capacity</td>
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<tr>
<td>Option -286</td>
<td>Option -420 15.3 TB HDD Storage Capacity</td>
</tr>
<tr>
<td>Option -309</td>
<td>Option -430 30.7 TB HDD Storage Capacity</td>
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<tr>
<td>Option -311</td>
<td>Option -460 61.4 TB HDD Storage Capacity</td>
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<td>Option -681</td>
<td>10 to 36 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and General Options may change, contact Pentek for the latest information

Specifications subject to change without notice
Model RTR 2546

200 MS/sec RF/IF Rugged SFF Recorder

General Information
Optimized for SWaP (size, weight and power), the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

Configured with four 200 MS/sec 16-bit A/Ds the RTR 2546 is capable of recording the full four-channel bandwidth at a 1.6 GB/sec sustained rate to disk. An 800 MHz 16-bit D/A allows for real-time full-bandwidth signal reproduction.

Built-in digital downconverters and upconverters allow IF signals to be converted to baseband and reproduced at the original IF frequency.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates, and DUC interpolations are among the GUI-selectable system parameters, providing a fully programmable system capable of recording and reproducing a wide range of signals.

An ATX power supply accepts 110-240 VAC, drawing under 150 W and typically around 100 W. SFF Models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds. An optional GPS receiver allows for precise GPS time and position stamping.

SystemFlow Software
All Talon Rugged Small Form Factor recorders include the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. A user API is also included to allow custom recorder control interfaces to be easily built.

SystemFlow provides signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows Professional workstation, all Talon SFF recorders allow the user to install post-processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data files.

Rugged Chassis with SSD Storage
The SFF system is configured with hot-swappable SSDs, front-panel USB ports, and I/O connectors on the rear panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 30.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

A push of a button unlatches each of the data drives and the OS drive. Drives are mounted on sleds and can be easily transferred to an offload system while the recorder stays in the field.

PC and signal I/O are available on the rear panel with standard connectors.

Features
- Housed in a small chassis measuring 5.25” H x 8.5” W x 14” D
- Weighs 17 lb (7.7 kg)
- Shock and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 200 MHz 16-bit A/Ds
- 800 MHz 16-bit D/A s
- Real-time aggregate recording rates of up to 1.6 GB/sec
- DDC decimation and DUC interpolation range from 2 to 65,536
- 80 MHz record and playback signal bandwidths
- Recording and playback of IF signals up to 700 MHz
- Up to 30 terabytes of SSD storage to NTFS RAID solid state disk array
- Windows® workstation with high performance Intel® Core™ i7 processor
- SystemFlow® GUI with Signal Viewer analysis tool
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
Model RTR 2546  
200 MS/sec RF/IF Rugged SFF Recorder

➤ SystemView Graphical User Interface

SystemFlow Recorder Interface
The RTR 2546 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

SystemFlow Hardware Configuration Interface
The RTR 2546’s Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer
The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201 818-5900 ● Fax: 201 818-5904 ● Email: info@pentek.com  www.pentek.com
Specifications

PC Workstation (standard configuration)
Operating System: Windows workstation
Processor: Intel i7 7700K (7th Gen) quad core processor
Clock Speed: 4.2 GHz
Operating System Drive: 250 GB SSD
SDRAM: 8 standard, 16 or 32 GB optional
RAID
  - Total Storage: 3.8 TB – 30.6 TB
  - Supported RAID Levels: 0, 5 and 6
  - Drive Bays: Hot-swap, removable, front panel

Rear Panel I/O
  - Four USB 3.0 ports
  - Two Gigabit RJ45 ports
  - Two HDMI and One DVI ports
  - Audio and PS2 ports
  - USB 3.0 Type-C port
  - Two Wi-Fi antenna ports

Front Panel I/O
  - Two USB 2.0 ports
  - Power and recessed RESET buttons
  - LED indicators for power and HDD access

Analog Signal Inputs
  - Transformer-coupled, female SSMC connectors
  - Transformer Type: Coil Craft WBC4-6TLB
  - Full Scale Input: +8 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
  - Type: Texas Instruments ADS5485
  - Sampling Rate ($f_s$): 10 MHz to 200 MHz
  - Resolution: 16 bits
  - A/D Record Bandwidth: $f_s/2 = \text{Nyquist bandwidth}$
  - Anti-Aliasing Filters: External, user-supplied

Digital Downconverter
  - Type: Pentek IP Core
  - Decimation(D): 2 to 65,536
  - IF Center Frequency Tuning: DC to $f_s$, 32 bits
  - DDC Usable Bandwidth: $0.8 f_s/D$

Analog Signal Outputs
  - Connectors: Transformer-coupled, female SSMC
  - Full Scale Output: +4 dBm into 50 ohms
  - 3 dB Passband: 300 kHz to 700 MHz

Digital Upconverter, Interpolator and D/As
  - D/A Resolution: 16 bits
  - Output Signal: Analog, real or quadrature
  - Type: TI DAC5688 and Pentek-installed IP core interpolator
  - Interpolation: 2 to 65,536
  - Input Data Rate to DAC5688: 250 MS/sec max.
  - Output Sampling Rate: 800 MHz max
  - Output IF: DC to 400 MHz
  - Bandwidth Range: Matches recording bandwidths
  - Clock Sources: Selectable from onboard programmable VCXO, external or LVDS clocks

External Clocks
  - Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, 10 to 200 MHz

Physical and Environmental
  - Size: 5.25” H x 8.5” W x 14.0” D
  - Weight: 17 lb (7.7 kg)
  - Operating Temp: 0° to +50° C
  - Storage Temp: –40° to +85° C
  - Relative Humidity: 5 to 95%, non-condensing
  - Operating Shock: 15 g max. (11 msec, half-sine wave)
  - Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
    20 to 500 Hz: 1.4 g peak acceleration
  - Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 150 W max.

Model RTR 2546 Ordering Information and Options

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<thead>
<tr>
<th>Channel Configurations</th>
<th>Storage Options</th>
<th>Additional Options</th>
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</thead>
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<td>Option -202</td>
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<td>Option -203</td>
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<tr>
<td>Option -204</td>
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<tr>
<td>Option -221</td>
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<td>Option -310</td>
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<td>Option -222</td>
<td></td>
<td>Option -630</td>
</tr>
<tr>
<td>Option -224</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201.818.5900  Fax: 201.818.5904  Email: info@pentek.com
www.pentek.com
General Information

Optimized for SWaP (size, weight and power) the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25" H x 8.5" W x 14" D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

Configured with two A/Ds and two D/As, the 2547 provides the ability to play back two channels of real data or one channel of complex data with the available DUC.

Built-in digital downconverters and upconverters allow for IF signals to be converted to baseband and reproduced at the original IF frequency.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates, and DUC interpolations are among the GUI-selectable system parameters, providing a fully programmable system capable of recording and reproducing a wide range of signals.

An ATX power supply accepts 110-240 VAC, drawing under 150 W and typically around 100 W. SFF Models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds.

An optional GPS receiver allows for precise GPS time and position stamping.

SystemFlow Software

All Talon Rugged Small Form Factor recorders include the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. A user API is also included to allow custom recorder control interfaces to be easily built.

SystemFlow provides signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows Professional workstation, all Talon SFF recorders allow the user to install post-processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data files.

Rugged and Flexible Architecture

The SFF system is configured with hot-swappable SSDs, front-panel USB ports, and I/O connectors on the rear panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 30.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

A push of a button unlatches each of the data drives and the OS drive. Drives are mounted on sleds and can be easily transferred to an offload system while the recorder stays in the field.

PC and signal I/O is available on the rear panel with standard connectors.
Model RTR 2547
500 MS/sec RF/IF Rugged SFF Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Recorder Interface

The RTR 2747 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTR 2747 Configure screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
## Specifications

**PC Workstation (standard configuration)**
- **Operating System**: Windows workstation
- **Processor**: Intel i7 7700K (7th Gen) quad core processor
- **Clock Speed**: 4.2 GHz
- **Operating System Drive**: 250 GB SSD
- **SDRAM**: 8 GB standard, 16 GB or 32 GB optional
- **RAID**
  - **Total Storage**: 3.8 TB – 30.6 TB
  - **Supported RAID Levels**: 0, 5 and 6
  - **Drive Bays**: Hot-swap, removable, front panel

**Rear Panel I/O**
- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

**Front Panel I/O**
- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

**Analog Signal Inputs**
- Transformer-coupled, female SSMC connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +5 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters**
- **Type**: Texas Instruments AD55463 or AD55474 (Option-014)
- **Sampling Rate (f_s)**: 10 MHz to 500 MHz
- **Resolution**: 12 Bits or 14 bits (Option-014)
- **A/D Record Bandwidth**: f_s/2 = Nyquist bandwidth
- **Anti-Aliasing Filters**: External, user-supplied

**Digital Downconverter**
- **Type**: Pentek IP Core
- **Decimation (D)**: 2to 65,536
- **IF Center Frequency Tuning**: DC to f_s, 32 bits
- **DDC Usable Bandwidth**: 0.8*f_s/D

**Analog Signal Outputs**
- **Connectors**: Transformer-coupled, female SSMC
- **Full Scale Output**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

**Digital Upconverter, Interpolator and D/A**
- **D/A Resolution**: 16 bits
- **Output Signal**: Analog, real or quadrature
- **Type**: TI DAC5688 and Pentek-installed IP core interpolator
- **Interpolation**: 2 to 65,536
- **Input Data Rate to DAC5688**: 250 MS/sec max.
- **Output Sampling Rate**: 800 MHz max
- **Output IF**: DC to 400 MHz
- **Bandwidth Range**: Matches recording bandwidths

**Clock Sources**: Selectable from onboard programmable VCXO, external or LVDS clocks

**External Clocks**
- **Type**: Female SSMC connector, sine wave, 0 to +12 dBm, AC-coupled, 50 ohms, 10 to 500 MHz divider input clock or PLL system reference

**Internal Clock**
- **Type**: Programmable VCXO from 10 to 810 MHz

**Physical and Environmental**
- **Size**: 5.25” H x 8.5” W x 14.0” D
- **Weight**: 17 lb (7.7 kg)
- **Operating Temp**: 0° to +50° C
- **Storage Temp**: –40° to +85° C
- **Relative Humidity**: 5 to 95%, non-condensing
- **Operating Shock**: 15 g max. (11 msec, half-sine wave)
- **Operating Vibration**: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- **Power Requirements**: 100 to 240 VAC, 50 to 60 Hz, 150 W max.

## Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-201</td>
<td>1-channel recording</td>
</tr>
<tr>
<td>-202</td>
<td>2-channel recording</td>
</tr>
<tr>
<td>-221</td>
<td>1-channel playback</td>
</tr>
<tr>
<td>-222</td>
<td>2-channel playback</td>
</tr>
</tbody>
</table>

## Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-410</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>-415</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>-420</td>
<td>15.3 TB SSD storage capacity</td>
</tr>
<tr>
<td>-430</td>
<td>30.6 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

## Additional Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-261</td>
<td>GPS Time and Position Stamping</td>
</tr>
<tr>
<td>-285</td>
<td>Raid 5 Configuration</td>
</tr>
<tr>
<td>-286</td>
<td>Raid 6 Configuration</td>
</tr>
<tr>
<td>-309</td>
<td>16 GB System Memory</td>
</tr>
<tr>
<td>-310</td>
<td>32 GB System Memory</td>
</tr>
<tr>
<td>-014</td>
<td>400 MHz, 14-bit A/Ds</td>
</tr>
<tr>
<td>-630</td>
<td>6 to 30 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
**Model RTR 2548**

**1 GS/sec RF/IF Rugged SFF Recorder**

**General Information**

Optimized for SWaP (size, weight and power), the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

Configured with 1.0 GS/sec 12-bit A/D, the RTR 2548 is capable of recording the full-channel bandwidth at a 2.0 GB/sec sustained rate to disk. A 1.0 GHz 16-bit D/A allows for real-time full-bandwidth signal reproduction.

A/D and D/A sampling rates are among the GUI-selectable system parameters, providing a fully programmable system capable of recording and reproducing a wide range of signals. A built-in synchronization module is provided to allow for multichannel phase-coherent operation.

An ATX power supply accepts 110-240 VAC, drawing under 150 W and typically around 100 W. SFF Models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds. An optional GPS receiver allows for precise GPS time and position stamping.

**SystemFlow Software**

All Talon Rugged Small Form Factor recorders include the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. A user API is also included to allow custom recorder control interfaces to be easily built.

SystemFlow provides signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows Professional workstation, all Talon SFF recorders allow the user to install post-processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data files.

**Rugged Chassis with SSD Storage**

The SFF system is configured with hot-swappable SSDs, front-panel USB ports, and I/O connectors on the rear panel. It is built in a rugged steel and aluminum chassis and is tested for shock and vibration.

The SSDs provide storage capacities of up to 30.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels including 0, 5, and 6, provide a choice for the required level of redundancy.

A push of a button unlatches each of the data drives and the OS drive. Drives are mounted on sleds and can be easily transferred to an offload system while the recorder stays in the field.

PC and signal I/O is available on the rear panel with standard connectors.
SystemFlow Graphical User Interface

The RTR 2548 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Recorder Interface

The RTR 2548 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTR 2548 Configure screens provide a simple and intuitive means for setting up the system parameters. The A/D configuration screen shown here, allows user entries for gate/trigger mode, gate/trigger polarity, and trigger source. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Model RTR 2548
1 GS/sec RF/IF Rugged SFF Recorder

Specifications

PC Workstation (standard configuration)
- Operating System: Windows workstation
- Processor: Intel i7 7700K (7th Gen) quad core processor
- Clock Speed: 4.2 GHz
- Operating System Drive: 250 GB SSD
- SDRAM: 8 GB standard, 16 GB or 32 GB optional
- RAID
  - Total Storage: 3.8 TB – 30.6 TB
  - Supported RAID Levels: 0, 5 and 6
  - Drive Bays: Hot-swap, removable, front panel

Rear Panel I/O
- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

Front Panel I/O
- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

Analog Recording Input

- Input Type: Transformer-coupled, female SSMC connector
- Transformer Type: Macom ETC1-1-13TR
- Full Scale Input: +10 dBm into 50 ohms
- 3 dB Passband: 5 MHz to 2 GHz

A/D Converter

- Type: Texas Instruments ADS5400
- Sampling Rate ($f_s$): 100 MHz to 1 GHz
- Resolution: 12 bits
- A/D Record Bandwidth: $f_s$/2 = Nyquist bandwidth
- Anti-Aliasing Filters: External, user-supplied

Analog Playback Output

- Output Type: Transformer-coupled, female SSMC connector
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

D/A Converter

- Type: TI DAC5681Z
- Interpolation: 1x, 2x or 4x
- Input Data Rate to DAC5681Z: 500 MS/sec max.
- Output Sampling Rate: 1 GHz, max.
- Output IF: 700 MHz, max.
- D/A Resolution: 16 bits

Clock Sources: Selectable from onboard programmable VCXO or external clock

External Clock

- Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz input clock or 10 MHz system reference

Internal Clock

- Type: Programmable VCXO
- VCXO Frequency Ranges: 100 to 945 MHz, 970 MHz to 1 GHz

Physical and Environmental

- Size: 5.25” H x 8.5” W x 14.0” D
- Weight: 17 lb (7.7 kg)
- Operating Temp: 0° to +50° C
- Storage Temp: –40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half-sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 150 W max.

Channel Configurations

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>-201</td>
<td>1-channel recording</td>
</tr>
<tr>
<td>-221</td>
<td>1-channel playback</td>
</tr>
</tbody>
</table>

Storage Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Storage Capacity</th>
</tr>
</thead>
<tbody>
<tr>
<td>-410</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>-415</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>-420</td>
<td>15.3 TB SSD storage capacity</td>
</tr>
<tr>
<td>-430</td>
<td>30.6 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

Additional Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-261</td>
<td>GPS Time and Position Stamping</td>
</tr>
<tr>
<td>-285</td>
<td>Raid 5 Configuration</td>
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<tr>
<td>-286</td>
<td>Raid 6 Configuration</td>
</tr>
<tr>
<td>-309</td>
<td>16 GB System Memory</td>
</tr>
<tr>
<td>-310</td>
<td>32 GB System Memory</td>
</tr>
<tr>
<td>-630</td>
<td>6 to 30 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
**Specifications**

PC Workstation (standard configuration)
- Operating System: Windows workstation
- Processor: Intel i7 7700K (7th Gen) quad core processor
- Clock Speed: 4.2 GHz
- Operating System Drive: 250 GB SSD
- SDRAM: 8 GB standard, 16 GB or 32 GB optional

RAID
- Total Storage: 3.8 TB – 30.6 TB
- Supported RAID Levels: 0, 5 and 6
- Drive Bays: Hot-swap, removable, front panel

Rear Panel I/O
- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

Front Panel I/O
- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD acces

Analog Recording Input
- Input Type: Transformer-coupled, female SSMC connector
- Transformer Type: Macom ETC1-1-13TR
- Full Scale Input: +10 dBm into 50 ohms
- 3 dB Passband: 5 MHz to 2 GHz

A/D Converter
- Type: Texas Instruments AD55400
- Sampling Rate \( (f_s) \): 100 MHz to 1 GHz
- Resolution: 12 bits
- A/D Record Bandwidth: \( f_s / 2 \) = Nyquist bandwidth
- Anti-Aliasing Filters: External, user-supplied

Analog Playback Output
- Output Type: Transformer-coupled, female SSMC connector
- Full Scale Output: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

D/A Converter
- Type: TI DAC5681Z
- Interpolation: 1x, 2x or 4x
- Input Data Rate to DAC5681Z: 500 MS/sec max.
- Output Sampling Rate: 1 GHz, max.

Clock Sources: Selectable from onboard programmable VCXO or external clock

External Clock
- Type: Female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz input clock or 10 MHz system reference

Internal Clock
- Type: Programmable VCXO
- VCXO Frequency Ranges: 100 to 945 MHz, 970 MHz to 1 GHz

Physical and Environmental
- Size: 5.25” H x 8.5” W x 14.0” D
- Weight: 17 lb (7.7 kg)
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half-sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 150 W max.

**Model RTR 2548 Ordering Information and Options**

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<tr>
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<th>Additional Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -201</td>
<td>Option -410</td>
<td>Option -261</td>
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<tr>
<td>1-channel recording</td>
<td>3.8 TB SSD storage capacity</td>
<td>GPS Time and Position Stamping</td>
</tr>
<tr>
<td>Option -221</td>
<td>Option -415</td>
<td>Option -285</td>
</tr>
<tr>
<td>1-channel playback</td>
<td>7.6 TB SSD storage capacity</td>
<td>Raid 5 Configuration</td>
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<tr>
<td></td>
<td>Option -420</td>
<td>Option -286</td>
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<tr>
<td></td>
<td>15.3 TB SSD storage capacity</td>
<td>Raid 6 Configuration</td>
</tr>
<tr>
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<td>Option -430</td>
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</tr>
<tr>
<td></td>
<td>30.6 TB SSD storage capacity</td>
<td>16 GB System Memory</td>
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<td></td>
<td>6 to 30 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
Model RTR 2549

3.6 GS/sec Ultra Wideband RF/IF Rugged SFF Recorder

General Information

Optimized for SWaP (size, weight and power,) the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

The RTR 2549 uses 12-bit, 3.6 GHz A/D converters. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit or 16-bit-wide consecutive samples (12-bit digitized samples residing in the 16 MSBs of the 16-bit word). A high-speed RAID array provides a maximum streaming recording rate to disk of 4.0 GB/sec.

An ATX power supply accepts 110-240 V AC, drawing under 150 W and typically around 100 W. SFF Models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds.

Optional GPS time and position stamping allows the user to capture this critical information in the header of each data file.

SystemFlow Software

All Talon Rugged Small Form Factor recorders include the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. A user API is also included to allow custom recorder control interfaces to be easily built.

SystemFlow provides signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session. These tools include a virtual oscilloscope, spectrum analyzer and spectrogram displays.

Built on a Windows Professional workstation, all Talon SFF recorders allow the user to install post-processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data files.

Rugged Chassis with SSD Storage

The SFF system is configured with hot-swappable SSDs, front-panel USB ports, and I/O connectors on the rear panel. It is built in a rugged steel and aluminum chassis and is tested for shock and vibration.

The SSDs provide storage capacities of up to 30.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels including 0, 5, and 6, provide a choice for the required level of redundancy.

A push of a button unlatches each of the data drives and the OS drive. Drives are mounted on sleds and can be easily transferred to an offload system while the recorder stays in the field.

PC and signal I/O is available on the rear panel with standard connectors.

Features

- Housed in a small chassis measuring 5.25” H x 8.5” W x 14” D
- Weighs 17 lb (7.7 kg)
- Shock and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Sample rates up to 3.6 GHz in single-channel mode
- Sample rates up to 1.8 GHz in dual-channel mode
- Capable of recording RF/IF frequencies to 1.75 GHz in single-channel mode
- Capable of recording RF/IF frequencies to 2.8 GHz in dual-channel mode
- 12-bit A/D, with 16-bit and 8-bit packing modes
- Real-time aggregate recording rate of up to 4.0 GB/sec
- Up to 30 terabytes of SSD storage to NTFS RAID solid state disk array
- Windows® workstation with high-performance Intel® Core™ i7 processor
- SystemFlow® GUI with Signal Viewer analysis tool
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Channel 1

Channel 2

3.6 GHz
1.8 GHz
12-bit A/D

INTEL

PROCESSOR

SYSTEM DRIVE

DDR SDRAM

HOST PROCESSOR

RUNNING SYSTEMFLOW

Gigabit Ethernet

USB

Video Output

GPS

Antenna (Optional)

DATA DRIVES

DATA DRIVES

DATA DRIVES

DATA DRIVES

RAID DATA STORAGE

MODEL RTR 2549

www.pentek.com

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com
SystemFlow Graphical User Interface

The RTR 2549 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Recorder Interface

The RTR 2549 GUI provides the user with a control interface for the recording system. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or signals recorded on disk.

SystemFlow Hardware Configuration Interface

The RTR 2549 Configure screens provide a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, sampling frequency, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual, annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Specifications

PC Workstation (standard configuration)
- Operating System: Windows workstation
- Processor: Intel i7 7700K (7th Gen) quad core processor
- Clock Speed: 4.2 GHz
- Operating System Drive: 250 GB SSD
- SDRAM: 8 GB standard, 16 GB or 32 GB optional

RAID
- Total Storage: 3.8 TB – 30.6 TB
- Supported RAID Levels: 0, 5 and 6
- Drive Bays: Hot-swap, removable, front panel

Rear Panel I/O
- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

Front Panel I/O
- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

Analog Signal Inputs
- Connectors: Two rear panel SSMC connectors, In 1 & In 2
- Input Type: Single-ended, non-inverting
- Full Scale Input: +4 dBm into 50 ohms
- Coupling: Transformer-coupled
- Analog Input Transformers:
  - Bandwidth: 4.5 kHz to 3.0 GHz

A/D Converters
- Type: Texas Instruments ADC12D1800
- Sampling Rate:
  - Single-channel mode: 500 MHz to 3.6 GHz
  - Dual-channel mode: 150 MHz to 1.8 GHz
- Resolution: 12 bits
- Maximum Usable Input Frequency
  - Single-channel mode: 1.75 GHz
  - Dual-channel mode: 2.8 GHz
- Anti-Aliasing Filters: External, user-supplied

Digital Downconverters
- Modes: One or two channels, programmable
- Supported Sample Rate ($f_s$):
  - One-channel mode: 3.6 GHz
  - Two-channel mode: 1.8 GHz
- Decimation Range ($D$):
  - One-channel mode: 8x, 16x, 32x, bypass
  - Two-channel mode: 4x, 8x, 16x, bypass
- Usable Output Bandwidth: $0.8f_s/D$

Physical and Environmental
- Size: 5.25” H x 8.5” W x 14.0” D
- Weight: 17 lb (7.7 kg)
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half-sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 150 W max.

Storage Options
- Option -415: 7.6 TB SSD storage capacity
- Option -420: 15.3 TB SSD storage capacity
- Option -430: 30.6 TB SSD storage capacity

Additional Options
- Option -261: GPS Time and Position Stamping
- Option -285: Raid 5 Configuration
- Option -286: Raid 6 Configuration
- Option -309: 16 GB System Memory
- Option -310: 32 GB System Memory
- Option -630: 6 to 30 VDC Power Supply

Model RTR 2549 Ordering Information and Options

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201 818-5900  Fax: 201 818-5904  Email: info@pentek.com  www.pentek.com
Model RTS 2715

10-Gigabit Ethernet Rackmount Recorder

General Information
The Talon® RTS 2715 is a complete turn-key recording system for storing one or two ten-gigabit Ethernet (10GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

Rear panel SFP+ connectors accommodate copper, multi-mode or single-mode fibre interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software
The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Features
- Records 10-gigabit Ethernet streams
- TCP and UDP protocols
- Copper or optical 10GbE interfaces
- Aggregate recording rates to 1.6 GB/sec
- 4U or 5U 19-inch industrial rackmount PC server chassis
- Windows® 7 Professional workstation with a high performance Intel® Core™ i7 processor
- Up to 100 terabytes storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into applications
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Contact factory for options, number of channels, recording rates, and disk capacity.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTS 2715 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Flexible Architecture
The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.
SystemFlow Main Interface

The RTS 2715 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
**Model RTS 2715**

**10-Gigabit Ethernet Rackmount Recorder**

**SystemFlow API**

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTS 2715 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTS 2715 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

**Specifications**

**PC Workstation**

- **Operating System:** Windows 7 Professional
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or higher
- **SDRAM:** 8 GB
- **RAID**
  - **Storage:** 2–100 TB
  - **Drive Type:** Hard disk drives
  - **Supported Levels:** 0, 1, 5, 6, 10 and 50

**Physical and Environmental**

- **Dimensions**
  - 4U Long Chassis: 19” W x 26” D x 7” H
  - 5U Long Chassis: 19” W x 26” D x 8.75” H
- **Weight:** 50–80 lb
- **Operating Temp:** +5° to +45° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

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**Model RTS 2715 Ordering Information and Options**

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<th>Storage Options</th>
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<td><strong>Option -406</strong> 2.0 TB HDD storage capacity</td>
</tr>
<tr>
<td><strong>Option -102</strong> 10-Gigabit Ethernet</td>
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<tr>
<td><strong>Channel Configuration</strong></td>
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</tr>
<tr>
<td><strong>Option -201</strong> 1-Ethernet port</td>
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<td><strong>Option -202</strong> 2-Ethernet ports</td>
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<tr>
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<td><strong>Option -282</strong> Single-mode optical, LC connectors</td>
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</tr>
<tr>
<td><strong>Option -284</strong> RJ45 Connector</td>
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</tbody>
</table>

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTR 2755 is a complete turn-key recording system for storing 10-Gigabit Ethernet (10GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized disk storage technology, the system guarantees loss-free performance at aggregate recording rates up to 4.0 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTR 2755 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2755 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2755 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2755 performs well in ground, shipborne and airborne environments. The hot-swappable SSDs provide storage capacity of up to 46 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2755 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy.

Features

- Designed to operate under conditions of shock and vibration
- Records 10-Gigabit Ethernet streams
- TCP and UDP protocols
- Copper or optical 10GbE interfaces
- Aggregate recording rates to 4.0 GB/sec
- Removable SSD drives
- 4U short 19-inch rugged rackmount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- Up to 46 terabytes of storage to NTFS RAID solid state disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into applications
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Contact factory for options, number of channels, recording rates, and disk capacity.
SystemFlow Graphical User Interface

The RTR 2755 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
➤ SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2755 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2755 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation

Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB
RAID
  Storage: 3.8, 7.6, 15.3, 30.7 or 46.0 TB
  Drive Type: Solid-state drive
  Supported Levels: 0, 1, 5, 6, 10 and 50

10-Gigabit Ethernet Interface

Option 280: SFP+
  Quantity: 2 ports
  Connector Type: SFP+

Option 281: Multi-mode Fibre Optical
  Quantity: 2 ports
  Cable: Multi-mode fibre, 850 nm
  Connector Type: LC
  Max. Cable Length: Up to 300 m

Option 282: Single-mode Fibre Optical
  Quantity: 2 ports
  Cable: Single-mode fibre, 1310 nm
  Connector Type: LC
  Max Cable Length: Up to 10 km

Physical and Environmental

Dimensions
  4U Short Chassis: 19” W x 21” D x 7” H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTR 2755 Ordering Information and Options

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<tr>
<td>Gigabit Ethernet</td>
<td>3.8 TB SSD storage capacity</td>
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<td>Option -102</td>
<td>Option -415</td>
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<tr>
<td>10-Gigabit Ethernet</td>
<td>7.6 TB SSD storage capacity</td>
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<table>
<thead>
<tr>
<th>Channel Configuration</th>
<th>General Options (append to all options)</th>
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<tbody>
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<td>Option -201</td>
<td>Option -261</td>
</tr>
<tr>
<td>1-Ethernet port</td>
<td>GPS time and position stamping</td>
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<tr>
<td>Option -202</td>
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<tr>
<td>2-Ethernet ports</td>
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<tr>
<td>Option -204</td>
<td></td>
</tr>
<tr>
<td>4-Ethernet ports</td>
<td></td>
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<tr>
<td>Option -208</td>
<td></td>
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<tr>
<td>8-Ethernet ports</td>
<td></td>
</tr>
<tr>
<td>Note: Option -208 available only with Option -101</td>
<td></td>
</tr>
</tbody>
</table>

10GbE Interface

Option -280 SFP+ connectors
Option -281 Multi-mode optical, LC connectors
Option -282 Single-mode optical, LC connectors

Contact Pentek for other configurations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

The Talon® RTX 2775 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2775 is intended for military, airborne and UAV applications requiring a rugged system.

The RTX 2775 records one or two 10-gigabit Ethernet (10GbE) streams; it is ideal for capturing any type of streaming sources, including live transfers from sensors or data from other computers, and supports both TCP and UDP protocols.

Using highly-optimized disk storage technology, the system guarantees loss-free performance at aggregate recording rates up to 4.0 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTX 2775 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Features

- Designed to meet MIL-STD-810 shock and vibration
- Designed to meet EMC/EMI per MIL-STD-461 EMC
- 4U 19-inch rugged rackmount PC server chassis, 22" deep
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
- Records 10-gigabit Ethernet streams
- One or two channels
- TCP and UDP protocols
- Copper or optical 10GbE interfaces
- Real-time aggregate recording rates up to 4.0 GB/sec
- Up to four front-panel removable QuickPac SSD drive canisters with eight drives each
- Up to 30 terabytes of storage to NTFS RAID disk array
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTX 2775 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTX 2775 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

Rugged Mil-Spec Chassis

The Talon RTX 2775 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.
SystemFlow Main Interface

The RTX 2775 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2755 from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2755 as a high-performance server front-end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation (standard configuration)

Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB

Data Storage

Style: Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
Location: Front panel
Capacity: Up to 30 TB
Number of Drives: Up to 32 total
Supported RAID Levels: 0, 1, 5 and 6

Ten-Gigabit Ethernet Interface

Option 280: SFP+
  Quantity: 2 ports
  Connector Type: SFP+
Option 281: Multi-mode Fibre Optical
  Quantity: 2 ports
  Cable: Multi-mode fibre, 850 nm
  Connector Type: LC
  Max. Cable Length: Up to 300 m
Option 282: Single-mode Fibre Optical
  Quantity: 2 ports
  Cable: Single-mode fibre, 1310 nm
  Connector Type: LC
  Max. Cable Length: Up to 10 km

Physical and Environmental

Dimensions: 19" W x 22" D x 7" H
Weight: 50 lb, approx.
Operating Temp: –20° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 10% to 95%, non-condensing
Operating Shock: Designed to MIL-STD 810F, method 514.5, procedures I and VI
Operating Vibration: Designed to MIL-STD 810F, method 514.5, procedure I
EMI/EMC: Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS103
Input Power: 85 to 264 VAC, 47– 400 Hz, 600 W max.

Model RTX 2775 Ordering Information and Options

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<th>Storage Options</th>
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<td>Option -410 3.8 TB SSD storage</td>
</tr>
<tr>
<td>Option -102 10-Gigabit Ethernet</td>
<td>Option -415 7.6 TB SSD storage</td>
</tr>
<tr>
<td>Option -201 1-Ethernet port</td>
<td>Option -418 11.5 TB SSD storage</td>
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<tr>
<td>Option -202 2-Ethernet ports</td>
<td>Option -420 15.3 TB SSD storage</td>
</tr>
<tr>
<td>Option -204 4-Ethernet ports</td>
<td>Option -425 23.0 TB SSD storage</td>
</tr>
<tr>
<td>Option -208 8-Ethernet ports</td>
<td>Option -430 30.7 TB SSD storage</td>
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| 10GbE Interface                   | Option -625 Front-panel removable OS drive |

Contact Pentek for other configurations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
Model RTR 2735A

1-, 10-, 40-Gigabit Portable Ethernet Recorder

General Information
The Talon® RTR 2735A can accommodate multiple Ethernet data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

The RTR 2735A can accommodate gigabit, 10-gigabit and 40-gigabit Ethernet interfaces.

Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 4.0 GB/sec.

Rear panel SFP+ or RJ45 connectors accommodate copper, multi-mode or single-mode fibre interfaces.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

SystemFlow Software
The RTR 2735A includes the Pentek System-Flow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Features
- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, approximately 25 pounds
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Records gigabit, 10-gigabit or 40-gigabit Ethernet streams
- TCP and UDP protocols
- Copper or optical interfaces
- Aggregate recording rates to 4.0 GB/sec
- Windows workstation with a high performance Intel® Core™ i7 processor
- Up to 61 terabytes of SSD storage to NTFS RAID solid state disk array
- Multiple RAID levels, including 0, 5, and 6
- SystemFlow® GUI with Signal Viewer analysis tool
- C-callable API for integration of recorder into applications
- Optional file headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Optional 10–36 VDC power supply

Contact factory for options, number of channels, recording rates, and disk capacity.

Built on a server-class Windows Server 2016 workstation, the RTR 2735A allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2735A records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk using the 8X double layer DVD±R/RW drive.

Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

Rugged Chassis with SSD Storage
The RTR 2735A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration.

The SSDs provide storage capacities of up to 61,4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

Contact factory for options, number of channels, recording rates, and disk capacity.
Model RTR 2735A
1-, 10-, 40-Gigabit Portable Ethernet Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Main Interface
The RTR 2735A GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface
The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface
The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
Model RTR 2735A
1-, 10-, 40-Gigabit Portable Ethernet Recorder

SystemFlow API
SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2735A from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2735A as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications
PC Workstation (standard configuration)
- Operating System: 64-bit Windows workstation
- Processor: Intel Core i7 processor
- Clock Speed: 3.0 GHz or higher
- Operating System Drive: 250 GB SSD
- SDRAM: 8 GB standard, optionally up to 64 GB
- Monitor: Built-in 17.3” high-resolution LCD, 1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface Brightness: 300 cd/m²; Contrast ratio: 400:1 typical
- RAID
  - Storage: 3.8 to 61.4 TB
  - Drive Type: Solid-state drives
  - Supported RAID Levels: 0, 5, and 6
  - Drive Bays: Hot-swap, removable, side panel
  - USB 2.0 Ports: Four on left side, two on front panel
  - USB 3.0 Ports: Two on left side
  - 1 Gb Ethernet Ports: Two on left side
  - Aux Video Output: 15-pin VGA on left side

Optional DC Power supply
- Voltage: 10 to 36 VDC
- Input Current: 42 to 26 A (39 A at 24 VDC)
- Inrush Current: 100 A at 24 VDC
- Temperature Range: Oper.: 0° to 50° C, Store: −40° to 80° C
- Efficiency: >80% typical at 24 V full load
- Power Good Signal: On delay 100 to 500 msec
- OverPower Protection: 110% to 160%
- Remote Control: On/Off
- Safety: Meets UL, TUV, CB specifications

Physical and Environmental
- Size: 16.0” W x 6.9” D x 13.0” H
- Weight: 30 lb max.
- Operating Temp: 0° to +50° C
- Storage Temp: −40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 30 g max. (11 msec, half-sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- Non-operating Vibration: 5 to 500 Hz: 2.06 g RMS
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Interface Options
- Option -101 Gigabit Ethernet
- Option -102 10-Gigabit Ethernet
- Option -103 40-Gigabit Ethernet

Channel Configuration
- Option -201 1-Ethernet port
- Option -202 2-Ethernet ports
- Option -204 4-Ethernet ports
- Option -208 8-Ethernet ports

10GBE Interfaces available with Option -102
- Option -280 SFP+ connectors
- Option -281 Multi-mode optical, LC connectors
- Option -282 Single-mode optical, LC connectors
- Option -284 RJ45 Connector

Storage Options
- Option -410 3.8 TB SSD storage capacity
- Option -415 7.6 TB SSD storage capacity
- Option -420 15.3 TB SSD storage capacity
- Option -430 30.7 TB SSD storage capacity
- Option -460 61.4 TB SSD Storage Capacity

Additional Options
- Option -261 GPS Time & Position Stamping
- Option -264 IRIG-B Time Stamping
- Option -285 RAID 5 Configuration
- Option -286 RAID 6 Configuration
- Option -309 16 GB System Memory
- Option -311 64 GB System Memory
- Option -625 Removable Operating System Drive
- Option -681 10 to 36 VDC Power Supply

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information
Specifications subject to change without notice
Model RTV 2602

Serial FPDP Rackmount Value Recorder

General Information

The Talon® RTV 2602 Serial FPDP Value Recorder is designed to provide a low-cost solution to users looking to capture and play back multiple Serial FPDP streams. It can record up to four Serial FPDP channels to the built-in 4 TB RAID consisting of cost-effective, enterprise-class HDD storage. It is a complete turnkey recording system, ideal for capturing any type of streaming sources. These include live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification.

Like all Talon recorders in the RTV Value Recorder series, the RTV 2602 ships from stock allowing users to be up and running in the field just days after purchase.

The RTV 2602 comes in a 4U 19 in. rack-mount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available in the front. Air is pulled through the system from front to back to allow operation at ambient temperatures from 5°C to 35°C.

The RTV 2606 can be populated with up to four SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates. Up to four channels can be recorded simultaneously with an aggregate recording rate of up to 400 MB/sec.

As an option, a GPS or IRIG receiver card can be supplied with the system providing accurate time stamping of recorded data. Additionally, the GPS receiver delivers GPS position information that can be recorded along with the input signals.

Features

- Complete Serial FPDP record and playback system
- Lowest-cost entry into Serial FPDP
- Quick delivery: Model RTV 2602 ships from stock
- 4U 19-inch industrial rack-mount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i3 processor
- Real-time aggregate recording rates up to 400 MB/sec
- 4 TB of data storage to NTFS RAID disk array
- SystemFlow® recording software
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

New! New! New! New! New!

- Complete Serial FPDP record and playback system
- Lowest-cost entry into Serial FPDP
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- 4U 19-inch industrial rack-mount PC server chassis
- Windows® 7 Professional workstation with high-performance Intel® Core™ i3 processor
- Real-time aggregate recording rates up to 400 MB/sec
- 4 TB of data storage to NTFS RAID disk array
- SystemFlow® recording software
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping

SystemFlow Software and API

The RTV 2602 includes the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder.

Custom configurations can be stored as profiles and later loaded when needed, so users can select preconfigured settings with a single click.

In addition to the GUI, the RTV 2602 provides a C-callable API that allows the user to integrate the recorder control into any application. A simple set of commands that provide configuration and control come with source code and examples to allow for an exceptionally fast integration.

INTEL PROCESSOR

SYSTEM DRIVE

DDR SDRAM

HOST PROCESSOR

RUNNING SYSTEMFLOW

Gigabit Ethernet
USB
Keyboard
Mouse
Video Output
GPS Antenna (Optional)

MODEL RTV 2602

4 TB DATA STORAGE

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS

Channels In / Out

Serial FPDP

INTEL PROCESSOR

SYSTEM DRIVE

DDR SDRAM

HOST PROCESSOR

RUNNING SYSTEMFLOW

Gigabit Ethernet
USB
Keyboard
Mouse
Video Output
GPS Antenna (Optional)

MODEL RTV 2602

4 TB DATA STORAGE

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS

Channels In / Out

Serial FPDP

INTEL PROCESSOR

SYSTEM DRIVE

DDR SDRAM

HOST PROCESSOR

RUNNING SYSTEMFLOW

Gigabit Ethernet
USB
Keyboard
Mouse
Video Output
GPS Antenna (Optional)

MODEL RTV 2602

4 TB DATA STORAGE

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS

DATA DRIVERS
➤ SystemFlow Graphical User Interface

SystemFlow Main Interface
The RTV 2602 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface
The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP’s copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface
The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified and monitoring functions inform the operator of recording progress. ➤
Model RTV 2602

System Architecture

Built on a Windows 7 Professional workstation, the RTV 2602 allows the user to install post-processing and analysis tools to operate on the recorded data. The recorder stores data in the native NTFS file system, providing immediate access to any installed Windows application. Alternately, the NTFS drive can be accessed remotely over the built-in gigabit Ethernet link from a remote Windows or Linux machine.

Recorded data can be off-loaded via the rear-panel gigabit Ethernet port, two front-panel USB 3.0 ports, two rear-panel USB 3.0 ports or four rear-panel USB 2.0 ports. A built-in DVD +/- R/RW drive allows the user to burn recorded data to disk. Hot-swappable front-panel drives can be easily removed and replaced with empty drives to provide additional data storage.

Specifications

PC Workstation (standard configuration)

- Operating System: Windows 7 Professional
- Processor: Intel Core i3 processor
- Clock Speed: 2.0 GHz or higher
- SDRAM: 8 GB
- RAID Storage: 4 TB
- Number of Drives: Six, removable, front panel access
- Optical Drive: DVD +/- R/RW, front panel access
- USB Ports: Front panel: Two USB 3.0; rear panel:
  - Two USB 3.0; Four USB 2.0
- Ethernet: Single 1GbE, rear panel
- Supported RAID Levels: 0

Serial FPDP Interface

- Copper - Option 280
  - Cable: 100-ohm shielded twin-ax
  - Connector Type: SFP+
  - Max. Cable Length: 20 m
- Multi-mode Fiber Optical - Option 281
  - Cable: Multi-mode fiber, 850 nm
  - Connector Type: LC
  - Max. Cable Length: Up to 300 m
- Single-mode Fiber Optical - Option 282
  - Cable: Single-mode fiber
  - Connector Type: LC
  - Max. Cable Length: Up to 10 km

Physical and Environmental

- Size: 19" W x 22.75" D x 7" H
- Weight: 50 lbs
- Operating Temp: +5° to +35° C
- Storage Temp: −40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTV 2602 Options Information

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Specifications are subject to change without notice
**General Information**

The Talon® RTS 2716 is a complete turn-key recording system capable of recording and playing multiple Serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

The RTS 2716 can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per Serial FPDP link.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

**SystemFlow Software**

The RTS 2716 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2716 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTS 2716 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

**Flexible Architecture**

The RTS 2716 is configured in a 4U or 5U 19” rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

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**Features**

- Complete Serial FPDP record and playback system
- Up to eight I/O channels in a single 4U or 5U 19 inch industrial rackmount PC server chassis
- Supports Flow Control, CRC, and Copy/Loop Mode as a receiver and transmitter
- Supports 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates
- Copper, single-mode and multi-mode fiber interfaces available
- Real-time aggregate recording rates of up to 1.6 GB/sec
- Up to 100 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high performance Intel® Core™ i7 processor

Contact factory for options, number of channels, recording rates, and disk capacity.
Model RTS 2716

Serial FPDP Rackmount Recorder

➤ SystemFlow Graphical User Interface

The RTS 2716 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The RTS 2716 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP's copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
➤ **SystemFlow API**

SystemFlow includes a complete API (Application Programming Interface) that supports control and status queries of all operations of the RTS 2716 from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTS 2716 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

**Specifications**

**PC Workstation**
- **Operating System:** Windows 7 Professional
- **Processor:** Intel Core i7 processor
- **Clock Speed:** 3.0 GHz or greater
- **SDRAM:** 6 GB
- **RAID**
  - Storage: 2.0–100.0 TB
  - Drive Type: 3.5” HDD
  - Supported Levels: 0, 1, 5, 6, 10 and 50

**Serial FPDP Interface**
- **Copper - Option 280**
  - Cable: 100-ohm shielded twin-ax
  - Connector Type: SFP+
  - Max. Cable Length: 20 m
- **Multi-mode Fiber Optical - Option 281**
  - Cable: Multi-mode fiber, 850 nm
  - Connector Type: LC
  - Max. Cable Length: Up to 300 m
- **Single-mode Fiber Optical - Option 282**
  - Cable: Single-mode fiber
  - Connector Type: LC
  - Max. Cable Length: Up to 10 km

**Physical and Environmental**
- **Dimensions**
  - Full 4U Chassis: 19” W x 26” D x 7” H
- **Weight:** 30 – 80 lb
- **Operating Temp:** +5° to +45° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.

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**Channel Configuration**
- **Option -204**
  - 4-channel recording
- **Option -208**
  - 8-channel recording

**SFPDP Interface**
- **Option -280**
  - SFP+ connectors
- **Option -281**
  - Multi-mode optical, LC connectors
- **Option -282**
  - Single-mode optical, LC connectors

**Storage Options**
- **Option -406**
  - 2.0 TB HDD storage capacity
- **Option -411**
  - 4.0 TB HDD storage capacity
- **Option -416**
  - 8.0 TB HDD storage capacity
- **Option -421**
  - 16.0 TB HDD storage capacity
- **Option -423**
  - 20.0 TB HDD storage capacity
- **Option -439**
  - 30.0 TB HDD storage capacity
- **Option -450**
  - 45.0 TB HDD storage capacity
- **Option -460**
  - 60.0 TB HDD storage capacity
- **Option -480**
  - 100.0 TB HDD storage capacity

*Note: Options -450 and -460 require a 5U Chassis; Option -480 requires a 6U chassis*

**General Options** (append to all options)
- **Option -261**
  - GPS time & position stamping
- **Option -264**
  - IRIG-B time stamping

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTR 2736 is a complete turn-key recording system capable of recording and playing back multiple Serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2.4 GB/sec.

The RTR 2736 can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per Serial FPDP link.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

SystemFlow Software

The RTR 2736 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2736 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2736 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via a gigabit Ethernet port, eight USB 2.0 ports, two USB 3.0 ports or two eSATA 3 Ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Rugged and Flexible Architecture

The RTR 2736 is configured in a portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using shock- and vibration-resistant SSDs, the RTR 2736 is designed to reliably operate as a portable field instrument.

The hot-swappable SSDs provide storage capacities of up to 7.6 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 1, 5 and 6, provide a choice for the required level of redundancy.

Features

- Designed to operate under conditions of shock and vibration
- Portable system measures 16.9” W x 9.5” D x 13.4” H
- Rugged aluminum alloy chassis
- Lightweight, approximately 30 pounds
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Up to eight I/O channels
- Supports Flow Control, CRC, and Copy/Loop Mode as a receiver and transmitter
- Supports 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates
- Copper, single-mode and multi-mode fiber interfaces available
- Real-time aggregate recording rates of up to 2.4 GB/sec
- Up to 7.6 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5 and 6
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor

Contact factory for options, number of channels, recording rates, and disk capacity.
SystemFlow Graphical User Interface

The RTR 2736 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The RTR 2736 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP’s copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2736 from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2736 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation

Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 2.0 GHz or greater
SDRAM: 6 GB
Monitor: Built-in 17” high-resolution LCD, 1440 x 900 pixels, 200 nits
RAID
  Storage: 1.9, 3.8, or 7.6 TB
  Supported RAID Levels: 0, 1, 5 and 6
  Drive Bays: Hot-swap, removable, rear panel
USB 2.0 Ports: Eight left side, two front panel
USB 3.0 Ports: Two left side
1 Gb Ethernet Port: One left side
eSATA Ports: Two left side
Aux Video Output: 15-pin VGA left side

Serial FPDP Interface

Copper - Option 280
  Cable: 100-ohm shielded twin-ax
  Connector Type: SFP+
  Max. Cable Length: 20 m
Multi-mode Fiber Optical - Option 281
  Cable: Multi-mode fiber, 850 nm
  Connector Type: LC
  Max. Cable Length: Up to 300 m
Single-mode Fiber Optical - Option 282
  Cable: Single-mode fiber
  Connector Type: LC
  Max. Cable Length: Up to 10 km

Physical and Environmental

Dimensions: 16.9” W x 9.5” D x 13.4” H
Weight: 30 lb, approximately
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTR 2736 Ordering Information and Options

<table>
<thead>
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<th>Storage Options</th>
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<td>Option -405</td>
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<tr>
<td>4-channel recording</td>
<td>1.9 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -208</td>
<td>Option -410</td>
</tr>
<tr>
<td>8-channel recording</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td></td>
<td>Option -415</td>
</tr>
<tr>
<td></td>
<td>7.6 TB SSD storage capacity</td>
</tr>
</tbody>
</table>

Serial FPDP Interface (append to all options)

Option -280 Copper, SFP+ connectors
Option -281 Multi-mode optical, LC connectors
Option -282 Single-mode optical, LC connectors

General Options (append to all options)

Option -261 GPS time & position stamping
Option -264 IRIG-B time stamping

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

The Talon® RTR 2736A is a complete turn-key recording system capable of recording and playing back multiple Serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.2 GB/sec.

The RTR 2736A can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125, and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per Serial FPDP link.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

SystemFlow Software

The RTR 2736A includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows workstation, the RTR 2736A allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2736A records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive. Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

Rugged Chassis with SSD Storage

The RTR 2736A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

Features

- Designed to operate under conditions of shock and vibration
- Portable system measuring 16.0” W x 6.9” D x 13.0” H
- Lightweight, just less than 30 pounds
- Shock- and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Up to eight I/O channels
- Supports Flow Control, CRC, and Copy/Loop Mode as a receiver and transmitter
- Supports 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates
- Copper, single-mode and multi-mode fiber interfaces available
- Real-time aggregate recording rates of up to 3.2 GB/sec
- Windows® workstation with high performance Intel® Core™ i7 processor
- Up to 61 terabytes of SSD storage to NTFS RAID solid state disk array
- SystemFlow® GUI with Signal Viewer analysis tool
- Optional file headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Optional 10–36 VDC power supply

Contact factory for options, number of channels, recording rates, and disk capacity.
➤ SystemFlow Graphical User Interface

SystemFlow Main Interface
The RTR 2736A GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface
The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP's copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface
The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
SystemFlow API
SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2736A from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2736A as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications
PC Workstation (standard configuration)
Operating System: 64-bit Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
Operating System Drive: 128 GB SSD
SDRAM: 8 GB
Monitor: Built-in 17.3" high-resolution LCD, 1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface
Brightness: 300 cd/m²; Contrast ratio: 400:1 typical
RAID
Total Storage: 1.9, 3.8, 7.6 or 15.3 TB
Supported RAID Levels: 0, 1, 5 and 6
Drive Bays: Hot-swap, removable, side panel
USB 2.0 Ports: Four on left side, two on front panel
USB 3.0 Ports: Two on left side
1 Gb Ethernet Ports: Two on left side
Aux Video Output: 15-pin VGA on left side

Serial FPDP Interface
Copper - Option 280
  Cable: 100-ohm shielded twin-ax
  Connector Type: SFP+
  Max. Cable Length: 20 m
Multi-mode Fiber Optical - Option 281
  Cable: Multi-mode fiber, 850 nm
  Connector Type: LC
  Max. Cable Length: Up to 300 m
Single-mode Fiber Optical - Option 282
  Cable: Single-mode fiber
  Connector Type: LC
  Max. Cable Length: Up to 10 km

Optional DC Power supply
  Voltage: 18 to 36 VDC
  Input Current: 42 to 26 A (39 A at 24 VDC)
  Inrush Current: 100 A at 24 VDC
  Temperature Range: Oper.: 0° to 50° C; Store: –0° to 80° C
  Efficiency: >80% typical at 24 V full load
  Power Good Signal: On delay 100 to 500 msec
  OverPower Protection: 110% to 160%
  Remote Control: On/Off
  Safety: Meets UL, TUV, CB specifications

Physical and Environmental
Size: 16.0” W x 6.9” D x 13.0” H
Weight: 30 lb max.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 30 g max. (11 msec, half-sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak,
  20 to 500 Hz: 1.4 g peak acceleration
Non-operating Vibration: 5 to 500 Hz: 2.06 g RMS
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Channel Configurations
<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-204</td>
<td>4-channel recording</td>
</tr>
<tr>
<td>-208</td>
<td>8-channel recording</td>
</tr>
</tbody>
</table>

Storage Options
<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-405</td>
<td>1.9 TB SSD storage capacity</td>
</tr>
<tr>
<td>-410</td>
<td>3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>-415</td>
<td>7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td>-420</td>
<td>15.3 SSD storage capacity</td>
</tr>
</tbody>
</table>

Serial FPDP Interface (append to all options)
<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-280</td>
<td>Copper, SFP+ connectors</td>
</tr>
<tr>
<td>-281</td>
<td>Multi-mode optical, LC connectors</td>
</tr>
<tr>
<td>-282</td>
<td>Single-mode optical, LC connectors</td>
</tr>
</tbody>
</table>

General Options (append to all options)
<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-261</td>
<td>GPS time &amp; position stamping</td>
</tr>
<tr>
<td>-264</td>
<td>IRIG-B time stamping</td>
</tr>
<tr>
<td>-625</td>
<td>Removable operating system drive</td>
</tr>
<tr>
<td>-681</td>
<td>18 to 36 VDC Power Supply</td>
</tr>
</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

The Talon® RTR 2756 is a complete turn-key recording system capable of recording and playing back multiple Serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.2 GB/sec.

The RTR 2756 can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multimode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per Serial FPDP link.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file's header.

SystemFlow Software

The RTR 2756 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2756 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2756 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2756 performs well in ground, shipborne and airborne environments. Configurable with hot-swappable SSDs, the RTR 2756 can provide storage capacities of up to 46 TB in a rugged chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2756 is configured in a 4U 19” rack-mountable chassis, with hot-swap data drives, front-panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50 provide a choice for the required level on redundancy. Redundant power supplies are optionally available to provide a robust and reliable high-performance recording system. ▶

Contact factory for options, for number and type of channels, recording rates, and disk capacity.

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
**SystemFlow Graphical User Interface**

The RTR 2756 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

**SystemFlow Main Interface**

The RTR 2756 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

**SystemFlow Hardware Configuration Interface**

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP's copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Record Interface**

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
➤ SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2756 from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2756 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation

- Operating System: Windows 7 Professional
- Processor: Intel Core i7 processor
- Clock Speed: 2.0 GHz or greater
- SDRAM: 6 GB
- RAID
  - Storage: 3.8, 7.6, 15.3, 30.7 or 46.0 TB
  - Supported Levels: 0, 1, 5, 6, 10 and 50

Serial FPDP Interface

- Copper - Option 280
  - Cable: 100-ohm shielded twin-ax
  - Connector Type: SFP+
  - Max. Cable Length: 20 m
- Multi-mode Fiber Optical - Option 281
  - Cable: Multi-mode fiber, 850 nm
  - Connector Type: LC
  - Max. Cable Length: Up to 300 m
- Single-mode Fiber Optical - Option 282
  - Cable: Single-mode fiber
  - Connector Type: LC
  - Max. Cable Length: Up to 10 km

Physical and Environmental

- Dimensions & Weights
  - All options except 085: 19” W x 21” D x 7” (4U) H
  - Weight: 50 lb, approx.
  - Option 085: 19” W x 26” D x 7” (4U) H
  - Weight: 65-90 lb
- Operating Temp: 0° to +50° C
- Storage Temp: -40° to +85° C
- Relative Humidity: 5 to 95%, non-condensing
- Operating Shock: 15 g max. (11 msec, half sine wave)
- Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz; 1.4 g peak acceleration

Specifications are subject to change without notice

Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information
**General Information**

The Talon® RTX 2776 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2776 is intended for military, airborne and UAV applications requiring a rugged system.

The Talon RTX 2776 is a complete turn-key recording system capable of recording and playing back multiple Serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.2 GB/sec.

The RTX 2776 can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

**SystemFlow Software**

The RTX 2776 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTX 2776 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTX 2776 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

**Rugged Mil-Spec Chassis**

The Talon RTX 2776 uses a shock and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.
Model RTX 2776

Serial FPDP Extreme Rackmount Recorder

➤ SystemFlow Graphical User Interface

The RTX 2776 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The RTX 2776 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP’s copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTX 2776 from a custom application. High-level C-language function calls and the supporting device drivers allow users to incorporate the RTX 2776 as a high-performance server front-end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation (standard configuration)

Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB

Data Storage
Style: Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister
Location: Front panel
Capacity: Up to 30 TB
Number of Drives: Up to 32 total
Supported RAID Levels: 0, 1, 5 and 6

Serial FPDP Interface

Copper - Option 280
  Cable: 100-ohm shielded twin-ax
  Connector Type: SFP+
  Max. Cable Length: 20 m

Multi-mode Fiber Optical - Option 281
  Cable: Multi-mode fiber, 850 nm
  Connector Type: LC
  Max. Cable Length: Up to 300 m

Single-mode Fiber Optical - Option 282
  Cable: Single-mode fiber
  Connector Type: LC
  Max. Cable Length: Up to 10 km

Physical and Environmental

Dimensions: 19" W x 22" D x 7" H
Weight: 50 lb, approx.
Operating Temp: -20° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 10% to 95%, non-condensing

Operating Shock: Designed to MIL-STD 810F, method 514.5, procedures I and VI
Operating Vibration: Designed to MIL-STD 810F, method 514.5, procedure I

EMI/EMC: Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS103
Input Power: 85 to 264 VAC, 47– 400 Hz, 600 W max.

Model RTX 2776 Ordering Information and Options

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<td>Option -410</td>
</tr>
<tr>
<td>4-channel record/payback</td>
<td>3.8 TB SSD storage</td>
</tr>
<tr>
<td>Option -208</td>
<td>Option -415</td>
</tr>
<tr>
<td>8-channel record/playback</td>
<td>7.6 TB SSD storage</td>
</tr>
<tr>
<td>Option -280</td>
<td>Option -418</td>
</tr>
<tr>
<td>Serial FPDP Interface</td>
<td>11.5 TB SSD storage</td>
</tr>
<tr>
<td>Option -281</td>
<td>Option -420</td>
</tr>
<tr>
<td>SFP + connectors</td>
<td>15.3 TB SSD storage</td>
</tr>
<tr>
<td>Option -282</td>
<td>Option -425</td>
</tr>
<tr>
<td>Multi-mode optical, LC connectors</td>
<td>23.0 TB SSD storage</td>
</tr>
<tr>
<td></td>
<td>Option -430</td>
</tr>
<tr>
<td></td>
<td>30.7 TB SSD storage</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>General Options (append to all options)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Option -261</td>
</tr>
<tr>
<td>GPS time and position stamping</td>
</tr>
<tr>
<td>Option -264</td>
</tr>
<tr>
<td>IRIG-B Time Stamping</td>
</tr>
<tr>
<td>Option -680</td>
</tr>
<tr>
<td>28 VDC power supply</td>
</tr>
<tr>
<td>Option -625</td>
</tr>
<tr>
<td>Front-panel removable OS drive</td>
</tr>
</tbody>
</table>

Contact Pentek for other configurations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

The Talon® RTS 2718 is a complete turn-key system for recording and playing back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves sustained recording rates of up to 1.6 GB/sec.

The RTS 2718 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTS 2718 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTS 2718 allows the user to install post-processing and analysis tools to operate on the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or eight USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD±R/RW drive.

Flexible Architecture

The RTS 2718 is configured in a 4U 19” rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. Up to 16 hot-swappable SATA drives are optionally available, allowing up to 20 terabytes of real-time data storage space in a single 4U chassis.

SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) that supports control and status queries of all operations of the RTS 2718 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTS 2718 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Features

- 32 bits of LVDS digital I/O
- LVDS clock, Data Valid and Data Suspend signals
- Supports clock rates up to 250 MHz
- Real-time aggregate recording rates up to 1.6 GB/s
- Up to 20 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 1, 5, 6, 10 and 50
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor

Contact factory for options, recording rates, and disk capacity.
SystemFlow Graphical User Interface

SystemFlow Main Interface
The RTS 2718 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface
The Configure screen presents operational system parameters including temperature and voltages. These parameters include data valid and suspend enables, as well as polarity control for both signals. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface
The SystemFlow Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
Model RTS 2718

LVDS Digital I/O Rackmount Recorder

Specifications

PC Workstation
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB
RAID
Storage: 2.0–100.0 TB
Drive Type: 3.5” HDD
Supported RAID Levels: 0, 1, 5, 6, 10 and 50

LVDS Interface
Cable: 80-pin ribbon cable
Connector Type: 2x40 pin IDC
Data Lines: 32 LVDS pairs, 2.5 V compliant
Clock: One LVDS pair, 2.5 V compliant
Data Valid: One LVDS pair, 2.5 V compliant
Data Suspend: One LVDS pair, 2.5 V compliant

Physical and Environmental
Dimensions
4U Long Chassis: 19” W x 26” D x 7” H
Size: 19” W x 26” D x 7” H
Weight: 50-80 lb
Operating Temp: +5° to +45° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 500 W max.

Model RTS 2716 Ordering Information and Options

Channel Configuration
Option -201 Recording interface
Option -221 Playback interface

Storage Options
Option -406 2.0 TB HDD storage capacity
Option -411 4.0 TB HDD storage capacity
Option -416 8.0 TB HDD storage capacity
Option -421 16.0 TB HDD storage capacity
Option -423 20.0 TB HDD storage capacity
Option -439 30.0 TB HDD storage capacity
Option -450 45.0 TB HDD storage capacity
Option -460 60.0 TB HDD storage capacity
Option -480 100.0 TB HDD storage capacity

Note: Options -450 and -460 require a 5U Chassis; Option -480 requires a 6U chassis

General Options (append to all options)
Option -261 GPS time & position stamping
Option -264 IRIG-B time stamping

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications subject to change without notice
General Information

The Talon® RTR 2738A is a complete turn-key system for recording and playing back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the rugged, lightweight portable package achieves sustained recording rates of up to 1.0 GB/sec.

The RTR 2738A utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

SystemFlow Software

The RTR 2738A includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system. It also includes a C-callable API that allows users to easily integrate the Talon recorder into a larger system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2738A allows the user to install post-processing and analysis tools to operate on the recorded data.

Data can be off-loaded via gigabit Ethernet, USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Option -625 replaces the DVD±R/RW drive with a removable operating system drive; an external DVD drive can be used.

Rugged Chassis with SSD Storage

The RTR 2736A is configured with hot-swappable SSDs, front panel USB ports, and I/O connectors on the side panel. It is built in an extremely rugged steel and aluminum chassis and is tested for shock and vibration. The SSDs provide storage capacities of up to 61.4 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Multiple RAID levels, including 0, 5, and 6, provide a choice for the required level of redundancy.

SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) that supports control and status queries of all operations of the RTR 2738A from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2738A as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Contact factory for options, recording rates, and disk capacity.
SystemFlow Graphical User Interface

SystemFlow Main Interface

The RTR 2738A GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. These parameters include data valid and suspend enables, as well as polarity control for both signals. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The SystemFlow Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
## Specifications

**PC Workstation (standard configuration)**  
**Operating System:** 64-bit Windows workstation  
**Processor:** Intel Core i7 processor  
**Clock Speed:** 3.0 GHz or higher  
**Operating System Drive:** 128 GB SSD  
**SDRAM:** 8 GB  
**Monitor:** Built-in 17.3” high-resolution LCD,  
1920 x 1080 pixels, 16:9 aspect ratio, anti-glare surface  
Brightness: 300 cd/m²; Contrast ratio: 400:1 typical  

**RAID**  
**Total Storage:** 3.8 – 61.4 TB  
**Supported RAID Levels:** 0, 5 and 6  
**Drive Bays:** Hot-swap, removable, side panel  
**USB 2.0 Ports:** Four on left side, two on front panel  
**USB 3.0 Ports:** Two on left side  
**1 Gb Ethernet Ports:** Two on left side  
**Aux Video Output:** 15-pin VGA on left side  

**LVDS Interface**  
**Cable:** 80-pin ribbon cable  
**Connector Type:** 2x40 pin IDC  
**Data Lines:** 32 LVDS pairs, 2.5 V compliant  
**Clock:** One LVDS pair, 2.5 V compliant  
**Data Valid:** One LVDS pair, 2.5 V compliant  
**Data Suspend:** One LVDS pair, 2.5 V compliant  

## Optional DC Power supply  
**Voltage:** 10 to 36 VDC  
**Input Current:** 42 to 26 A (39 A at 24 VDC)  
**Inrush Current:** 100 A at 24 VDC  
**Temperature Range:** Oper.: 0° to 50° C, Store: −0° to 80° C  
**Efficiency:** >80% typical at 24 V full load  
**Power Good Signal:** On delay 100 to 500 msec  
**OverPower Protection:** 110% to 160%  
**Remote Control:** On/Off  
**Safety:** Meets UL, TUV, CB specifications  

## Physical and Environmental  
**Size:** 16.0” W x 6.9” D x 13.0” H  
**Weight:** 30 lb max.  
**Operating Temp:** 0° to +50° C  
**Storage Temp:** −40° to +85° C  
**Relative Humidity:** 5 to 95%, non-condensing  
**Operating Shock:** 30 g max. (11 msec, half-sine wave)  
**Operating Vibration:** 10 to 20 Hz: 0.02 inch peak,  
20 to 500 Hz: 1.4 g peak acceleration  
**Non-operating Vibration:** 5 to 500 Hz: 2.06 g RMS  
**Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 500 W max.  

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### Model RTR 2738A Ordering Information and Options

<table>
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<th>Channel Configurations</th>
<th>Additional Options</th>
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**Option -261** GPS Time & Position Stamping  
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**Option -285** RAID 5 Configuration  
**Option -286** RAID 6 Configuration  
**Option -309** 16 GB System Memory  
**Option -311** 64 GB System Memory  
**Option -625** Removable Operating System Drive  
**Option -681** 10 to 36 VDC Power Supply  |

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<tr>
<th>Storage Options</th>
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</table>
| **Option -410** 3.8 TB SSD Storage  
**Option -415** 7.6 TB SSD Storage  
**Option -420** 15.3 TB SSD Storage  
**Option -430** 30.7 TB SSD Storage  
**Option -460** 61.4 TB SSD Storage  |

Contact Pentek for compatible Option combinations  
Storage and Channel-count Options may change, contact Pentek for the latest information  

Specifications are subject to change without notice
General Information

The Talon® RTR 2758 is a complete turn-key system for recording and playing back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves sustained recording rates of up to 1.0 GB/sec.

The RTR 2758 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTR 2758 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2758 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2758 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2758 performs well in ground, shipborne and airborne environments. Configurable with hot-swappable SSDs, the RTR 2758 can provide storage capacities of up to 46 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2758 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50 provide a choice for the required level on redundancy. Redundant power supplies are optionally available to provide a robust and reliable high-performance recording system.

Contact factory for options, recording rates, and disk capacity.
➤ SystemFlow Graphical User Interface

SystemFlow Main Interface

The RTR 2758 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. These parameters include data valid and suspend enables, as well as polarity control for both signals. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
Model RTR 2758
LVDS Digital I/O Rugged Rackmount Recorder

➤ SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) that supports control and status queries of all operations of the RTR 2758 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2758 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation
Operating System: Windows 7 Professional
Processor: Intel Core i7 processor
Clock Speed: 3.0 GHz or higher
SDRAM: 8 GB
RAID
Storage: 3.8, 7.6, 15.3, 30.7 or 46.0 TB
Supported Levels: 0, 1, 5, 6, 10 and 50

LVDS Interface
Cable: 80-pin ribbon cable
Connector Type: 2x40 pin IDC
Data Lines: 32 LVDS pairs, 2.5 V compliant
Clock: One LVDS pair, 2.5 V compliant
Data Valid: One LVDS pair, 2.5 V compliant
Data Suspend: One LVDS pair, 2.5 V compliant

Physical and Environmental
Dimensions & Weights
Dimensions: 19" W x 21" D x 7" (4U) H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Operating Shock: 15 g max. (11 msec, half sine wave)
Operating Vibration: 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz; 1.4 g peak acceleration

Specifications are subject to change without notice
Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Model RTR 2758 Ordering Information and Options

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<td>Option -410 3.8 TB SSD storage capacity</td>
</tr>
<tr>
<td>Option -221 Playback interface</td>
<td>Option -415 7.6 TB SSD storage capacity</td>
</tr>
<tr>
<td></td>
<td>Option -420 15.3 TB SSD storage capacity</td>
</tr>
<tr>
<td></td>
<td>Option -430 30.7 TB SSD storage capacity</td>
</tr>
<tr>
<td></td>
<td>Option -440 46.0 TB SSD storage capacity</td>
</tr>
<tr>
<td></td>
<td>Note: Options -430 and -440 require 26-inch deep chassis</td>
</tr>
</tbody>
</table>

General Options (append to all options)
Option -261 GPS time & position stamping
Option -264 IRIG-B time stamping

Contact Pentek for compatible Option combinations
Specifications are subject to change without notice
**General Information**

The Talon® RTX 2778 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2778 is intended for military, airborne and UAV applications requiring a rugged system.

The RTX 2778 records and plays back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves aggregate recording rates of up to 1.0 GB/sec.

The RTX 2778 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

Optional GPS time and position stamping accurately identifies each record in the file header.

**SystemFlow Software**

The RTX 2778 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTX 2778 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTX 2778 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two rear-access gigabit Ethernet ports, two USB 3.0 ports or up to four USB 2.0 ports.

**Rugged Mil-Spec Chassis**

The Talon RTX 2778 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. The chassis uses an in-line EMI filter along with rear-panel MIL-style connectors to meet MIL-STD-461 emissions specifications.

Up to four front-panel removable QuickPac drive canisters are provided, each containing up to eight SSDs. Each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data.

Forced-air cooling draws air from the front of the chassis and pushes it out the back via exhaust fans. A hinged front door with a serviceable air filter provides protection against dust and sand.
SystemFlow Graphical User Interface

The RTX 2778 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The RTX 2778 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Record Interface

The SystemFlow Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. These parameters include data valid and suspend enables, as well as polarity control for both signals. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
**SystemFlow API**

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTX 2776 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTX 2776 as a high-performance server front-end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

**Specifications**

**PC Workstation (standard configuration)**

**Operating System:** Windows 7 Professional  
**Processor:** Intel Core i7 processor  
**Clock Speed:** 3.0 GHz or higher  
**SDRAM:** 8 GB

**Data Storage**

- **Style:** Up to four front-panel removable QuickPac drive canisters; up to eight SSDs contained in each canister  
- **Location:** Front panel  
- **Capacity:** Up to 30 TB  
- **Number of Drives:** Up to 32 total  
- **Supported RAID Levels:** 0, 1, 5 and 6

**LVDS Interface**

- **Cable:** 80-pin ribbon cable  
- **Connector Type:** 2x40 pin IDC  
- **Data Lines:** 32 LVDS pairs, 2.5 V compliant  
- **Clock:** One LVDS pair, 2.5 V compliant  
- **Data Valid:** One LVDS pair, 2.5 V compliant  
- **Data Suspend:** One LVDS pair, 2.5 V compliant

**Physical and Environmental**

- **Dimensions:** 19” W x 22” D x 7” H  
- **Weight:** 50 lb, approx.  
- **Operating Temp:** –20° to +50° C  
- **Storage Temp:** –40° to +85° C  
- **Relative Humidity:** 10% to 95%, non-condensing  
- **Operating Shock:** Designed to MIL-STD 810F, method 514.5, procedures I and VI  
- **Operating Vibration:** Designed to MIL-STD 810F, method 514.5, procedure I  
- **EMI/EMC:** Designed to MIL-STD 461E, CE101, CE102, CS101, CS113, RE101, RE102, RS101, RS103  
- **Input Power:** 85 to 264 VAC, 47– 400 Hz, 600 W max.

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**Model RTX 2778 Ordering Information and Options**

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<td>Option -221</td>
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<td>Option -418</td>
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<td>Option -420</td>
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<td>Option -425</td>
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<td>Option -430</td>
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<td></td>
<td><strong>General Options (append to all options)</strong></td>
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<td></td>
<td>Option -261</td>
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<td></td>
<td>Option -264</td>
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<td></td>
<td>Option -680</td>
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<td></td>
<td>Option -625</td>
</tr>
</tbody>
</table>

**Contact Pentek for other configurations**

Storage and Channel-count Options may change, contact Pentek for the latest information.

*Specifications are subject to change without notice*
Model RTR 2555

1-, 10-, 40-Gigabit Ethernet Rugged SFF Recorder

General Information

Optimized for SWaP (size, weight and power) the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

The Talon® RTR 2555 is a complete turnkey recording and playback system for storing 1-, 10- and 40-gigabit Ethernet streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

An ATX power supply accepts 110-240 V AC, drawing under 150 W and typically around 100 W. These models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTR 2555 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2555 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2555 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2555 performs well in ground, shipborne and airborne environments.

Configurable with hot-swappable SSDs, the RTR 2555 can provide storage capacities of up to 30.6 TB in a rugged chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2555 is configured with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 5 and 6 provide a choice for the required level of redundancy.

Features

- Housed in a small chassis measuring 5.25” H x 8.5” W x 14” D
- Weighs 17 lb (7.7 kg)
- Shock and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Records gigabit, 10-gigabit or 40-gigabit Ethernet streams
- TCP and UDP protocols
- Copper or optical interfaces
- Aggregate recording rates to 4.0 GB/sec
- Up to 30 terabytes of storage to NTFS RAID disk array
- RAID levels of 0, 5 and 6
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into applications
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
**SystemFlow Graphical User Interface**

The RTR 2555 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

**SystemFlow Main Interface**

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Hardware Configuration Interface**

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Record Interface**

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
**Model RTR 2555**

1-, 10-, 40-Gigabit Ethernet Rugged SFF Recorder

➤ **SystemFlow API**

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2555 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2555 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

**Specifications**

**PC Workstation (standard configuration)**

- **Operating System:** Windows workstation
- **Processor:** Intel i7 7700K (7th Gen) quad core processor
- **Clock Speed:** 4.2 GHz
- **Operating System Drive:** 250 GB SSD
- **SDRAM:** 8 standard, 16 or 32 GB optional
- **RAID**
  - **Total Storage:** 3.8 TB – 30.6 TB
  - **Supported RAID Levels:** 0, 5 and 6
  - **Drive Bays:** Hot-swap, removable, front panel

**Rear Panel I/O**

- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

**Front Panel I/O**

- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

**Physical and Environmental**

- **Size:** 5.25” H x 8.5” W x 14.0” D
- **Weight:** 17 lb (7.7 kg)
- **Operating Temp:** 0° to +50° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 15 g max. (11 msec, half-sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 150 W max.

**Ethernet Interface Options**

- **Option -101** Gigabit Ethernet
- **Option -102** 10-Gigabit Ethernet
- **Option -103** 40-Gigabit Ethernet

**Channel Configuration**

- **Option -201** 1-Ethernet port
- **Option -202** 2-Ethernet ports
- **Option -204** 4-Ethernet ports

**Ethernet Connector Options**

- **Option -280** SFP + connectors
- **Option -281** Multi-mode optical, LC connectors
- **Option -282** Single-mode optical, LC connectors
- **Option -284** RJ 45 connectors

**Storage Options**

- **Option -410** 3.8 TB SSD storage
- **Option -415** 7.6 TB SSD storage
- **Option -420** 15.3 TB SSD storage
- **Option -430** 30.6 TB SSD storage

**General Options**

- **Option -261** GPS Time and Position Stamping
- **Option -285** Raid 5 Configuration
- **Option -286** Raid 6 Configuration
- **Option -309** 16 GB System Memory
- **Option -310** 32 GB System Memory
- **Option -630** 6 to 30 VDC Power Supply

Contact Pentek for other configurations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
General Information

Optimized for SWaP (size, weight and power) the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

Configured as a complete turnkey system capable of recording and playing back multiple Serial FPDP data streams, it is ideal for capturing any type of streaming sources such as live transfers from sensors or data from other computers. It is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 3.2 GB/sec.

The RTR 2556 can be populated with up to four SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 425 MB/sec per Serial FPDP link.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds.

SystemFlow Software

The RTR 2556 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system.

Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2556 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2556 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB 2.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD+R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2556 performs well in ground, shipborne and airborne environments. Configurable with hot-swappable SSDs, the RTR 2556 can provide storage capacities of up to 30.6 TB in a rugged chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2556 is configured with hot-swap data drives, front-panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. Multiple RAID levels, including 0, 5, and 6 provide a choice for the required level of redundancy.

Features

- Housed in a small chassis measuring 5.25” H x 8.5” W x 14” D
- Weighs 17 lb (7.7 kg)
- Shock and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- Complete Serial FPDP record and playback system
- Up to four I/O channels
- Removable SSDs
- Up to 30 terabytes of storage to NTFS RAID disk array
- Copper, single-mode and multi-mode fiber interfaces available
- Real-time aggregate recording rates of up to 1.6 GB/sec
- Supports Flow Control, CRC, and Copy/Loop Mode as a receiver and transmitter
- Supports 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates
- RAID levels of 0, 5 and 6
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor

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Model RTR 2556

Serial FPDP Rugged SFF Recorder

Pentek, Inc., One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com

www.pentek.com
SystemFlow Graphical User Interface

The RTR 2556 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Main Interface

The SystemFlow Main Interface includes Configure, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface

The Configure screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying the flow control settings and the recognition of a CRC in the data stream. Each channel can also be set up to utilize Serial FPDP's copy/loop mode. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface

The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.
SystemFlow API

SystemFlow includes a complete API (Application Programming Interface) supporting control and status queries of all operations of the RTR 2556 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2556 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet port, either to a local host or through an internet link for remote, stand-alone acquisition. Recorded NTFS files can be easily retrieved through the same connection.

Specifications

PC Workstation (standard configuration)

- **Operating System:** Windows workstation
- **Processor:** Intel i7 7700K (7th Gen) quad core processor
- **Clock Speed:** 4.2 GHz
- **Operating System Drive:** 250 GB SSD
- **SDRAM:** 8 standard, 16 or 32 GB optional
- **RAID:**
  - **Total Storage:** 3.8 TB – 30.6 TB
  - **Supported RAID Levels:** 0, 5 and 6
  - **Drive Bays:** Hot-swap, removable, front panel

Rear Panel I/O

- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

Front Panel I/O

- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

Physical and Environmental

- **Size:** 5.25” H x 8.5” W x 14.0” D
- **Weight:** 17 lb (7.7 kg)
- **Operating Temp:** 0° to +50° C
- **Storage Temp:** -40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 15 g max. (11 msec, half-sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 150 W max.

Model RTR 2556 Ordering Information and Options

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Contact Pentek for compatible Option combinations

Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice
Model RTR 2558
LVDS Digital I/O Rugged SFF Recorder

General Information

Optimized for SWaP (size, weight and power) the Pentek Talon® RTR Small Form Factor (SFF) product line provides the performance and storage capacity previously only possible in much larger rackmountable chassis. Measuring 5.25” H x 8.5” W x 14” D and weighing only 17 pounds (7.7 kg), this small package can hold up to 30.6 TB of SSD storage.

The Talon® RTR 2558 is a complete turn-key system for recording or playing back digital data. Using highly optimized disk storage technology, the system achieves sustained recording rates of up to 1.0 GB/sec.

The RTR 2758 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

An ATX power supply accepts 110-240 VAC, drawing under 150 W and typically around 100 W. These models have the option for a 6-30 VDC power supply.

Eight front panel data drives can be easily removed along with a front panel removable OS drive to allow all non-volatile memory to be removed from the system in seconds.

Optional GPS time and position stamping accurately identifies each record in the file header.

SystemFlow Software

The RTR 2558 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2758 allows the user to install post-processing and analysis tools to operate on the recorded data.

The RTR 2558 records data to the native NTFS file system, providing immediate access to the recorded data.

Data can be off-loaded via two gigabit Ethernet ports or six USB ports. Additionally, data can be copied to optical disk using the 8X double layer DVD±R/RW drive.

Rugged and Flexible Architecture

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2758 performs well in ground, shipborne and airborne environments.

Configurable with hot-swappable SSDs, the RTR 2558 can provide storage capacities of up to 30.6 TB in a rugged chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.

The RTR 2558 is configured with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.

Multiple RAID levels, including 0, 5, and 6 provide a choice for the required level of redundancy.

Features

- Housed in a small chasis measuring 5.25” H x 8.5” W x 14” D
- Weighs 17 lb (7.7 kg)
- Shock and vibration-resistant SSDs perform well in vehicles, ships and aircraft
- 32 bits of LVDS digital I/O
- LVDS clock, Data Valid and Data Suspend signals
- Supports clock rates up to 250 MHz
- Real-time aggregate recording rates up to 1.0 GB/sec
- Up to 30 terabytes storage to NTFS RAID disk array
- RAID levels of 0, 5, and 6
- SystemFlow® GUI virtual instrumentation panel for fast, intuitive operation
- C-callable API for integration of recorder into application
- File headers include time stamping and recording parameters
- Optional GPS time and position stamping
- Windows® 7 Professional workstation with high-performance Intel® Core™ i7 processor
Model RTR 2558 LVDS Digital I/O Rugged SFF Recorder

➤ SystemFlow Graphical User Interface

SystemFlow Main Interface
The RTR 2558 GUI shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configure, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to configure parameters, control and monitor a recording, and play back a recorded stream.

SystemFlow Hardware Configuration Interface
The Configure screen presents operational system parameters including temperature and voltages. These parameters include data valid and suspend enables, as well as polarity control for both signals. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

SystemFlow Record Interface
The Record screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress. ➤
**Model RTR 2558**  
LVDS Digital I/O Rugged SFF Recorder

➤ **SystemFlow API**

SystemFlow includes a complete API (Application Programming Interface) that supports control and status queries of all operations of the RTR 2558 from a custom application.

High-level C-language function calls and the supporting device drivers allow users to incorporate the RTR 2558 as a high-performance server front end to a larger system. This is supported using a socket interface through the Ethernet interface.

** Specifications**

**PC Workstation (standard configuration)**

- **Operating System:** Windows workstation
- **Processor:** Intel i7 7700K (7th Gen) quad core processor
- **Clock Speed:** 4.2 GHz
- **Operating System Drive:** 250 GB SSD
- **SDRAM:** 8 standard, 16 or 32 GB optional

**RAID**

- **Total Storage:** 3.8 TB – 30.6 TB
- **Supported RAID Levels:** 0, 5 and 6
- **Drive Bays:** Hot-swap, removable, front panel

**Rear Panel I/O**

- Four USB 3.0 ports
- Two Gigabit RJ45 ports
- Two HDMI and One DVI ports
- Audio and PS2 ports
- USB 3.0 Type-C port
- Two Wi-Fi antenna ports

**Front Panel I/O**

- Two USB 2.0 ports
- Power and recessed RESET buttons
- LED indicators for power and HDD access

**LVDS Interface**

- **Cable:** 80-pin ribbon cable
- **Connector Type:** 2x40 pin IDC
- **Data Lines:** 32 LVDS pairs, 2.5 V compliant
- **Clock:** One LVDS pair, 2.5 V compliant
- **Data Valid:** One LVDS pair, 2.5 V compliant
- **Data Suspend:** One LVDS pair, 2.5 V compliant

**Physical and Environmental**

- **Size:** 5.25” H x 8.5” W x 14.0” D
- **Weight:** 17 lb (7.7 kg)
- **Operating Temp:** 0° to +50° C
- **Storage Temp:** –40° to +85° C
- **Relative Humidity:** 5 to 95%, non-condensing
- **Operating Shock:** 15 g max. (11 msec, half-sine wave)
- **Operating Vibration:** 10 to 20 Hz: 0.02 inch peak, 20 to 500 Hz: 1.4 g peak acceleration
- **Power Requirements:** 100 to 240 VAC, 50 to 60 Hz, 150 W max.

**Model RTR 2558 Ordering Information and Options**

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<td><strong>Option -410</strong> 3.8 TB SSD storage capacity</td>
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</tr>
<tr>
<td><strong>Option -630</strong></td>
<td>6 to 30 VDC Power Supply</td>
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</tbody>
</table>

Contact Pentek for compatible Option combinations
Storage and Channel-count Options may change, contact Pentek for the latest information

Specifications are subject to change without notice

Pentek, Inc., One Park Way • Upper Saddle River • New Jersey 07458  
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com  
www.pentek.com
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We’re glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at: 

www.pentek.com

Customer Service phone: 201-818-5900  •  fax: 201-818-5697  •  email: custsvc@pentek.com

www.pentek.com
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<td>5694</td>
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<td>9190</td>
<td>Clock and Sync Generator for I/O Modules</td>
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<td>9192</td>
<td>Rack-mount High-Speed System Synchronizer Unit</td>
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Customer Information
Multifrequency Clock Synthesizer - PMC

Model 7190

General Information

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7190 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications

Front Panel Reference Input
Connector Type: SMC
Input Impedance: 50 ohms
Reference Frequency: 5 to 100 MHz
Input Level: -6 dBm to +10 dBm
PLL Clock Synthesizers & Jitter Cleaners
Quantity: Four
Type: Texas Instruments CDC7005
Frequency Dividers: 1, 2, 4, 8 and 16
Quad VCXOs (Quantity: Four)
Frequencies per VCXO: 4*, software-programmable
Frequency Range: 50 to 700 MHz
Unlocked Accuracy: ±20 ppm
Front Panel Clock Outputs (Quantity: Eight)
Connector Type: SMC
Output Impedance: 50 ohms
Output Level: +3 dBm @ 700 MHz
Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface

PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
Operation: control and status interface

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard PMC module, 2.91 in. x 5.87 in.

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

Ordering Information

Model 7190 Multifrequency Clock Synthesizer - PMC

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-9904 • Email: info@pentek.com

www.pentek.com
Multifrequency Clock Synthesizers - 3U/6U cPCI

General Information
These Models generate up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Models 7290 and 7390 generate eight clocks while Model 7290D generates sixteen.

Clock Synthesizer Circuits
These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005’s can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface
These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications
Front Panel Reference Input
Connector Type: SMC
Input Impedance: 50 ohms
Reference Frequency: 5 to 100 MHz
Input Level: -6 dBm to +10 dBm
PLL Clock Synthesizers & Jitter Cleaners
Quantity: Four or eight
Type: Texas Instruments CDC7005
Frequency Dividers: 1, 2, 4, 8 and 16
Quad VCXOs (Quantity: Four or eight)
Frequencies per VCXO: 4*, software-programmable
Frequency Range: 50 to 700 MHz
Unlocked Accuracy: ±20 ppm
Front Panel Clock Outputs (Quantity: 8 or 16)
Connector Type: SMC
Output Impedance: 50 ohms
Output Level: +3 dBm @ 700 MHz
Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
Operation: control and status interface

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0% to 95%, non-cond.

Size: Standard 3U or 6U cPCI board

Features
- Simultaneous synthesis of up to five different clocks
- Eight or 16 SMC clock outputs
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Quad VCXOs allow selection from different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

Ordering Information

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<td>7290D</td>
<td>Dual Multifrequency Clock Synthesizer - 6U cPCI</td>
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<tr>
<td>7390</td>
<td>Multifrequency Clock Synthesizer - 3U cPCI</td>
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Options
- Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz
- Contact Pentek to order specific frequencies

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Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
Model 7690 Multifrequency Clock Synthesizer - PCI

General Information

Model 7690 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7690 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7690 can be programmed to route any of these 20 frequencies to the board’s five output oscillators.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7690’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7690 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. It attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

Specifications

Front Panel Reference Input
  Connector Type: SMC
  Input Impedance: 50 ohms
  Reference Frequency: 5 to 100 MHz
  Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
  Quantity: Four
  Type: Texas Instruments CDC7005
  Frequency Dividers: 1, 2, 4, 8 and 16
  Quad VCXOs (Quantity: 4)
    Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz
  Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
  Connector Type: SMC
  Output Impedance: 50 ohms
  Output Level: +3 dBm @ 700 MHz
  Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
  PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
  Operation: control and status interface

Environmental
  Operating Temp: 0° to 50° C
  Storage Temp: -20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.

Size: Standard half-length PCI board

Ordering Information

Model 7690 Multifrequency Clock Synthesizer - PCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

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ReadyFlow Board Support Package

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General Information

Model 7890 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7890 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7890 can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7890’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7890 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input

- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: +6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners

- Quantity: Four
- Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16
- Quad VCXOs (Quantity: Four)
- Frequencies per VCXO: 16, software-programmable

Frequency Range: 50 to 700 MHz
- Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)

- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

- PCIe Interface: Gen. 2, x8 width
- PCIe Ports: one x4 port to PCIe bus, one x8 port to PCIe motherboard
- Operation: control and status interface

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe, 4.38 in. x 6.6 in
General Information

Model 5390 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5390 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 5390 can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5390’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Switch

Model 5390 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths.

Specifications

Front Panel Reference Input
- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- Quantity: Four

Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)
- Frequencies per VCXO: 4*, software-programmable

Frequency Range: 50 to 700 MHz
- Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**Multifrequency Clock Synthesizer - 6U OpenVPX**

**General Information**

Models 5790 and 5890 generate up to eight or 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

**Clock Synthesizer Circuits**

These models use four or eight Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005’s can output up to five or 10 different clocks each. These models can be programmed to route any of these frequencies to the board’s five or 10 output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or 10 different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than 10 different clock outputs are required simultaneously, multiple 5890’s can be used and phase-locked with a 5 to 100 MHz system reference.

**Specifications**

**Front Panel Reference Input**
- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: –6 dBm to +10 dBm

**PLL Clock Synthesizers & Jitter Cleaners**
- Quantity: Model 5790: Four
- Model 5890: eight
- Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16

**Quad VCXOs (Quantity: Four or Eight)**
- Frequencies per VCXO: 4*, software-programmable

**Frequency Range:** 50 to 700 MHz
- Unlocked Accuracy: ±20 ppm

**Front Panel Clock Outputs (Eight or 16)**
- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

**PCI-Express Interface**
- PCI Express Bus: Gen. 1, 2 : x4, control and status

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)

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**Features**

- Simultaneous synthesis of up to five or 10 different clocks
- Eight or 16 SMC clock outputs
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

**Ordering Information**

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<td>Multifrequency Clock Synthesizer - 6U VPX Single Density</td>
<td>Specify frequencies of factory-installed quad VCXOs between 50 and 700 MHz</td>
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<tr>
<td>5890</td>
<td>Multifrequency Clock Synthesizer - 6U VPX Double Density</td>
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* Contact Pentek to order specific frequencies
General Information
Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits
The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface
The Model 7191 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications
Front Panel Reference Input
- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- Quantity: Four
- Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16
- Programmable VCXOs (Quantity: Four)
- Frequency Range: 50 to 700 MHz
- Tuning Resolution: 32 bits
- Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: -105 dBC/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
- Operation: control and status interface

Environmental
- Operating Temp: 0° to 50°C
- Storage Temp: -20° to 90°C
- Relative Humidity: 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.
Programmable Multifrequency Clock Synthesizers - 3U/6U cPCI

General Information
These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Models 7291 and 7391 generate eight clocks while Model 7291D generates sixteen.

Clock Synthesizer Circuits
These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005’s can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board’s output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7291D’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface
These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications
Front Panel Reference Input
Connector Type: SMC
Input Impedance: 50 ohms
Reference Frequency: 5 to 100 MHz
Input Level: –6 dBm to +10 dBm
PLL Clock Synthesizers & Jitter Cleaners
Quantity: Four or eight
Type: Texas Instruments CDC7005
Frequency Dividers: 1, 2, 4, 8 and 16
Programmable VCXOs (Quantity: 8 or 16)
Frequency Range: 50 to 700 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
Front Panel Clock Outputs (Quantity: 8 or 16)
Connector Type: SMC
Output Impedance: 50 ohms
Output Level: +3 dBm @ 700 MHz
Typ. Phase Noise: –105 dBc/Hz @ 1 kHz
(dependent on reference source stability)

PCI Interface
PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
Operation: control and status interface

Environmental
Operating Temp: 0°C to 50°C
Storage Temp: –20°C to 90°C
Relative Humidity: 0% to 95%, non-cond.
Size: Standard 3U or 6U cPCI board.

Features
- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

Ordering Information
Model | Description
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7291 | Programmable Multifrequency Clock Synthesizer - 6U cPCI
7291D | Dual Programmable Multifrequency Clock Synthesizer - 6U cPCI
7391 | Programmable Multifrequency Clock Synthesizer - 3U cPCI

Model 7291 and 7391 Block Diagram
Model 7291D doubles all resources except the PCI Bridge

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Tel: 201-818-5900 ◆ Fax: 201-818-5904 ◆ Email: info@pentek.com
www.pentek.com
Model 7691 Programmable Multifrequency Clock Synthesizer - PCI

General Information
Model 7691 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits
The 7691 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7691 can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector. Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7691’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface
The Model 7691 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications
Front Panel Reference Input
Connector Type: SMC
Input Impedance: 50 ohms
Reference Frequency: 5 to 100 MHz
Input Level: –6 dBm to +10 dBm
PLL Clock Synthesizers & Jitter Cleaners
Quantity: Four
Type: Texas Instruments CDC7005
Frequency Dividers: 1, 2, 4, 8 and 16
Programmable VCXOs (Quantity: Four)
Frequency Range: 50 to 700 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
Front Panel Clock Outputs (Quantity: Eight)
Connector Type: SMC
Output Impedance: 50 ohms
Output Level: +3 dBm @ 700 MHz
Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
PCI Bus: 32-bit, 66 MHz (supports 33 MHz)
Operation: control and status interface

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard half-length PCI board

Features
Simultaneous synthesis of up to five different clocks
Eight SMC clock outputs
Ideal for A/D and D/A converter clock sources
Typical phase noise: –105 dBc/Hz @ 1 kHz offset
All clocks are phase-locked to input reference signal
Input reference frequency of 5 to 100 MHz
Four programmable VCXOs with 32-bit tuning resolution
Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
Output clock frequencies between 50 and 700 MHz
Control and status via PCI bus interface
General Information

Model 7891 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from onboard programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7891 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7891 can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a flex panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7891’s can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7891 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input
- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: -6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- Quantity: Four
- Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16
- Programmable VCXOs (Quantity: Four)
- Frequency Range: 50 to 700 MHz
- Tuning Resolution: 32 bits
- Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: -105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface

PCIe Interface: Gen. 2, x8 width
PCIe Ports: One x4 port to PCI bus, one x8 port to PCIe motherboard
Operation: Control and status interface

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half-length PCIe, 4.38 in. x 6.6 in.
General Information

Model 5391 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5391 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 5391 can be programmed to route any of these 20 frequencies to the board’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

Specifications

Front Panel Reference Input
- Connector Type: SMC
- Input Impedance: 50 ohms
- Reference Frequency: 5 to 100 MHz
- Input Level: –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- Quantity: Four
- Type: Texas Instruments CDC7005
- Frequency Dividers: 1, 2, 4, 8 and 16
- Programmable VCXOs (Quantity: Four)
- Frequency Range: 50 to 700 MHz
- Tuning Resolution: 32 bits
- Unlocked Accuracy: ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- Connector Type: SMC
- Output Impedance: 50 ohms
- Output Level: +3 dBm @ 700 MHz
- Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model 5391
- Programmable Multifrequency Clock Synthesizer - 3U VPX

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
General Information

Models 5791 and 5891 generate up to eight or 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

These models use four or eight Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005’s can output up to five frequencies each. These models can be programmed to route any of these frequencies to the board’s five or 10 output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or 10 different clocks to various outputs.

With four or eight independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than 10 different clock outputs are required simultaneously, multiple 5891’s can be used and phase-locked with a 5 to 100 MHz system reference.

Specifications

Front Panel Reference Input
Connector Type: SMC
Input Impedance: 50 ohms
Reference Frequency: 5 to 100 MHz
Input Level: -6 dBm to +10 dBm
PLL Clock Synthesizers & Jitter Cleaners
Quantity: Model 5791: Four
Model 5891: eight
Type: Texas Instruments CDC7005
Frequency Dividers: 1, 2, 4, 8 and 16
Programmable VCXOs (Four or eight)
Frequency Range: 50 to 700 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
Front Panel Clock Outputs (Eight or 16)
Connector Type: SMC
Output Impedance: 50 ohms
Output Level: +3 dBm @ 700 MHz
Typ. Phase Noise: –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2: x4, control and status

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 6U Board 9.187 in x 6.717 in
(233.35 mm x 170.61 mm)

Features
- Simultaneous synthesis of up to five or 10 different clocks
- Eight or 16mSMC clock outputs
- Typical phase noise: -105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

Ordering Information

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<th>Model</th>
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<td>5791</td>
<td>Programmable Multifrequency Clock Synthesizer - 3U VPX</td>
</tr>
<tr>
<td>5891</td>
<td>Programmable Multifrequency Clock Synthesizer - 3U VPX</td>
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</table>

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
Features

- Synchronizes up to four separate high-speed Cobalt, Onyx, or Jade I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt, Onyx, and Jade modules

General Information

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt, Onyx, and Jade modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt, Onyx, and Jade board to generate the clock for all subsequent boards in the system.

Output Signals

The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt, Onyx, and Jade modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals

The 7192 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 7192 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected modules. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 7192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.
Calibration

The 7192 features a calibration output specifically designed to work with the 71640/41, 71741 and 71841 3.6 GHz A/D XMC modules to provide a signal reference for phase adjustment across multiple A/Ds.

Programming

The 7192 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 7192 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt, Onyx, and Jade modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 7192 supports all high-speed models in the Cobalt, Onyx and Jade families including the 71x30 1 GHz A/D and D/A XMC modules; the 71x40/41 3.6 GHz A/D XMC modules; and the 71x70/71 Four-channel 1.25 GHz, 16-bit D/A XMC modules.

Specifications

Front Panel Sample Clock/Reference Input
Connector Type: MMCX
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
Connector Type: MMCX
Input Level: LVTTL

Front Panel µSync Inputs/Outputs
Quantity: 4
Connector Type: 19-pin µHDMI
Signal Level: CML
Signals (µSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (µSync connectors 2–4): Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
Connector Type: MMCX
Output Impedance: 50 ohms
Output Level: +6 dBm nominal, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz

Programmable VCXO:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16
PMC/XMC Interface: Power only on PMC P1 or XMC P15

Environmental
Operating Temp: 0° to 50° C
Storage Temp: −20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard PMC module, 2.91 in. x 5.87 in.
High-Speed Synchronizer and Distribution Board - 3U/6U cPCI

**General Information**

These High-Speed Synchronizer and Distribution cPCI Boards synchronize multiple Pentek Cobalt, Onyx, Jade or Flexor boards within a system. They enable synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to eight boards can be synchronized using the 7492, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

**Input Signals**

These models provide three or six front panel MMCX connectors to accept input signals from external sources: one or two for clock, one or two for gate or trigger and one or two for synchronization signals. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the front panel µSync output connectors, allowing a single Cobalt, Onyx, and Jade board to generate the clock for all subsequent boards in the system.

**Output Signals**

These models provide up to eight front panel µSync output connectors, compatible with Pentek’s high-speed Cobalt, Onyx and Jade boards in addition to most of the Flexor products. The µSync signals include reference clocks, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

**Clock Signals**

These models can accept one or two user supplied external clocks on front panel MMCX connectors. As an alternative to the external clock, they can use on-board programmable voltage controlled crystal oscillators (VCXOs) as the clock sources. The VCXOs can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock inputs.

The external or on-board clocks can operate at full rate or be divided and used to register all sync and gate/trigger signals as well as providing reference clocks to all connected boards. In addition, the clocks are available at the Clock Out MMCX as sample or reference clocks for other boards in the system.

**Gate and Synchronization Signals**

These models feature separate inputs for gate/trigger and sync signals. Programmable delays allow the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.

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**Features**

- Synchronizes four or eight separate Cobalt, Onyx, Jade or Flexor I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt, Onyx, Jade or Flexor boards
High-Speed Synchronizer and Distribution Board - 3U/6U cPCI

Models 7292, 7492 and 7392

Calibration
These models feature a calibration output specifically designed to work with the 72x40/41, 73x40/41 and 74x40/41 3.6 GHz A/D cPCI boards to provide a signal reference for phase adjustment across multiple A/Ds.

Programming
These models allow programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

These models are programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all Cobalt, Onyx, Jade or Flexor boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products
These sync products are compatible with the high-speed Cobalt, Onyx and Jade boards and all Flexor products. See the complete list of supported products on the Model 7292, Model 7392 and Model 7492 web pages.

Ordering Information

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<td>7492</td>
<td>Eight µSync High-Speed Synchronizer band Distribution Board - 6U cPCI</td>
</tr>
<tr>
<td>7392</td>
<td>Four µSync High-Speed Synchronizer and Distribution Board - 3U cPCI</td>
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</table>

Accessories
4 ea. 18”µSync cables are supplied with Models 7292 and 7392;
8 ea. 18”µSync cables are supplied with Model 7492;
additional cables may be ordered:
2192-018 µSync cable - 18”
2192-036 µSync cable - 36”

Specifications

Front Panel Sample Clock/Reference Input Connector Type: MMCX
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs Connector Type: MMCX
Input Level: LVTTL

Front Panel µSync Inputs/Outputs
Quantity: 4 or 8
Connector Type: 19-pin µHDMI
Signal Level: CML
Signals (µSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (µSync connectors 2–4): Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output Connector Type: MMCX
Output Impedance: 50 ohms
Output Level: +6 dBm nominal, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz

Programmable VCXOs:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm

PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16

cPCI Interface
Power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 3U or 6U cPCI board

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201.818.5900 ● Fax: 201.818.5904 ● Email: info@pentek.com
www.pentek.com
Features
- Synchronizes up to four separate Cobalt, Onyx, Flexor or Jade I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt, Onyx, Flexor or Jade boards

General Information
The Model 7892 High-Speed Synchronizer and Distribution PCIe Board synchronizes multiple Pentek Cobalt, Onyx, Flexor or Jade boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four boards can be synchronized using the 7892, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals
Model 7892 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high-performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt, Onyx, Flexor or Jade board to generate the clock for all subsequent boards in the system.

Output Signals
The 7892 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt, Onyx, Flexor and Jade boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals
The 7892 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 7892 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals
The 7892 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.
Calibration
The 7892 features a calibration output specifically designed to work with the 78640 or 78740 3.6 GHz A/D board and provide a signal reference for phase adjustment across multiple D/As.

Programming
The 7892 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 7892 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt, Onyx, Flexor and Jade boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products
The 7892 is compatible with the high-speed Cobalt, Onyx and Jade boards, and all Flexor products.

See the complete list of supported products on the Model 7892 web pages.

Specifications
Front Panel Sample Clock/Reference Input
Connector Type: MMCX
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
Connector Type: MMCX
Input Level: LVTTL

Front Panel µSync Inputs/Outputs
Quantity: 4
Connector Type: 19-pin µHDMI
Signal Level: CML
Signals (µSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (µSync connectors 2–4): Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
Connector Type: MMCX
Output Impedance: 50 ohms
Output Level: +6 dBm nominal, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz

Programmable VCXO:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16

PCI Express Interface
PCIe Bus: x4 or x8, power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: −20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: PCIe card 4.380 in x 7.130 in
(111.25 mm x 181.10 mm)

Ordering Information

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<td>High-Speed Synchronizer and Distribution Board - PCIe</td>
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Accessories
4 ea. 18” µSync cables are supplied; additional cables may be ordered:
2192-018 µSync cable - 18”
2192-036 µSync cable - 36”

www.pentek.com
Model 5392 COTS (left) and rugged version

High-Speed Synchronizer and Distribution Board - 3U VPX

General Information
The Model 5392 High-Speed Synchronizer and Distribution 3U VPX Board synchronizes multiple Pentek Cobalt, Onyx, and Jade boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four boards can be synchronized using the 5392, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Output Signals
The 5392 provides four front panel μSync output connectors, compatible with a range of high-speed Pentek Cobalt, Onyx, and Jade boards. The μSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals
The 5392 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 5392 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals
The 5392 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the μSync output connectors.

Features
- Synchronizes up to four separate high-speed Cobalt, Onyx, and Jade I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel μSync connectors compatible with a range of Pentek Cobalt, Onyx, and Jade boards

New! New! New! New! New!

Model 5392 COTS (left) and rugged version

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
Calibration

The 5392 features a calibration output specifically designed to work with the 52x40/41 and 53x40/41 3.6 GHz A/D 3U VPX boards to provide a signal reference for phase adjustment across multiple A/Ds.

Programming

The 5392 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the μSync connectors.

The 5392 is programmed via a TWSI control interface on the first μSync connector. The control interface is compatible with the front panel μSync connectors of all high-speed Cobalt, Onyx and Jade boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 5392 supports all high-speed models in the Cobalt, Onyx and Jade families including the 52x30 and 53x30 1 GHz A/D and D/A 3U VPX boards; the 52x40/41 and 53x40/41 3.6 GHz A/D 3U VPX boards; and the 52x70/71 and 53x70/71 Four-channel 1.25 GHz, 16-bit D/A 3U VPX boards.

Specifications

Front Panel Sample Clock/Reference Input
Connector Type: MMCX
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
Connector Type: MMCX
Input Level: LVTTL

Front Panel μSync Inputs/Outputs
Quantity: 4
Connector Type: 19-pin μHDMI
Signal Level: CML
Signals (μSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (μSync connectors 2–4): Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
Connector Type: MMCX
Output Impedance: 50 ohms
Output Level: +6 dBm nominal, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz

Programmable VCXO:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm

PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16

VPX Interface
Power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3U VPX board 3.937 in x 6.717 in (100.00 mm x 170.61 mm)

Ordering Information

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Accessories
4 ea. 18”μSync cables are supplied; additional cables may be ordered:
2892-018  μSync cable - 18”
2892-036  μSync cable - 36”
General Information

The Models 5792 and 5892 High-Speed Synchronizer and Distribution 6U VPX boards synchronize multiple Pentek Cobalt or Onyx boards within a system. They enable synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four or eight boards can be synchronized using these models, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

These models provide three or six front panel MMCX connectors to accept input signals from external sources: one or two for clock, one or two for gate or trigger and one or two for synchronization signals. Clock signals can be applied from an external source such as a high-performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the front panel µSync output connectors, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

These models provide up to eight front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards.

Clock Signals

These models can accept one or two user-supplied external clocks on front panel MMCX connectors. As an alternative to the external clock, they can use on-board programmable voltage controlled crystal oscillators (VCXOs) as the clock sources. The VCXOs can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock inputs.

The external or on-board clocks can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing reference clocks to all connected boards. In addition, the clocks are available at the Clock Out MMCX as sample or reference clocks for other boards in the system.

Gate and Synchronization Signals

These models feature separate inputs for gate/trigger and sync signals. Programmable delays allow the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.
High-Speed Synchronizer and Distribution Board - 6U VPX

Calibration
These models feature a calibration output specifically designed to work with the 57640, 58640 or 57740, 58740 3.6 GHz A/D boards and provide a signal reference for phase adjustment across multiple D/As.

Programming
These models allow programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

Both models are programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products
These models support all high-speed models in the Cobalt and Onyx families including the 57630 and 58630 1 GHz A/D and D/A 6U VPX boards; the 57730 and 58730 1 GHz A/D and D/A 6U VPX boards; the 57640 and 58640 3.6 GHz A/D 6U VPX boards; the 57740 and 58740 3.6 GHz A/D 6U VPX boards; the 57670 and 58670 Four-channel 1.25 GHz, 16-bit D/A 6U VPX boards; the 57770 and 58770 Four-channel 1.25 GHz, 16-bit D/A 6U VPX boards; and the 57630 and 58630 1 GHz A/D, D/A 6U VPX boards.

Specifications
Front Panel Sample Clock/Reference Input
Connector Type: MMCX
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz
Front Panel Gate/Trigger & Sync Inputs
Connector Type: MMCX
Input Level: LVTTL
Front Panel µSync Inputs/Outputs
Quantity: Model 5792: Four;
Model 5892: Eight
Connector Type: 19-pin µHDMI
Signal Level: CML
Signals (µSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (µSync connectors 2–4): Reference Clock Out, Gate/Trigger Out, Sync Out
Front Panel Clock / Calibration Output
Connector Type: MMCX
Output Impedance: 50 ohms
Output Level: +6 dBm nominal, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz
Programmable VCXOs:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16
PCI Express Interface
PCI Bus: ×4 or ×8, power only
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)

Ordering Information
Model Description
5792 High-Speed Synchronizer and Distribution Board - 6U VPX, Single Density
5892 High-Speed Synchronizer and Distribution Board - 6U VPX, Double Density

Accessories
4 ea. 18"µSync cables are supplied with Models 7292 and 7392;
8 ea. 18"µSync cables are supplied with Model 7492;
additional cables may be ordered:
2192-018 µSync cable - 18";
2192-036 µSync cable - 36"
General Information
The Model 5692 High-Speed Synchronizer and Distribution board synchronizes multiple Pentek Cobalt, Onyx, and Jade modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four modules can be synchronized using the 5692, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals
Model 5692 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt, Onyx, and Jade board to generate the clock for all subsequent boards in the system.

Output Signals
The 5692 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt, Onyx, and Jade modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals
The 5692 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 5692 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected modules. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals
The 5692 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.
High-Speed Synchronizer and Distribution Board - AMC

Calibration
The 5692 features a calibration output specifically designed to work with the 56640/41, 56741 and 56841 3.6 GHz A/D AMC boards to provide a signal reference for phase adjustment across multiple A/Ds.

Programming
The 5692 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 5692 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt, Onyx, and Jade modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products
The 5692 supports all high-speed models in the Cobalt, Onyx and Jade families including the 56x30 1 GHz A/D and D/A AMC modules; the 56x40/41 3.6 GHz A/D AMC modules; and the 56x70/71 Four-channel 1.25 GHz, 16-bit D/A AMC modules.

Specifications
- Front Panel Sample Clock/Reference Input
  - Connector Type: MMCX
  - Input Impedance: 50 ohms
  - Input Level: 0 dBm to +10 dBm, sine wave
  - Sample Clock Frequency: 100 MHz to 2 GHz
  - Reference Frequency: 5 to 100 MHz

- Front Panel Gate/Trigger & Sync Inputs
  - Connector Type: MMCX
  - Input Level: LVTTTL

- Front Panel µSync Inputs/Outputs
  - Quantity: 4
  - Connector Type: 19-pin µHDMI
  - Signal Level: CML

- Front Panel Clock / Calibration Output
  - Connector Type: MMCX
  - Output Impedance: 50 ohms
  - Output Level: +6 dBm nominal, sine wave
  - Sample Clock Frequency: 100 MHz to 1.8 GHz

- Programmable VCXO:
  - Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
  - Tuning Resolution: 32 bits
  - Unlocked Accuracy: ±20 ppm

- PLL, Divider & Jitter Cleaner
  - Type: Texas Instruments CDCM7005
  - Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16

- AMC Interface
  - Power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: −20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

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<td>5692</td>
<td>High-Speed Synchronizer and Distribution Board - AMC</td>
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</table>

Accessories
- 4 ea. 18"µSync cables are supplied; additional cables may be ordered:
  - 2192-018  µSync cable - 18"
  - 2192-036  µSync cable - 36"
General Information

Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions.

For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

Input Signals

The Model 7893 provides four front panel SMA connectors to accept LV-TTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 also accepts the 26-pin Timing Bus connector used on Cobalt and Onyx boards. This input allows a single Cobalt or Onyx board to generate the timing and clock signals for the 7893 for distribution of up to eight additional boards. This input can also be used to link multiple 7893’s for larger systems.

Output Signals

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system’s sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

Clock Signals

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. In addition, the board is equipped with a programmable on-board VCXO clock generator which can free run or be locked to a user supplied, 10 MHz typical, system reference. In all cases, the sample clock can be divided by 1, 2, 4, 8 or 16 prior to distribution to the Clock Out SMAs or the timing bus output connectors.

USB Interface

The 7893 is programmed via a USB interface. In addition to status and control, the USB interface can be used to generate Gate/Trigger and Sync/PPS signals for distribution to all connected boards.

Physical Characteristics

The 7893 is a single-slot PCIe size board which can be mounted in any PCI or PCIe slot. The board receives power from a standard six-pin PCIe power connector and uses the PCI or PCIe slot solely for physical mounting, with no electrical connections.

Features

- Synchronizes up to eight separate Cobalt or Onyx boards
- Up to eight 7893s can be linked together to synchronize up to 64 boards
- Synchronizes sampling, data acquisition and playback for multichannel systems
- Synchronizes gating and triggering functions
- On-board programmable sample clock generator
- Output clock rates up to 800 MHz
- Front panel SMA connectors for TTL input signals and clock outputs
- Single-slot PCIe format
Supported Products

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D, 200 MHz transceivers, the 78650 and 78651 two-channel A/D, 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.

Specifications

Sample Clock/Reference Clock Input
Type: Front panel female SMC connector
Signal: Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or 4 to 180 MHz PLL system reference, typically 10 MHz

TTL Gate/Trigger Input
Type: Front panel female SMC connector
Signal: LVTTL
Function: Programmable functions include gate and trigger

TTL Sync/PPS Input A
Type: Front panel female SMC connector
Signal: LVTTL
Function: Programmable functions include sync and PPS

TTL Sync/PPS Input B
Type: Front panel female SMC connector
Signal: LVTTL
Function: Programmable functions include sync and PPS

Timing Bus In
Type: One rear 26-pin connector
Signals: LVPECL bus includes: Sample Clock A & B In, Gate/Trigger A & B In, and Sync/PPS A & B In

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 800 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference (front panel Reference Clock Input), typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for each of five on-board clock buses.

Sample Clock Output
Type: Four front panel female SMC connectors, each can be independently divided
Output Level: +9 dBm, nominal, sine wave

Timing Bus Out
Type: Eight rear 26-pin connectors
Signals: LVPECL bus includes: Sample Clock A & B Out, Gate/Trigger A & B Out, and Sync/PPS A & B Out

Control: Rear USB input for connecting to motherboard on-board USB 8-pin header

Power: Rear 8-pin connector compatible with PCIe power connectors

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information
Model  Description
7893  System Synchronizer and Distribution Board- PCIe

Accessories
2891  Timing Bus Cables
# Model 7194

## High-Speed Clock Generator - PMC/XMC

### General Information

Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt and Onyx modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

### Sample Clock Synthesizer

The Model 7194 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

### On-board Reference Clock

In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

### Physical Characteristics

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power. The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

### Specifications

- **Sample Clock Frequency**: Fixed, 1.4 to 2.0 GHz by ordering option
- **Sample Clock Outputs**
  - **Type**: Four front panel female SMA connectors
  - **Output Level**: +10 dBm, nominal, sine wave
- **Reference Clock In**
  - **Type**: Front panel female SMA connector
  - **Frequency**: 10 MHz
  - **Input Impedance**: 50 ohms
  - **Input Level**: 0 dBm to +10 dBm, sine wave
- **Reference Clock Out**
  - **Type**: Front panel female SMA connector
  - **Center Frequency**: 10 MHz
  - **Output Impedance**: 50 ohms
  - **Output Level**: +10 dBm, nominal, sine wave
- **Frequency Stability vs. Change in Temperature**: 50.0 ppb
- **Frequency Calibration**: ±1.0 ppm
- **Aging**
  - **Daily**: ±10 ppb/day
  - **First Year**: ±300 ppb
- **Total Frequency Tolerance (20 years)**: ±4.60 ppm
- **Phase Noise**
  - 1 Hz Offset: -67 dBc/Hz
  - 10 Hz Offset: -100 dBc/Hz
  - 100 Hz Offset: -130 dBc/Hz
  - 1 KHz Offset: -148 dBc/Hz
  - 10 KHz Offset: -154 dBc/Hz
  - 100 KHz Offset: -155 dBc/Hz
- **PMC/XMC Interface**: Power only on PMC P1 or XMC P15

### Environmental

- **Operating Temp**: 0° to 50° C
- **Storage Temp**: –20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: Standard PMC module, 2.91 in. x 5.87 in.
**Ordering Information**

**Model** | **Description**
--- | ---
7194 | High-speed Clock Generator - PMC/XMC

**Options** | **Description**
--- | ---
104 | PMC P14 (Power only)
105 | XMC P15 (Power only)
106 | PCIe 6-pin connector (Power only)
150 | 1.500 GHz sample clock
180 | 1.800 GHz sample clock

*Contact Pentek for additional sample clock options*
High-Speed Clock Generator - 3U/6U cPCI

Models 7294, 7494 and 7394

New! New! New! New! New!

Models 7294 and 7394 Block Diagram. Model 7494 Doubles all Resources.

General Information
These High-Speed Clock Generators provide fixed-frequency sample clocks to cPCI Cobalt and Onyx boards in multiboard systems. They enable synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Model 7394 is a 3U cPCI board that generates four clocks. Model 7294 is a 6U cPCI board that generates four clocks, while Model 7494 is a double-density 6U cPCI board that generates eight clocks.

Sample Clock Synthesizer
These models use one or two high-precision, fixed-frequency, PLOs (Phase-Locked Oscillators) to generate four or eight output sample clocks. The PLOs accept a 10 MHz reference clock through front panel SMA connectors. The PLOs lock the output sample clocks to the incoming reference. Power splitters then receive the sample clocks and distribute them to four or eight front panel SMA connectors.

These models are available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock
In addition to accepting a reference clock on the front panel, these models include one or two on-board 10 MHz reference clocks. The reference clocks are OCXOs (Oven-Controlled Crystal Oscillators), which provide an exceptionally precise frequency standard with excellent phase noise characteristics.

Physical Characteristics
These models are standard CompactPCI boards. They do not require programming and the interface connectors are used solely for power. The boards can be optionally configured with a PCIe-style 6-pin power connector allowing them to be used in virtually any chassis or enclosure.

Specifications
Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option
Sample Clock Outputs
Type: Four or eight front panel female SMA connectors
Output Level: +10 dBm, nominal, sine wave

Reference Clock In
Type: Front panel female SMA connector
Frequency: 10 MHz
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave

Reference Clock Out
Type: Front or eight front panel female SMA connectors
Center Frequency: 10 MHz
Output Impedance: 50 ohms
Output Level: +10 dBm, nominal, sine wave
Frequency Stability vs. Change in Temperature: 50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
Daily: ±10 ppb/day
First Year: ±300 ppb
Total Frequency Tolerance (20 years): ±4.60 ppm
Phase Noise
1 Hz Offset: -67 dBc/Hz
10 Hz Offset: -100 dBc/Hz
100 Hz Offset: -130 dBc/Hz
1 KHz Offset: -148 dBc/Hz
10 KHz Offset: -154 dBc/Hz
100 KHz Offset: -155 dBc/Hz

PCI Interface
PCI Bus: 32-bit, 66 MHz (supports 33 MHz), power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 3U or 6U cPCI board
Sample Clock Phase Noise

Phase Noise (1 Hz BW, typical)

![Graph showing phase noise](image)

Phase Noise 10.00 dB/Ref -20.00 dBC/Hz

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<td>High-Speed Clock Generator - 3U cPCI</td>
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<td>1.500 GHz sample clock</td>
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<td>180</td>
<td>1.800 GHz sample clock</td>
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Contact Pentek for additional sample clock options
Model 7894 High-Speed Clock Generator - PCIe

General Information

Model 7894 High-Speed Clock Generator provides fixed-frequency sample clocks to PCIe Cobalt and Onyx boards in multi-board systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Sample Clock Synthesizer

The Model 7894 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7894 is available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock

In addition to accepting a reference clock on the front panel, the 7894 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Physical Characteristics

The 7894 is a standard PCI Express board. The board does not require programming and the PCIe interface connector is used solely for power.

Specifications

Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option

Sample Clock Outputs

Type: Four front panel female SMA connectors
Output Level: +10 dBm, nominal, sine wave

Reference Clock In

Type: Front panel female SMA connector
Frequency: 10 MHz
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave

Reference Clock Out

Type: Front panel female SMA connector
Center Frequency: 10 MHz
Output Impedance: 50 ohms
Output Level: +10 dBm, nominal, sine wave

Frequency Stability vs. Change in Temperature: 50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
Daily: ±10 ppb/day
First Year: ±300 ppb
Total Frequency Tolerance (20 years): ±4.60 ppm

Phase Noise

1 Hz Offset: -67 dBc/Hz
10 Hz Offset: -100 dBc/Hz
100 Hz Offset: -130 dBc/Hz
1 KHz Offset: -148 dBc/Hz
10 KHz Offset: -154 dBc/Hz
100 KHz Offset: -155 dBc/Hz

PCI Express Interface

PCIe Bus: x4 or x8, power only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half length PCIe card, 4.38 in. x 7.13 in.

Features

- Provides sample clock for up to four separate PCIe Cobalt or Onyx boards
- Locks to user-supplied 10 MHz reference clock or on-board reference.
- OCXO provides an exceptionally precise clock

New! New! New! New! New!
Model 7894
High-Speed Clock Generator - PCIe

Sample Clock Phase Noise

Phase Noise (1 Hz BW, typical)

Phase Noise 10.00 dB/Ref -20.00 dBC/Hz

Contact Pentek for additional sample clock options

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<tr>
<th>Options</th>
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<tbody>
<tr>
<td>150</td>
<td>1.500 GHz sample clock</td>
</tr>
<tr>
<td>180</td>
<td>1.800 GHz sample clock</td>
</tr>
</tbody>
</table>
Model 5294 COTS (left) and rugged version

Features
- Provides sample clock for up to four separate 3U VPX Cobalt or Onyx boards
- Locks to user-supplied 10 MHz reference clock or on-board reference.
- OCXO provides an exceptionally precise clock

General Information
Model 5294 High-Speed Clock Generator provides fixed-frequency sample clocks to 3U VPX Cobalt and Onyx boards in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Sample Clock Synthesizer
The Model 5294 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front-panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 5294 is available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock
In addition to accepting a reference clock on the front panel, the 5294 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Physical Characteristics
The 5294 is a standard 3U VPX board. The board does not require programming and the PCIe interface connector is used solely for power. The board can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Specifications
Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option
Sample Clock Outputs
- Type: Four front panel female SMA connectors
- Output Level: +10 dBm, nominal, sine wave

Reference Clock In
- Type: Front panel female SMA connector
- Frequency: 10 MHz
- Input Impedance: 50 ohms
- Input Level: 0 dBm to +10 dBm, sine wave

Reference Clock Out
- Type: Front panel female SMA connector
- Center Frequency: 10 MHz
- Output Impedance: 50 ohms
- Output Level: +10 dBm, nominal, sine wave
- Frequency Stability vs. Change in Temperature: 50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance (20 years): ±4.60 ppm
- Phase Noise
  - 1 Hz Offset: -67 dBc/Hz
  - 10 Hz Offset: -100 dBc/Hz
  - 100 Hz Offset: -130 dBc/Hz
  - 1 kHz Offset: -148 dBc/Hz
  - 10 kHz Offset: -154 dBc/Hz
  - 100 kHz Offset: -155 dBc/Hz
- PCI Express Interface
  - PCIe Bus: x4, power only
- Environmental
  - Operating Temp: 0° to 50° C
  - Storage Temp: -20° to 90° C
  - Relative Humidity: 0 to 95%, non-cond.
  - Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
Model 5294  
High-Speed Clock Generator - 3U VPX

Sample Clock Phase Noise

Phase Noise (1 Hz BW, typical)

Phase Noise 10.00 dB/Ref -20.00 dBc/Hz

Ordering Information

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</table>

Contact Pentek for additional sample clock options
general information

These High-Speed Clock Generators provide fixed-frequency sample clocks to 6U VPX Cobalt and Onyx boards in multiboard systems. They enable synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Model 5794 is a 6U VPX board that generates four clocks. Model 5894 is a double-density 6U VPX board that generates eight clocks.

Sample Clock Synthesizer

These models use one or two high-precision, fixed-frequency, PLOs (Phase-Locked Oscillators) to generate four or eight output sample clocks. The PLOs accept a 10 MHz reference clock through front panel SMA connectors. The PLOs lock the output sample clocks to the incoming reference. Power splitters then receive the sample clocks and distribute them to four or eight front panel SMA connectors.

These models are available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock

In addition to accepting a reference clock on the front panel, these models include one or two on-board 10 MHz reference clocks. The reference clocks are OCXOs (Oven-Controlled Crystal Oscillators), which provide an exceptionally precise frequency standard with excellent phase noise characteristics.

Physical Characteristics

These models are standard 6U OpenVPX boards. They do not require programming and the interface connectors are used solely for power. The boards can be optionally configured with a PCIe-style 6-pin power connector allowing them to be used in virtually any chassis or enclosure.

Features

- Provides sample clock for up to four or eight separate 6U VPX Cobalt or Onyx boards
- Locks to user-supplied 10 MHz reference clock or on-board reference
- OCXO provides an exceptionally precise clock

Specifications

Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option

Sample Clock Outputs

Type: Four or eight front panel female SMA connectors
Output Level: +10 dBm, nominal, sine wave

Reference Clock In

Type: Front panel female SMA connector
Frequency: 10 MHz
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave

Reference Clock Out

Type: Four or eight front panel female SMA connectors
Center Frequency: 10 MHz
Output Impedance: 50 ohms
Output Level: +10 dBm, nominal, sine wave

Frequency Stability vs. Change in Temperature: 50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
Daily: ±10 ppb/day
First Year: ±300 ppb
Total Frequency Tolerance (20 years): ±4.60 ppm

Phase Noise

1 Hz Offset: -67 dBc/Hz
10 Hz Offset: -100 dBc/Hz
100 Hz Offset: -130 dBc/Hz
1 KHz Offset: -148 dBc/Hz
10 KHz Offset: -154 dBc/Hz
100 KHz Offset: -155 dBc/Hz

PCI Express Interface

PCI Bus: x4 or x8, power only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)

Model 5794 Block Diagram
Model 5894 Doubles all Resources.
Sample Clock Phase Noise

Phase Noise (1 Hz BW, typical)

Contact Pentek for additional sample clock options
High-Speed Clock Generator - AMC

General Information
Model 5694 High-Speed Clock Generator provides fixed-frequency sample clocks to AMC Cobalt and Onyx boards in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

Sample Clock Synthesizer
The Model 5694 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front-panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 5694 is available with sample clock frequencies from 1.4 to 2.0 GHz.

On-board Reference Clock
In addition to accepting a reference clock on the front panel, the 5694 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Physical Characteristics
The 5694 is a standard AMC board. The board does not require programming and the PCIe interface connector is used solely for power. The board can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Specifications
Sample Clock Frequency: Fixed, 1.4 to 2.0 GHz by ordering option

Sample Clock Outputs
Type: Four front panel female SMA connectors
Output Level: +10 dBm, nominal, sine wave

Reference Clock In
Type: Front panel female SMA connector
Frequency: 10 MHz
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave

Reference Clock Out
Type: Front panel female SMA connector
Center Frequency: 10 MHz
Output Impedance: 50 ohms
Output Level: +10 dBm, nominal, sine wave

Frequency Stability vs. Change in Temperature: 50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
Daily: ±10 ppb/day
First Year: ±300 ppb
Total Frequency Tolerance (20 years): ±4.60 ppm
Phase Noise
1 Hz Offset: -67 dBc/Hz
10 Hz Offset: -100 dBc/Hz
100 Hz Offset: -130 dBc/Hz
1 KHz Offset: -148 dBc/Hz
10 KHz Offset: -154 dBc/Hz
100 KHz Offset: -155 dBc/Hz

PCI-Express Interface
PCI Express Bus: Gen. 1 x4 or x8, power only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
**Model 5694**

High-Speed Clock Generator - AMC

**Sample Clock Phase Noise**

**Phase Noise (1 Hz BW, typical)**

![Graph showing phase noise](image)

Phase Noise 10.00 dB/Ref -20.00 dBc/Hz

**Ordering Information**

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Contact Pentek for additional sample clock options
Model 9190

Clock and Sync Generator for I/O Modules

Features
- Synchronizes up to 80 I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Synchronizes local oscillator phase, decimation phase and frequency switching for multichannel digital receivers and upconverters
- Clock rates up to 105 MHz
- Supports most popular I/O modules
- Front panel SMA connectors for external clock and timing signal inputs and outputs
- 19-inch wide, 1.75 in. high rack-mount chassis with integral AC line power supply
- Flexible cable installation supports many different system configurations

General Information

Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Input Signals

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the 9190.

Output Signals

The front panel clock and sync connectors in the list of supported modules fall into two classes, thus requiring two types of front panel cable. The first type uses a 26-pin connector (for the 621x series, the 6229, the 7x31, 7x40 and 7x42 series) delivering the clock and four timing signals. The second type uses a 36-pin connector (for the 623x series) delivering the clock and five timing signals.

Either cable type can be installed in any of the 80 positions of the Model 9190. However, systems with mixed types of I/O modules may not have all functions supported. Contact the factory for assistance with your specific configuration.

Buffered versions of the clock and five timing signals are also available as outputs on the 9190’s front panel SMA connectors.

Supported Products

Model 9190 currently supports VIM Models 6210, 6211, 6216, 6228, 6229, 6230, 6231, 6232, 6235, 6236; the PMC Models 7131, 7140, 7141, 7142 and 7150; the PCI Models 7631A, 7640, 7641, 7642 and 7650; and the cPCI Models 7231, 7331, 7240, 7340, 7241, 7341, 7242, 7342 and 7350. Contact us for an up-to-date list of supported modules.

Ordering Information

Model Description
9190 Clock and Sync Generator
Options:
-019 64 MHz internal oscillator
-040 40-Channel version
Model 9192

Rackmount High-Speed System Synchronizer Unit

General Information

Model 9192 Rackmount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt, Onyx, Flexor and Jade modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high-performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt, Onyx, Flexor or Jade board to generate the clock for all subsequent boards in the system.

Output Signals

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt, Onyx, Flexor and Jade boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals

The 9192 can accept a user supplied external clock on its rear panel SMA connector. As an alternative to the external clock, the 9192 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the rear panel reference clock input.

The on-board or external clock can operate at full rate or can be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at twelve Clock Out SMAs as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 9192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors.
Rackmount High-Speed System Synchronizer Unit

Calibration
The 9192 features a calibration output specifically designed to work with the xx640, xx641, xx741 and xx841 3.6 GHz A/D XMC modules to provide a signal reference for phase adjustment across multiple A/Ds.

Programming
The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 is programmed via a rear panel USB connector or a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt, Onyx, Jade and Flexor modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products
The 9192 is compatible with the high-speed Cobalt, Onyx and Jade boards, and all Flexor products.

See the complete list of supported products on the Model 9192 web pages.

Specifications
Rear Panel Sample Clock / Reference Input
Connector Type: SMA
Input Impedance: 50 ohms
Input Level: 0 dBm to +10 dBm, sine wave
Sample Clock Frequency: 100 MHz to 2 GHz
Reference Frequency: 5 to 100 MHz
Rear Panel Gate/Trigger & Sync Inputs
Connector Type: SMA
Input Level: LVTTL
Rear Panel µSync Inputs/Outputs
Quantity: 12
Connector Type: 19-pin µHDMI
Signal Level: CML
Signals (µSync connector 1): Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
Signals (µSync connectors 2-12): Reference Clock Out, Gate/Trigger Out, Sync Out
Rear Panel Clock / Calibration Outputs
Quantity: 12
Connector Type: SMA
Output Impedance: 50 ohms
Output Level: +6 dBm nominal at 1400 MHz, sine wave
Sample Clock Frequency: 100 MHz to 1.8 GHz
Programmable VCXO:
Frequency Ranges: 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
Tuning Resolution: 32 bits
Unlocked Accuracy: ±20 ppm
PLL, Divider & Jitter Cleaner
Type: Texas Instruments CDCM7005
Frequency Dividers: 1, 2, 3, 4, 6, 8 and 16
Power: 120VAC
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 1U Rackmount, 19 in. x 1.75 in.

Ordering Information
Model | Description
9192  | Rackmount High-Speed System Synchronizer Unit

Accessories
12 ea. 18" µSync cables are supplied; additional cables may be ordered:
2892-018 µSync cable - 18"
2892-036 µSync cable - 36"

Specifications are subject to change without notice.
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We’re glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at: Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900  •  fax: 201-818-5697  •  email: custsvc@pentek.com

www.pentek.com
## SOFTWARE & FPGA TOOLS

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**Customer Information**

Last updated: April 2018
Navigator Design Suite

General Information

Pentek’s Navigator Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, and software to control the FPGA hardware from a host computer.

Even when “turnkey” solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek’s Jade™ architecture and provide a better solution to the complex task of IP and software creation.

Navigator FDK (FPGA Design Kit)

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry’s first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek’s Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade data acquisition and processing board. When the design is opened in Vivado’s IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design. Each Navigator/Jade design includes User Blocks in the data-flow path, ideal for inserting custom processing IP.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP. In addition to the IP specific to the supported Jade board, Navigator also includes processing blocks for some of the most commonly used algorithms.

As a Certified Member of Xilinx’s Alliance program, Pentek has passed a comprehensive 320-point review of its technical, business, quality, and support processes and has committed engineers who completed the same rigorous training used by Xilinx Field Application Engineers worldwide.

Pentek continues to demonstrate years of expertise with Xilinx devices and implementation techniques that consistently deliver high-quality products and services utilizing the Xilinx programmable platforms.

The Model 78861 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today.

Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

This XMC board is also available in other formats such as 3U and 6U VPX, PCIe, 3U and 6U cPCI, and AMC.
As shown in the above screen shot, Navigator IP blocks work directly in Xilinx Vivado.

This screen shot shows Navigator IP blocks which are selectable from a pull-down menu.
Navigator BSP (Board Support Package)

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately. ➤

![Navigator BSP Signal Analyzer](image-url)
Optimize BSP and IP Development

For users who need to develop applications that include custom IP, the combination and compatibility of Navigator FDK and Navigator BSP streamline development.

When new IP is introduced into the design, it has the potential of changing how the hardware looks to the host, possibly breaking the software. Navigator FDK and BSP were designed together to closely match the FPGA IP blocks and the BSP functions that control them. As developers modify IP they can easily find the corresponding BSP functions and modify them in parallel.

Navigator FDK uses AXI4 for all IP block interfaces. When developers create their own IP blocks using AXI4, they are immediately compatible with the Pentek-supplied IP. Following the Navigator BSP style guide, users can similarly create BSP modules for compatibility with the Navigator BSP library.
**Model 4953**

**GateFlow®** is Pentek’s family of extendable FPGA products. The GateFlow product line includes the GateFlow FPGA Design Kit to ease custom algorithm development and the GateFlow Factory-installed IP Cores in Pentek FPGA board products.

The Pentek Model 4953 GateFlow FPGA Design Kit provides the user with design information, software files and utilities for extending FPGA functions in these products.

Users can implement a variety of custom preprocessing functions such as convolution, framing, pattern recognition, decompression, FFT, delay, decoding, time stamping, averaging, summation and many more.

**Using the FPGA Design Kit**

The GateFlow FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt, Onyx and Flexor architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

**The User Application Container**

Shown below is the FPGA block diagram of a typical Cobalt, Onyx or Flexor module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports that surround the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation or Vivado project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each module provides an example of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.
### Available Resources

The chart below shows the Xilinx FPGA families used in the three Pentek families of board-level products. These products use some FPGA resources to implement standard factory functions as well as installed IP cores. The chart shows the approximate percentage of unused system slices and RAM available to the user for extending the FPGA to include custom algorithms for the user’s application.

<table>
<thead>
<tr>
<th>Pentek Model</th>
<th>Board Type</th>
<th>No. of FPGAs</th>
<th>Logic Cells</th>
<th>CLB Slices</th>
<th>CLB Flip-Flops</th>
<th>Max. Block RAM</th>
<th>DSP 48E Blocks</th>
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*Cobalt form factors: 716xx = XMC; 726xx = 6U CPCI; 736xx = 3U CPCI; 746xx = 6U CPCI (Dual XMC); 786xx = x8 PCIe; 536xx = 3U VPX - Format 1; 526xx = 3U VPX - Format 2; 566xx = AMC; 576xx = 6U VPX; 586xx = 6U VPX (Dual XMC)  
**Onyx form factors: 717xx = XMC; 727xx = 6U CPCI; 737xx = 3U CPCI; 747xx = 6U CPCI (Dual XMC); 787xx = x8 PCIe; 537xx = 3U VPX - Format 1; 527xx = 3U VPX - Format 2; 567xx = AMC; 577xx = 6U VPX; 587xx = 6U VPX (Dual XMC)  
***Kintex form factors: 718xx = XMC; 728xx = 6U CPCI; 738xx = 3U CPCI; 748xx = 6U CPCI (Dual XMC); 788xx = x8 PCIe; 538xx = 3U VPX - Format 1; 528xx = 3U VPX - Format 2; 568xx = AMC; 578xx = 6U VPX; 588xx = 6U VPX (Dual XMC)  

Some Kintex Ultra Scale products use 1 in place of 8 - TBD: To Be Determined - N/A: Not Available
General Information

Users of high-performance data acquisition and signal processing boards often find themselves frustrated by the fact that when their new devices are delivered, they are unable to put them to immediate use. Because these boards are largely software controlled and offer a flexible range of functionality, a certain amount of programming is generally necessary to put the new cards through their paces. Then, if something does not go as planned, there is no way of knowing for sure whether the problem lies with the new code, or with the hardware itself.

To address this issue, Pentek has developed the ReadyFlow® BSPs (Board Support Packages) for all its board-level products. These packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code

What’s Included in the Package

In general, functions appropriate to the board-level product, such as:

- A “How to” section
  - Build object libraries
  - Compile and link application programs
- C-callable functions
  - Initialization and test
  - Data movement and communications
  - Backplane I/O
  - Mezzanine peripheral I/O
  - Control of board resources
- Utilities
  - Flash memory program loaders

The package contains C-language examples that can be used to demonstrate the capabilities of Pentek products. The examples included provide the answers to most of the questions that occur with first-time users of Pentek products.

These programming examples will also help you get an immediate start on writing your own application without having to reinvent the wheel. They provide sample code that is known to work, giving you, the new user, a means of verifying that your board set is operational.

ReadyFlow Board Support Packages are designed to reduce development time not only during the initial stages, but any time new hardware is added to the system. All packages are built with a consistent style and function-naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware as it’s added further shortening the learning curve.

Command Line Interface

The Command Line Interface provides access to precompiled executable examples that operate the hardware right out of the box, without the need to write any code.

Board-specific hardware operating arguments can be entered in the command line to control the following parameters: number of channels to enable, sample clock frequency, data transfer size, data rate divider, interpolation factor, reference clock frequency, reference clock source, number of iterations to run the program, etc.

Below is an example command line for D/A capable hardware that enables the channel one output, transfers 32,768 data bytes, executes 100,000 times, divides the data rate by 2, and interpolates the data by 4:

```c
C:> dacmode -chan 1 -xfersize 32768 -loop 100000 -ratediv 2 -interpolate 4
```

The Command Line Interface can be used to call an example application from within a larger user application to control the hardware, and parameter arguments are passed to the application for execution. Functions that control data acquisition, automatically save captured data to a pre-named host file or are routed to the Signal Analyzer example function for display.
Signal Analyzer*

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.

Example, Model 71620

As an example of XMC module support, the BSP for the Cobalt® Model 71620 Transceiver with three 200 MHz A/Ds, DUC (Digital Upconverter), and two 800 MHz D/As includes data structures and routines to support the following:

- PCIe Bus interface and DMA controller
- Board control registers
- Timing bus control and clock selection
- Triggering, gate enable and polarity
- Data input device management for the 200 MHz A/D
- Data output device management for the DUC and the 800 MHz D/A
- Built-in A/D Data Acquisition IP Modules
- Built-in D/A Waveform Playback IP Modules
- Built-in test waveform generator
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor
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■ Backplane I/O
■ Mezzanine peripheral I/O
■ Control of board resources
■ Utilities
■ Flash memory program loaders

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ReadyFlow Board Support Packages are designed to reduce development time not only during the initial stages, but any time new hardware is added to the system. All packages are built with a consistent style and function-naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware as it’s added further shortening the learning curve.

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C:> dacmode -chan 1 -xfersize 32768
     -loop 100000 -ratediv 2
     -interpolate 4

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Signal Analyzer

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals.

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- PCIe Bus interface and DMA controller
- Board control registers
- Timing bus control and clock selection
- Triggering, gate enable and polarity
- Data input device management for the 200 MHz A/D
- Data output device management for the DUC and the 800 MHz D/A
- Built-in A/D Data Acquisition IP Modules
- Built-in D/A Waveform Playback IP Modules
- Built-in test waveform generator
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor
The Models 4996/4996A VxWorks BSPs provide software developers with a complete library of hardware initialization, control and application functions for Pentek PowerPC®/Power Architecture® processor baseboards, VME/VXS, PMC/XMC, VIM, and cPCI boards and modules. Used in conjunction with Wind River’s Workbench® software development environment, they speed application development by providing a high-level API for accessing all of the processor board’s memory and communication resources, and control of the board’s I/O interfaces and I/O modules.

Processor specific functions found in the baseboard BSPs include: cache, DMA, SDRAM, interrupt, serial port, and timer control. Some general board functions include: reading and writing to mezzanine board FIFOs, VME/VXS, PMC/XMC, cPCI, and VIM I/O control, interprocessor communication, programming DMA reads and writes, programming interrupts, using mailboxes, managing RS-232 and ethernet interfaces, and control of optional Fibre Channel interfaces.

The VxWorks BSPs are designed to reduce development time not only during the initial stages of software development, but any time new I/O hardware is added to the system. Hardware Drivers, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and function naming convention. Similar parameters on different I/O modules have similar driver calls, thereby allowing immediate familiarity with new I/O hardware as it’s added. This can greatly shorten the application development learning curve when a system is modified or expanded.
Wind River’s Workbench development platform has dramatically improved embedded developers’ “time-to-productivity”. A component of Workbench, Workbench Tools, comprises a comprehensive suite of core and optional cross-development tools and utilities. The other integrated components of Workbench consist of the VxWorks run-time system, a high-performance scalable real-time operating system that executes on the target processor and a full range of communications options for the target connection to the host. Workbench Tools provides a highly visual and automated environment that accelerates the development of even the most complex VxWorks-based applications.

At the heart of the VxWorks run-time system is the highly efficient Wind microkernel which supports a full range of real-time features. These include fast multitasking, interrupt support, and both preemptive and round-robin scheduling. The microkernel design minimizes system overhead and enables fast, deterministic response to external events.

Ordering Information
Contact Wind River Systems at:
www.windriver.com
**General Information**

The Pentek SystemFlow Recording Software provides a rich set of function libraries and tools for controlling and building Pentek’s real-time recording and data acquisition systems. These libraries ensure a consistent look and feel for developers across system families.

SystemFlow software allows developers to configure and customize system interfaces and behavior. It includes API functions not only for the real-time data acquisition and playback functions, but also for the user-control software running on the host PC including the GUI. These API functions allow developers to either modify the sample code to meet their needs or use it as a reference for custom software development.

**API Library Components**

SystemFlow is based on a flexible client/server architecture. The host client application runs on a Windows or Linux platform and communicates with the server target application via a standard socket connection. In this way, server real-time recording and/or playback operations can be controlled from a local or remote host client.

All servers use PC hardware running under Windows. The server application includes scheduling, task management, full control of data from Pentek software radio hardware, and drivers for communication with the hard disk arrays.

**SystemFlow Recorder Interface**

The SystemFlow GUI provides the user with a control interface for recording data. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

**Hardware Configuration Interface**

The SystemFlow configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit checking and integrated help to provide an easier-to-use out-of-the-box experience.

**SystemFlow Signal Viewer**

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We’re glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at: Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900 • fax: 201-818-5697 • email: custsvc@pentek.com