PENTEK
Analog & Digital I/O
## Model Description

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cobalt 71630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57630 &amp; 58630</td>
<td>1-/2-Ch 1 GHz A/D and 1-/2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72630, 73630, 74630</td>
<td>1-/2-Ch 1 GHz A/D and 1-/2-Ch 1 GHz D/A, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 71640</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78640</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53640</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52640</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57640 &amp; 58640</td>
<td>1-/2-Ch 3.6 GHz or 2-/4-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72640, 73640, 74640</td>
<td>1-/2-Ch 3.6 GHz or 2-/4-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56640</td>
<td>1-Ch 3.6 GHz or 2-Ch 1.8 GHz 12-bit A/D, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 71660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57660 &amp; 58660</td>
<td>4-/8-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72660, 73660, 74660</td>
<td>4-/8-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56660</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 71663</td>
<td>1100 GSM Channelizer with Quad A/D - XMC</td>
</tr>
<tr>
<td>Cobalt 78663</td>
<td>1100 GSM Channelizer with Quad A/D - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53663</td>
<td>1100 GSM Channelizer with Quad A/D - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52663</td>
<td>1100 GSM Channelizer with Quad A/D - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57663 &amp; 58663</td>
<td>1100/2200 GSM Channelizer with Quad/Octal A/D - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72663, 73663, 74663</td>
<td>1100/2200 GSM Channelizer with Quad/Octal A/D - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56663</td>
<td>1100 GSM Channelizer with Quad A/D - AMC</td>
</tr>
<tr>
<td>Cobalt 71670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57670 &amp; 58670</td>
<td>4-/8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72670, 73670, 74670</td>
<td>4-/8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 71690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>MODEL</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Cobalt 57690 &amp; 58690</td>
<td>1-/2-Ch L-Band RF Tuner, 2-/4-Ch 200 MHz A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72690, 73690, 74690</td>
<td>1-/2-Ch L-Band RF Tuner, 2-/4-Ch 200 MHz A/D, Virtex-6 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56690</td>
<td>L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 71760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - XMC</td>
</tr>
<tr>
<td>Onyx 78760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Onyx 53760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Onyx 52760</td>
<td>4-/8-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 57760 &amp; 58760</td>
<td>4-/8-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Onyx 72760, 73760, 74760</td>
<td>4-Channel 200 MHz, 16-bit A/D, Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Onyx 56760</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - XMC</td>
</tr>
<tr>
<td>Onyx 71730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Onyx 78730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Onyx 53730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Onyx 52730</td>
<td>1-/2-Ch 1 GHz A/D and 1-/2-Ch 1 GHz D/A, Virtex-7 FPGAs - 6U VPX</td>
</tr>
<tr>
<td>Onyx 72730, 73730, 74730</td>
<td>1-/2-Ch 1 GHz A/D and 1-/2-Ch 1 GHz D/A, Virtex-7 FPGAs - 6U/3U cPCI</td>
</tr>
<tr>
<td>Onyx 56730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - AMC</td>
</tr>
<tr>
<td>Onyx 71741</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - XMC</td>
</tr>
<tr>
<td>Onyx 78741</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - 8 PCIe</td>
</tr>
<tr>
<td>Onyx 53741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Onyx 52741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Onyx 57741 &amp; 58741</td>
<td>1-/2-Ch. 3.6 GHz or 2-/4-Ch. 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>Onyx 72741, 73741, 74741</td>
<td>1-/2-Ch. 3.6 GHz or 2-/4-Ch. 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - 6U/3U cPCI</td>
</tr>
<tr>
<td>Onyx 56741</td>
<td>1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, DDC, Virtex-7 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 71610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - 8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57610 &amp; 58610</td>
<td>Single or Dual LVDS Digital I/O with Virtex-6 FPGAs - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72610, 73610, 74610</td>
<td>Single or Dual LVDS Digital I/O with Virtex-6 FPGAs - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - AMC</td>
</tr>
<tr>
<td>Cobalt 7811</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 71611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Cobalt 78611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Cobalt 53611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX - Format 1</td>
</tr>
<tr>
<td>Cobalt 52611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX - Format 2</td>
</tr>
<tr>
<td>Cobalt 57611 &amp; 58611</td>
<td>Quad or Octal Serial FPDP Interface with Virtex-6 FPGAs - 6U VPX</td>
</tr>
<tr>
<td>Cobalt 72611, 73611, 74611</td>
<td>Quad or Octal Serial FPDP Interface with Virtex-6 FPGAs - 6U/3U cPCI</td>
</tr>
<tr>
<td>Cobalt 56611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>
MODEL

Jade 71141  
Jade 78141  
Jade 53141  
Jade 52141  
Jade 57141 & 58141  
Jade 72141, 73141, 74141  
Jade 56141  
Flexor 5973  
Flexor 5983  
Flexor 7070  
Flexor 3312  
FlexorSet 5973-312  
FlexorSet 5983-313  
FlexorSet 7070-312  
Flexor 3316  
FlexorSet 5973-316  
FlexorSet 5983-317  
FlexorSet 7070-316  
Flexor 3320  
FlexorSet 5973-320  
FlexorSet 5983-320  
FlexorSet 7070-320  
Flexor 3324  
FlexorSet 5973-324  
FlexorSet 5983-324  
FlexorSet 7070-324  
Bandit 7120  
Bandit 7820  
Bandit 5220  
Bandit 5720 & 5820  
Bandit 7220, 7320, 7420  
Bandit 5620  
Bandit 8111  
8264  
8266  
8267

DESCRIPTION

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - XMC
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - x8 PCIe
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - 3U VPX
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - 6U VPX
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - 6U/3U cPCI
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex FPGA - AMC
Virtex-7 Processor and FMC Carrier - 3U VPX
Kintex UltraScale Processor and FMC Carrier - 3U VPX
Virtex-7 Processor and FMC Carrier - x8 PCIe

4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - FMC
4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - 3U VPX
4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - x8 PCIe
4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - 3U VPX
4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - x8 PCIe

8-Channel 250 MHz, 16-bit A/D - FMC
8-Channel 250 MHz, 16-bit A/D - Virtex-7 FPGA - 3U VPX
8-Channel 250 MHz, 16-bit A/D - Virtex-7 FPGA - x8 PCIe
2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - FMC
2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - 3U VPX
2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 - x8 PCIe
4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - FMC
4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - 3U VPX
Kintex 4-Channel 250 MHz, 16-bit A/D, 2-Channel 800 MHz, 16-bit D/A - x8 PCIe
4-Channel 500 MHz, 16-bit A/D, 4-Channel 1.5 GHz, 16-bit D/A - 3U VPX
Two-Channel Analog RF Wideband Downconverter - PMC/XMC
Two-Channel Analog RF Wideband Downconverter - PCIe
Two-Channel Analog RF Wideband Downconverter - 3U VPX
Two- or Four-Channel Analog RF Wideband Downconverter - x8 PCIe
Two- or Four-Channel Analog RF Wideband Downconverter - 6U OpenVPX
Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI
Two-Channel Analog RF Wideband Downconverter - AMC
Modular Analog RF Slot Downconverter Series
6U OpenVPX Development System for Cobalt and Onyx Boards
PC Development System for PCIe Cobalt and Onyx Boards
3U VPX Development System for Cobalt, Onyx and Flexor Boards

Customer Information
General Information

Model 71630 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for development and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71630 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Acquisition IP Module
The 71630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a linked definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module
The Model 71630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage
The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage
The 71630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors allowing large, multichannel synchronous configurations. Also, an LV TTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources
The 71630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
Model 71630

1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - XMC

XMC Interface
The Model 71630 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71630 supports 8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface
The Model 71630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits
Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Memory
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description
8266 PC Development System
See 8266 Datasheet for Options

Model Ordering Information
Model Description
71630 1 GHz A/D and D/A, Virtex-6 FPGA - XMC

Options:
-002* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

General Information

Model 78630 is a member of the Cobalt\textsuperscript{\textregistered} family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-\(\mu\)Sync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

---

**General Information**

Model 78630 is a member of the Cobalt\textsuperscript{\textregistered} family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general-purpose and gigabit serial card connectors for application specific I/O protocols.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-\(\mu\)Sync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

---

Pentek, Inc.  One Park Way • Upper Saddle River • New Jersey 07458  Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com  www.pentek.com
A/D Acquisition IP Module

The 78630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 78630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

D/A Converter Stage

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Memory Resources

The 78630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.➤
Model 78630
1 GHz A/D and 1 GHz D/A with Virtex-6 FPGA - x8 PCIe

PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

A/D Converter
- Type: Texas Instruments ADS5400
- Sampling Rate: 100 MHz to 1 GHz
- Resolution: 12 bits

D/A Converter
- Type: Texas Instruments DAC5681Z
- Input Data Rate: 1 GHz max.
- Interpolation Filter: bypass, 2x or 4x
- Output Sampling Rate: 1 GHz max.
- Resolution: 16 bits

Front Panel Analog Signal Outputs

A/D and D/A with Virtex-6 FPGA - x8 PCIe

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model Description
78630 1 GHz A/D and D/A, Virtex-6 FPGA - x8 PCIe

Options:
- 002 -2 FPGA speed grade
- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS FPGA I/O through 68-pin ribbon cable connector
- 105 Gigabit serial FPGA I/O through two 4X top edge connectors
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O

Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen.1: x4 or x8
Gen. 2: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.
Model 53630 COTS (left) and rugged version

General Information

Model 53630 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**Model 53630**

**A/D Acquisition IP Module**

The 53630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The 53630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 5392 and Model 9192 Cobalt Synchronizers can drive multiple 53630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

**Memory Resources**

The 53630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**SPARK Development Systems**

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>53630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX</td>
<td>-002* -2 FPGA speed grade</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-062 Xilinx VC6LX240T FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-064 Xilinx VC6LX315T FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-104 LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-105 Gigabit serial FPGA I/O to VPX P1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

- This option is always required

---

**Contact Pentek for availability of rugged and conduction-cooled versions**

---

**VPX Families**

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

---

**VPX Family Comparison**

<table>
<thead>
<tr>
<th></th>
<th>Form Factor</th>
<th># of XMCs</th>
<th>Crossbar Switch</th>
<th>PCIe Path</th>
<th>PCIe Width</th>
<th>Option -104 Path</th>
<th>Option -105 Path</th>
<th>Lowest Power</th>
<th>Lowest Price</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
<td>3U VPX</td>
<td>One XMC</td>
<td>No</td>
<td>VPX P1</td>
<td>x4</td>
<td>20 pairs on VPX P2</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>53xxx</td>
<td></td>
<td></td>
<td>Yes</td>
<td>VPX P1 or P2</td>
<td>x8</td>
<td></td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
General Information

Model 52630 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52630 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The XST part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-μSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

The 52630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52630 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 52630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 and to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 5292 and Model 9192 Cobalt Synchronizers can drive multiple 52630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 52630 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and it is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 02 -2 FPGA speed grade
- 08 Xilinx Virtex-6 XC6VFX360T FPGA
- 04 Xilinx Virtex-6 XC6VSX315T FPGA
- 10 Gigabit serial FPGA I/O to VPX P2
- 15 Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- 155 Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
- 165 Two 512 MB DDR3 SDRAM memory banks (Banks 3 and 4)

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

---

**Model 52630**

1 GHz A/D and D/A, Virtex-6 FPGA - 3U VPX

- **PCI Express Interface**
  
  The Model 52630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

- **Specifications**
  
  **Front Panel Analog Signal Inputs**
  
  - A/D Converter
    - Type: Texas Instruments ADS5400
    - Sampling Rate: 100 MHz to 1 GHz
    - Resolution: 12 bits
  
  - D/A Converter
    - Type: Texas Instruments DAC5681Z
    - Input Data Rate: 1 GHz max.
    - Interpolation Filter: bypass, 2x or 4x
    - Output Sampling Rate: 1 GHz max.
    - Resolution: 16 bits
  
  **Front Panel Analog Signal Outputs**
  
  - Output Type: Transformer-coupled, front panel female SSMC connectors
  
  **Clock Synthesizer**
  
  - Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  
  **External Clock**
  
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

- **Timing Bus:** 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

- **External Trigger Input**
  
  - Type: Front panel female SSMC connector, LVTTL
  
  **Field Programmable Gate Array**
  
  - Standard: Xilinx Virtex-6 XC6VLX130T-2
  
  **Custom I/O**
  
  - Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
  
  **Memory**
  
  - Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  
  **VPX Families**
  
  Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

---

**VPX Family Comparison**

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
General Information

Models 57630 and 58630 are members of the Cobalt family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a VPX carrier board.

Model 57630 is a 6U board with one Model 71630 module while the Model 58630 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The XXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit A/D
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
### A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

### D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

### A/D Converter Stage

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

### D/A Converter Stage

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

### Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latest mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

### Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

---

**VIRTEX-6 FPGA DATAFLOW DETAIL**

```
+---------------------+  +---------------------+  +---------------------+
|                    |   |                    |   |                    |
| INPUT MULTIPlexer  |   | MEMORY CONTROLLER  |   | MEMORY CONTROLLER   |
|                    |   |                    |   |                    |
|                    |   | DATA PACKING & FLOW |   | DATA PACKING & FLOW |
|                    |   | CONTROL            |   | CONTROL            |
|                    |   |                    |   | MEM to MUX         |
|                    |   |                    |   | MUX                |
|                    |   |                    |   | MEM to Mem Bank 1  |
|                    |   |                    |   | Mem Bank 1 to Mem|
|                    |   |                    |   | Mem Bank 2 to Mem|
|                    |   |                    |   | Mem Bank 3 to Mem|
|                    |   |                    |   | Mem Bank 4 to Mem|
|                    |   |                    |   | Mem Bank 1 to Mem|
|                    |   |                    |   | Mem Bank 2 to Mem|
|                    |   |                    |   | Mem Bank 3 to Mem|
|                    |   |                    |   | Mem Bank 4 to Mem|
|                    |   |                    |   |                   |
|                    |   |                    |   | MEMORY GENERATION |
|                    |   |                    |   | LINKED-LIST DMA    |
|                    |   |                    |   | ENGINE            |
|                    |   |                    |   |                   |
|                    |   |                    |   | WAVEFORM          |
|                    |   |                    |   | PLAYBACK IP       |
|                    |   |                    |   | MODULE            |
|                    |   |                    |   |                  |
|                    |   |                    |   | PCIe              |
|                    |   |                    |   |                  |
|                    |   |                    |   |                   |
|                    |   |                    |   |                  |
|                    |   |                    |   |                  |
|                    |   |                    |   |                  |
+---------------------+  +---------------------+  +---------------------+
```

**Memory Resources**

- 1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

---

Pentek, Inc.  One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com  www.pentek.com
Models
57630 & 58630

1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-6 FPGA - 6U OpenVPX

Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57630</td>
<td>1 GHz A/D and D/A with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58630</td>
<td>Two 1 GHz A/D and D/A, with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:
-02* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS I/O between the FPGA and P3 connector, Model 57630; P3 and P5 connectors, Model 58630
-105 Gigabit link between the FPGA and P2 connector, Model 57630; gigabit links from each FPGA to P2 connector, Model 78630
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8264
VPX Development System. See 8264 Datasheet for Options

PCI Express Interface
These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57630: 1 A/D, 1 D/A
Model 58630: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)
Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converters (1 or 2)
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)
Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)
On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus (1 or 2): 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57630; P3 and P5, Model 58630
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57630; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58630

Memory Banks (1 or 2)
Option 150: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI Express Interface

PCI Express Bus: Gen. 1 or 2: x4 or x8

Environmental:
Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 72630, 73630 and 74630 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71630 XMC modules mounted on a cPCI carrier board.

Model 72630 is a 6U cPCI board while the Model 73630 is a 3U cPCI board; both are equipped with one Model 71630 XMC. Model 74630 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP module. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these modules to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Up to 2 or 4 GB of DDR3 SDRAM; or: 16 MB or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

---

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
**A/D Acquisition IP Module**

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Modules**

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**A/D Converter Stage**

The front end accepts one or two analog HF or IF input on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**D/A Converter Stage**

The 71630 features one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data.

Analog output is through front panel SSMC connectors.

**Clocking and Synchronization**

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.

Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7292 and Model 9192 Cobalt Synchronizers can drive multiple µSync connectors enabling large, multi-channel synchronous configurations. Also, an LVTTI external gate/trigger input is accepted on a front panel SSMC connector.

**Memory Resources**

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.
1-or 2-Channel 1 GHz A/D, 1-or 2-Channel 1 GHz D/A with Virtex-6 FPGA - cPCI

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73630: 32 bits only.

Specifications

Model 72630 or Model 73630: 1 A/D, 1 D/A
Model 74630: 2 A/Ds, 2 D/A

Front Panel Analog Signal Inputs (1 or 2)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converters (1 or 2)

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

Environmental

Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74630</td>
<td>Two 1 GHz A/D and D/A, Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:

-002*  -2 FPGA speed grade
-062   XC6VLX240T FPGA
-064   XC6VSX315T FPGA
-104   LVDS I/O between the FPGA and J2 connector, Model 73630; J3 connector, Model 72630; J3 and J5 connectors, Model 74630
-160   Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155   Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165   Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required
**General Information**

Model 56630 is a member of the Cobalt® family of high performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56630 includes a front panel general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- Up to 2 GB of DDR3 SDRAM or 16 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Module

The 56630 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A. The circuitry is designed with associated memory banks for storing data in transient capture mode. Memory is available in four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as a combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. The internal memory functions include an A/D data transient capture mode and D/A waveform playback mode.

D/A Converter Stage

The 56630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO.
1 GHz A/D and 1 GHz D/A, Virtex-6 FPGA - AMC

**AMC Interface**

The Model 56630 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or μTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **A/D Converter**
  - **Type**: Texas Instruments ADS5400
  - **Sampling Rate**: 100 MHz to 1 GHz
  - **Resolution**: 12 bits
- **D/A Converter**
  - **Type**: Texas Instruments DAC5681Z
  - **Input Data Rate**: 1 GHz max.
  - **Interpolation Filter**: bypass, 2x or 4x
  - **Output Sampling Rate**: 1 GHz max.
  - **Resolution**: 16 bits

**Front Panel Analog Signal Outputs**

- **Output Type**: Transformer-coupled, front panel female SSMC connectors
- **Sample Clock Sources**: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock
- **Clock Synthesizer**
  - **Clock Source**: Selectable from on-board programmable VCXO or front panel external clock
  - **VCXO Frequency Ranges**: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  - **Synchronization**: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
  - **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>56630</td>
<td>1 GHz A/D and D/A, Virtex-6 FPGA - AMC</td>
<td>-002* -2 FPGA speed grade&lt;br&gt;-062 XC6VLX240T FPGA&lt;br&gt;-064 XC6VSX315T FPGA&lt;br&gt;-104 LVDS FPGA I/O through front panel connector&lt;br&gt;-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)&lt;br&gt;-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)&lt;br&gt;-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**
General Information

Model 71640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71640 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support other serial protocols.

---

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multimodule synchronization
- PCI Express Gen. 2 interface x8 wide
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Conversion Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 71640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 71640s can be synchronized using the Cobalt high speed sync module to drive the sync bus.

Memory Resources

The 71640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71640 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 5 GHz bit clock. With dual XMC connectors, the 71640 supports x8 PCIe on the first XMC connector leaving the optional second connector free to support user-installed transfer protocols specific to the target application.

A/D Acquisition IP Module

The 71640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC

PCI Express Interface

The Model 71640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable
Sample Clock Sources: Front panel SSMC connector
Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input
Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC</td>
</tr>
</tbody>
</table>

Options:
-002* -2 FPGA speed grade
-062 XC6VLX240T
-064 XC6VSX315T
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

PC Development System
See 8266 Datasheet for Options
Model 78640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

General Information
Model 78640 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 78640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78640 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture
The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features
- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Pentek, Inc.  One Park Way ◆ Upper Saddle River ◆ New Jersey 07458
Tel: 201-818-5900 ◆ Fax: 201-818-5904 ◆ Email: info@pentek.com
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 78640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 78640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 78640s can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The 78640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input

Type: Front panel female SSMC connector

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T-2

Optional: Xilinx Virtex-6 XC6VLX240T-2 XC6VSX315T-2

Custom I/O

Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model 78640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - x8 PCIe

Options:

-002* -2 FPGA speed grade

-062 XC6VLX240T FPGA

-064 XC6VSX315T FPGA

-104 LVDS FPGA I/O through 68-pin ribbon cable connector

-105 Gigabit serial FPGA I/O through two 4X top edge connectors

-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)

-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Model 8266

PC Development System

See 8266 Datasheet for Options
General Information

Model 53640 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a program- mable 15-bit gain adjustment allowing the 53640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 53640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 53640’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 53640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links of x4 or x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

---

**A/D Acquisition IP Module**

The 53640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

_model 53640_

Fabric-Transparent Crossbar Switch

The 53640 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency.

Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **A/D Converter**
  - **Type**: Texas Instruments ADC12D1800
  - **Sampling Rate**: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  - **Resolution**: 12 bits
  - **Input Bandwidth**: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  - **Full Scale Input**: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out reference clock

External Trigger Input

- **Type**: Front panel female SSMC connector
- **Function**: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VX315T-2

Custom I/O

- **Option -104**: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105**: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus**: Gen. 1or Gen. 2: x4 or x8

Environmental

- **Operating Temp**: 0° to 50° C
- **Storage Temp**: –20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

---

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options:</th>
</tr>
</thead>
<tbody>
<tr>
<td>53640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>-002* -2 FPGA speed grade</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-062 XC6VLX240T FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-064 XC6VX315T FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-104 LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-105 Gigabit serial FPGA I/O to VPX P1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

---

Model 8267

VPX Development System. See 8267 Datatsheet for Options

---
Model 52640

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, V-6 FPGA - 3U VPX

General Information

Model 52640 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52640 includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols. ▶

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 52640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

The 52640 accepts an 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multipin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 52640’s can be synchronized using the Cobalt high-speed sync board to drive the sync bus.

Memory Resources

The 52640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s data and capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52640 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Acquisition IP Module

The 52640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**

-002* - 2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

---

**Specifications**

**Front Panel Analog Signal Inputs**

*Input Type:* Transformer-coupled, front panel female SSMC connectors

**A/D Converter**

*Type:* Texas Instruments ADC12D1800

*Sampling Rate:* Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

*Resolution:* 12 bits

*Input Bandwidth:* Single-channel: 1.75 GHz; dual-channel: 2.8 GHz

*Full Scale Input:* +2 dBm to +4 dBm, programmable

**Sample Clock Sources:** Front panel SSMC connector

**Sync Bus:** Multi-pin connectors, bus includes gate, reset and in and out reference clock

**External Trigger Input**

*Type:* Front panel female SSMC connector, TTL

*Function:* Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

*Standard:* Xilinx Virtex-6 XC6VLX130T-2

*Optional:* Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**

*Option -104:* Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

*Option -105:* Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

*PCI Express Bus:* Gen. 1 or Gen. 2: x4

**Environmental**

*Operating Temp:* 0° to 50° C

*Storage Temp:* -20° to 90° C

*Relative Humidity:* 0 to 95%, non-cond.

*Size:* 3.937 in. x 6.717 in. (100 mm x 170.6 mm).

---

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
<td>VPX P1 or P2</td>
<td>VPX P1</td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
<td>20 pairs on VPX P2</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
**General Information**

Models 57640 and 58640 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a VPX carrier board.

Model 57640 is a 6U board with one Model 71640 module while the Model 58640 is a 6U board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57640, P3 and P5, Model 58640.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57640; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58640. ➤

---

**Features**

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 or 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- μSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
**Models 57640 & 58640**

**1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U OpenVPX**

**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Specifications**

- **Model 57640**: One A/D
- **Model 58640**: Two A/Ds
- **Front Panel Analog Signal Inputs (2 or 4)**
  - **Input Type**: Transformer-coupled, front panel female SSMC connectors
- **A/D Converter (1 or 2)**
  - **Type**: Texas Instruments ADC12D1800
  - **Sampling Rate**: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  - **Resolution**: 12 bits
- **Input Bandwidth**
  - Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input**: +2 dBm to +4 dBm, programmable
- **Sample Clock Sources (1 or 2)**
  - Front panel SSMC connector
- **Sync Bus (1 or 2)**
  - Multi-pin connectors, bus includes gate, reset and in and out ref clock
- **External Trigger Input (1 or 2)**
  - **Type**: Front panel female SSMC connector, TTL
  - **Function**: Programmable functions include: trigger, gate, sync and PPS
- **Field Programmable Gate Array (1 or 2)**
  - **Standard**: Xilinx Virtex-6 XC6VLX130T-2
  - **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2
- **Custom I/O**
  - **Option -104**: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57640; P3 and P5, Model 58640
  - **Option -105**: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57640; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58640
- **Memory Banks (1 or 2)**
  - Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
- **PCI-Express Interface**
  - **PCI Express Bus**: Gen. 1 or 2: x4 or x8
- **Environmental**
  - **Level L1 & L2 air-cooled**
  - **Level L3 ruggedized, conduction-cooled**
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58640</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS I/O between the FPGA and P3 connector, Model 57640; P3 and P5 connectors, Model 58640
- **-105** Gigabit link between the FPGA and P2 connector, Model 57640; gigabit links from each FPGA to P2 connector, Model 78640
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

*These options are always required*

---

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8264</td>
<td>VPX Development System. See 8264 Datasheet for Options</td>
</tr>
</tbody>
</table>
General Information

Models 72640, 73640 and 74640 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board.

Model 72640 is a 6U cPCI board while the Model 73640 is a 3U cPCI board; both are equipped with one Model 71640 XMC. Model 74640 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turn-key solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- One or two 1-channel mode with 3.6 GHz, 12-bit A/Ds
- Two or four 2-channel mode with 1.8 GHz, 12-bit A/Ds
- 2 or 4 GB of DDR3 SDRAM
- Sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple boards to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple boards can be synchronized using the Cobalt high speed sync board to drive the sync bus.

Memory Resources

The Cobalt architecture supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s memory and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73640: 32 bits only.

A/D Acquisition IP Modules

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP modules can receive data from the A/Ds, or a test signal generator. The IP modules have associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
# 1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - cPCI

## Specifications

**Model 72640 or Model 73640: One A/D**
**Model 74640: Two A/Ds**

**Front Panel Analog Signal Inputs (2 or 4)**
- **Input Type**: Transformer-coupled, front panel female SSMC connectors

**A/D Converter (1 or 2)**
- **Type**: Texas Instruments ADC12D1800
- **Sampling Rate**: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
- **Resolution**: 12 bits
- **Input Bandwidth**: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
- **Full Scale Input**: +2 dBm to +4 dBm, programmable

**Sample Clock Sources (1 or 2)**
- Front panel SSMC connector

**Sync Bus (1 or 2)**
- Multi-pin connectors, bus includes gate, reset and in and out ref clock

**External Trigger Input (1 or 2)**
- **Type**: Front panel female SSMC connector, TTL
- **Function**: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array (1 or 2)**
- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**
- **Option -104**: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640

**Memory Banks (1 or 2)**
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-X Interface**
- **PCI-X Bus**: 32 or 64 bits at 33 or 66 MHz
- **Model 73640**: 32 bits only

**Environmental**
- **Operating Temp**: 0° to 50° C
- **Storage Temp**: -20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.

**Size**: Standard 6U or 3U cPCI board

## Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73640</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74640</td>
<td>2-Ch. 3.6 GHz or 4-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**
- -002* -2 FPGA speed grade
- -062 XC6VLX240T
- -064 XC6VSX315T
- -104 LVDS I/O between the FPGA and the J2 connector, Model 73640; J3 connector, Model 72640; J3 and J5 connectors, Model 74640
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required
General Information

Model 56640 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56640 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56640 factory-installed functions include an A/D acquisition IP module. In addition, IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56640 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 56640 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**Clocking and Synchronization**

The 56640 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel multi-pin sync bus connector allows multiple modules to be synchronized, ideal for larger multichannel systems. The sync bus includes gate, reset and in and out reference clock signals. Multiple 56640’s can be synchronized using the Cobalt high speed sync module to drive the sync bus.

**Memory Resources**

The 56640 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and data capture capabilities. Built-in memory functions include an A/D data transient capture mode for taking snapshots of data for transfer to a host computer.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**AMC Interface**

The Model 56640 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

---

**A/D Acquisition IP Module**

The 56640 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
PCI Express Interface

The Model 56640 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Sample Clock Sources: Front panel SSMC connector

Sync Bus: Multi-pin connectors, bus includes gate, reset and in and out ref clock

External Trigger Input

Type: Front panel female SSMC connector, TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2, or XC6VSX315T-2

Custom I/O

Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1 or Gen. 2: 4 or 8

AMC Interface

Type: AMC.1
Module Management: IPMI Version 2.0

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model  Description
56640  1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - AMC

Options:

-002*  -2 FPGA speed grade
-062   XC6VLX240T
-064   XC6VSX315T
-104   LVDS FPGA I/O through front panel connector
-155*  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165*  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 71660 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SX315T part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.
A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 71660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71660 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 6 GHz bit clock. With dual XMC connectors, the 71660

A/D Acquisition IP Modules

The 71660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

_model_71660_
**Model 71660**

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - XMC

➤ supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

**PCI Express Interface**

The Model 71660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Inputs**

- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**

- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock

**Clock Synthesizer**

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**

- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
- **Option -105:** Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

**Memory**

- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Standard XMC module, 2.91 in. x 5.87 in.

---

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71660</td>
<td>4-Channel 200 MHz A/D with Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>Options:</td>
<td></td>
</tr>
<tr>
<td>-062</td>
<td>XC6VLX240T FPGA</td>
</tr>
<tr>
<td>-064</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O through P14 connector</td>
</tr>
<tr>
<td>-105</td>
<td>Gigabit serial FPGA I/O through P16 connector</td>
</tr>
<tr>
<td>-150</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>-160</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)</td>
</tr>
<tr>
<td>-155</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>-165</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

**Contact Pentek for availability of rugged and conduction-cooled versions**

---

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  
www.pentek.com
General Information

Model 78660 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78660 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory installed applications ideally matched to the board’s analog interfaces. The 78660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP 48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
**A/D Converter Stage**

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 78660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or a combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deep memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 78660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
### Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78660</td>
<td>4-Channel 200 MHz A/D with Virtex-6 FPGA - PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 104 LVDS FPGA I/O through 68-pin ribbon cable connector
- 105 Gigabit serial FPGA I/O through two 4X top edge connectors
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

### Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

### External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

### Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

### Custom I/O
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

### Memory
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

### PCI-Express Interface
- **PCI Express Bus:** Gen. 1: x4 or x8; Gen. 2: x4

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 in. x 7.13 in.
Model 53660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

General Information

Model 53660 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 53660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 53660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Model 8267
The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description | Options |
--- | --- | --- |
53660 | 4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX | -062 XC6VLX240T FPGA, -064 XC6VSX315T FPGA, -104 LVDS FPGA I/O to VPX P2, -105 Gigabit serial FPGA I/O to VPX P1, -150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2), -160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4), -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2), -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |

Model Description
8267 VPX Development System. See 8267 Datasheet for Options

Specifications

Front Panel Analog Signal Inputs
- Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8, Gen. 2: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>
Model 52660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

General Information
Model 52660 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

The 52660 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52660 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Supports gigabit serial fabrics including PCI Express, Serial RapidIO and Xilinx Aurora
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

 Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458 Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com www.pentek.com
A/D Converter Stage
The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources
The 52660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface
The Model 52660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

---

A/D Acquisition IP Modules

The 52660 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique A/D Gate Driven IP module. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
### Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52660</td>
<td>4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 062: XC6VLX240T FPGA
- 064: XC6VSX315T FPGA
- 104: LVDS FPGA I/O to VPX P2
- 105: Gigabit serial FPGA I/O to VPX P1
- 150: Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160: Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

### 4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 3U VPX

#### Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

**Timing Bus:** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

---

### VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

### Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory**
- **Option 150 or 160:** Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 or Gen. 2: x4

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 57660 and 58660 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a VPX carrier board.

Model 57660 is a 6U board with one Model 71660 module while the Model 58660 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660.

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 200 MHz 16-bit A/Ds
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conducton-cooled versions available
A/D Converter Stages

The front end accepts four or eight full-scale analog HF or LF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments AD55485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.
Models
57660 & 58660

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - 6U OpenVPX

➤ Specifications
Model 57660: 4 A/Ds
Model 58660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)
On-board clock synthesizers
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8264
The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model Description
57660: 4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U VPX
58660: 8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS I/O between the FPGA and P3 connector, Model 57660; P3 and P5 connectors, Model 58660
-105 Gigabit link between the FPGA and P2 connector, Model 57660; gigabit links from each FPGA to P2 connector, Model 58660
-150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Model 8264
VPX Development System. See 8264 Datasheet for Options

Model 8264
8264 VPX Development System. See 8264 Datasheet for Options

➤ Specifications
Model 57660: 4 A/Ds
Model 58660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources (1 or 2)
On-board clock synthesizers
Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57660; P3 and P5, Model 58660
Option -105: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57660; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58660

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or 2: x4 or x8
Environmental: Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - cPCI

**General Information**
Models 72660, 73660 and 74660 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71660 XMC modules mounted on a cPCI carrier board.

Model 72660 is a 6U cPCI board while the Model 73660 is a 3U cPCI board; both are equipped with one Model 71660 XMC. Model 74660 is a 6U cPCI board with two XMC modules rather than one. These models include four or eight A/Ds and four or eight banks of memory.

**The Cobalt Architecture**
The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

**Extendable IP Design**
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660.
A/D Acquisition IP Modules
These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or a test signal generator.
Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.
For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage
The front end accepts four or eight full-scale analog HF or LF inputs on front panel SSMC connectors at $+8$ dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADSS485 200 MHz, 16-bit A/D converters.
The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. An alternate clock source can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.
A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the master mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the slave mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Memory Resources
The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.
In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73660: 32 bits only.
Models 72660, 73660 and 74660

4- or 8-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - cPCI

Specifications

Model 72660 or Model 73660: 4 A/Ds
Model 74660: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)
  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
  Type: Texas Instruments ADS5485
  Sampling Rate: 10 MHz to 200 MHz
  Resolution: 16 bits

Sample Clock Sources (1 or 2)
  On-board clock synthesizers

Clock Synthesizers (1 or 2)
  Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
  Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
  Type: Front panel female SSMC connector, LVTTL
  Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
  Standard: Xilinx Virtex-6 XC6VLX130T
  Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
  Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660

Memory Banks (1 or 2)
  Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
  PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
  Model 73660: 32 bits only

Environmental
  Operating Temp: 0° to 50° C
  Storage Temp: -20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74660</td>
<td>8-Channel 200 MHz 16-bit A/D with two Virtex-6 FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
-062    | XC6VLX240T FPGA               |
-064    | XC6VSX315T FPGA               |
-104    | LVDS I/O between the FPGA and J2 connector, Model 73660; J3 connector, Model 72660; J3 and J5 connectors, Model 74660 |
-150    | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2) |
-160    | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4) |
-155    | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2) |
-165    | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4) |
Model 56660
4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

General Information
Model 56660 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56660 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56660 factory-installed functions include four A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56660 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 200 MHz 16-bit A/Ds
- Up to 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56660 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56660 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
Model 56660

4-Channel 200 MHz, 16-bit A/D with Virtex-6 FPGA - AMC

➤ PCI Express Interface

The Model 56660 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -062: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory

Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8; Gen. 2: x4

AMC Interface

Type: AMC.1
Module Management: IPMI Version 2.0

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Ordering Information

Model | Description
--- | ---
56660 | 4-Channel 200 MHz A/D with Virtex-6 FPGA - AMC

Options:

-062 | XC6VLX240T FPGA
-064 | XC6VSX315T FPGA
-104 | LVDS FPGA I/O through front panel connector
-150 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
-160 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
-155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. | One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
Model 71663

1100-Channel GSM Channelizer with Quad A/D - XMC

General Information

Model 71663 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 71663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 71663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

GSM Channelizer Cores

The 71663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

Features

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8

Features
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 71663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 71663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 71663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 71663 and host.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Specifications

Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

DDC Channels
- Channel Spacing: 200 kHz, fixed
- DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- DDC Channel Filter Characteristics
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz

DDC Output Rate $f_s$: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels
- Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:
  - First: -$f_s/4$ (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +$f_s/4$ (+270.8333 kHz)
  - Fourth: +$f_s/2$ (+541.666 kHz)

Superchannel Sample Rate: $f_s$

Superchannel Output Format: 26 bits I + 26 bits Q

Number of Superchannels per Bank:
  - 175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
- PCI Express Bus: Gen. 2 x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - XMC</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
Model 78663 1100-Channel GSM Channelizer with Quad A/D - x8 PCIe

**General Information**

Model 78663 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 78663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**GSM Channelizer Cores**

The 78663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 78663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 78663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz×13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 78663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 78663 and host.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

 Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer
Clock Synthesizer
Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

GSM Channel Banks
DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels
Channel Spacing: 200 kHz, fixed
DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

DDC Channel Filter Characteristics
< 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
> 18 dB attenuation at ±100 kHz
> 78 dB attenuation at ±170 kHz
> 83 dB attenuation at ±600 kHz
> 93 dB attenuation at ±800 kHz
> 96 dB attenuation at > ±3 MHz

DDC Output Rate fs: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

DDC Data Output Format:
24 bits I + 24 bits Q

Superchannels
Content: Four consecutive DDC channels are frequency-offset from each other and then summed together

Frequency Offsets for each DDC:
First: -fs/4 (-270.8333 kHz)
Second: 0 Hz
Third: +fs/4 (+270.8333 kHz)
Fourth: +fs/2 (+541.666 kHz)
Superchannel Sample Rate: fs
Superchannel Output Format:
26 bits I + 26 bits Q

Number of Superchannels per Bank:
175-Channel banks: 44; 375-Channel banks: 94

Field Programmable Gate Array: Xilinx Virtex-6 XC6VSX315T

PCI Express Interface
PCI Express Bus: Gen. 2 x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half length PCIe card, 4.38 x 7.13 in.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78663</td>
<td>1100-Channel GSM Channelizer with Quad A/D PCIe</td>
</tr>
<tr>
<td>8266</td>
<td>PC Development System</td>
</tr>
</tbody>
</table>

See 8266 Datasheet for Options

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 53663

1100-Channel GSM Channelizer with Quad A/D - VPX

**General Information**

Model 53663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 53663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

**GSM Channelizer Cores**

The 53663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

---

**Features**

- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCI Express Gen. 2 x8
- 3U VPX form factor provides a compact, rugged platform
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 53663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 53663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 53663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 53663 and host.

Fabric-Transparent Crossbar Switch

The 53663 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
### Specifications

#### Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors
- **Transformer Type:** Coil Craft WBC4-6TBL
- **Full Scale Input:** +8 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

#### A/D Converters
- **Type:** Texas Instruments ADS5485
- **Sampling Rate:** 10 MHz to 200 MHz
- **Resolution:** 16 bits

#### Sample Clock Sources
- **Type:** On-board clock synthesizer

#### Clock Synthesizer
- **Clock Source:** Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 10 MHz system reference

#### Timing Bus
- **Type:** 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

#### External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL

#### GSM Channel Banks
- **DDCs per bank:** two banks of 175 DDCs and two banks of 375 DDCs
- **Overall bandwidth per bank:** 35 MHz & 75 MHz for 175- & 375-channel banks
- **IF (Center) Freq:** 45, 135 or 225 MHz

#### DDC Channels
- **Channel Spacing:** 200 kHz, fixed
- **DDC Center Freqs:** IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
- **DDC Channel Filter Characteristics:**
  - < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
  - > 18 dB attenuation at ±100 kHz
  - > 78 dB attenuation at ±170 kHz
  - > 83 dB attenuation at ±600 kHz
  - > 93 dB attenuation at ±800 KHz
  - > 96 dB attenuation at > ±3 MHz
- **DDC Output Rate ƒs:** Resampled to 180 MHz/13/2160 = 1.0833333 MS/sec
- **DDC Data Output Format:** 24 bits I + 24 bits Q

### Superchannels
- **Content:** Four consecutive DDC channels are frequency-offset from each other and then summed together
- **Frequency Offsets for each DDC:**
  - First: -ƒs/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +ƒs/4 (+270.8333 kHz)
  - Fourth: +ƒs/2 (+541.666 kHz)
- **Superchannel Sample Rate:** ƒs
- **Superchannel Output Format:** 26 bits I + 26 bits Q

#### Number of Superchannels per Bank
- 175-Channel banks: 44; 375-Channel banks: 94

### Field Programmable Gate Array
- **Xilinx Virtex-6 XC6VSX315T**

### PCI Express Interface
- **PCI Express Bus:** Gen. 2 x8

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

---

### Ordering Information

<table>
<thead>
<tr>
<th>Model 53663</th>
<th>1100-Channel GSM Channelizer with Quad A/D - VPX</th>
</tr>
</thead>
</table>

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
<thead>
<tr>
<th>Model 8267</th>
<th>VPX Development System. See 8267 Datasheet for Options</th>
</tr>
</thead>
</table>

---

**SPARK Development Systems**

---

**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
<td>x4</td>
<td>x4 or x8</td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
Model 52663

1100-Channel GSM Channelizer with Quad A/D - VPX

General Information
Model 52663 is a member of the Cobalt® family of high-performance VPX boards based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 2 GB/sec.

The Cobalt Architecture
The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four DMA controllers, PCIe interface, gating, and triggering.

The 52663 is a complete, full-featured subsystem, ready to use with no additional FPGA development required.

A/D Converter Stage
The front end accepts four analog IF inputs on front panel SSMC connectors with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization
An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 52663s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

GSM Channelizer Cores
The 52663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.

---

Model 52663 Commercial (left) and rugged version

Features
- Complete GSM channelizer with analog IF interface
- Four 180 MHz 16-bit A/Ds
- Two banks of 375 DDCs for upper GSM band
- Two banks of 175 DDCs for lower GSM band
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- PCIe Express Gen. 2 x4
- 3U VPX form factor provides a compact, rugged platform

---
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 52663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 52663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

The Model 52663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x4, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 52663 and host.
Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: Coil Craft WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz

A/D Converters
  Type: Texas Instruments ADS5485
  Sampling Rate: 10 MHz to 200 MHz
  Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
  Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
  Synchronization: VCXO can be locked to an external 10 MHz system reference

External Clock
  Type: Front panel female SSMC connector, sine wave
  Function: Programmable functions include: trigger, gate, sync and PPS inputs

GSM Channel Banks

  DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
  Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
  IF (Center) Freq: 45, 135 or 225 MHz

DDC Channels

  Channel Spacing: 200 kHz, fixed
  DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
  DDC Channel Filter Characteristics:
    - < 0 dB passband flatness across ±80 kHz from center (160 kHz BW)
    - > 18 dB attenuation at ±100 kHz
    - > 78 dB attenuation at ±170 kHz
    - > 83 dB attenuation at ±600 kHz
    - > 93 dB attenuation at ±800 kHz
    - > 96 dB attenuation at ±1 MHz
  DDC Output Rate f_s: Resampled to 180 MHz/13/2160 = 1.0833333 MS/sec
  DDC Data Output Format: 24 bits I + 24 bits Q

Superchannels

  Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
  Frequency Offsets for each DDC:
    - First: -f_s/4 (-270.8333 kHz)
    - Second: 0 Hz
    - Third: +f_s/4 (+270.8333 kHz)
    - Fourth: +f_s/2 (+541.666 kHz)
  Superchannel Sample Rate: f_s
  Superchannel Output Format: 26 bits I + 26 bits Q

Environmental

  Operating Temp: 0° to 50° C
  Storage Temp: −20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.
  Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe path</td>
<td>x4</td>
<td>x4 or x8</td>
</tr>
<tr>
<td>PCIe width</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - 6U OpenVPX

General Information

Models 57663 and 58663 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a VPX carrier board.

Model 57663 is a 6U board with one Model 71663 module while the Model 58663 is a 6U board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

The Cobalt Architecture

The Pentek Cobalt architecture connects all of the board’s data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

A/D Converter Stage

The front end accepts four or eight analog IF inputs on front panel SSMC connectors with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

Clocking and Synchronization

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards. Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.
GSM Channelizer Cores

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz/13/2160, or approximately 1.083333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.083333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

The PCIe interface is also used as the programming interface for all status and control between these models and host.
**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Specifications**

Model 57663: 4 A/Ds, 1100 Channels  
Model 58663: 8 A/Ds, 2200 Channels

**Front Panel Analog Signal Inputs (4 or 8)**

- **Input Type**: Transformer-coupled, front panel female SSMC connectors  
- **Transformer Type**: Coil Craft WBC4-6TLB  
- **Full Scale Input**: +8 dBm into 50 ohms  
- **3 dB Passband**: 300 kHz to 700 MHz

**A/D Converters (4 or 8)**

- **Type**: Texas Instruments ADS5485  
- **Sampling Rate**: 10 MHz to 200 MHz  
- **Resolution**: 16 bits

**Sample Clock Sources (1 or 2)**

- **On-board clock synthesizer**

**Clock Synthesizers (1 or 2)**

- **Clock Source**: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus  
- **Synchronization**: VCXO can be locked to an external 10 MHz system reference

**External Clocks (1 or 2)**

- **Type**: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference

**Timing Bus (1 or 2)**

- 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Inputs (1 or 2)**

- **Type**: Front panel female SSMC connector, LVTTL

**Function**: Programmable functions include: trigger, gate, sync and PPS

**GSM Channel Banks (1 or 2)**

- **DDCs per bank**: two banks of 175 DDCs and two banks of 375 DDCs  
- **Overall bandwidth per bank**: 35 MHz & 75 MHz for 175- & 375-channel banks  
- **IF (Center) Freq**: 45, 135 or 225 MHz  
- **DDC Channels**: Channel Spacing: 200 kHz, fixed  
- **DDC Center Freq**: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187

**DDC Channel Filter Characteristics**

- < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)  
- > 18 dB attenuation at ±100 kHz  
- > 78 dB attenuation at ±170 kHz  
- > 83 dB attenuation at ±600 kHz  
- > 93 dB attenuation at ±800 kHz  
- > 96 dB attenuation at > ±3 MHz

**DDC Output Rate f_s**: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec

**DDC Data Output Format**: 24 bits I + 24 bits Q

**Superchannels**

- **Content**: Four consecutive DDC channels are frequency-offset from each other and then summed together

**Frequency Offsets for each DDC**

- First: -f_s/4 (-270.8333 kHz)  
- Second: 0 Hz  
- Third: +f_s/4 (+270.8333 kHz)  
- Fourth: +f_s/2 (+541.666 kHz)

**Superchannel Sample Rate**: f_s

**Superchannel Output Format**: 26 bits I + 26 bits Q

**Number of Superchannels per Bank**

- 175-Channel banks: 44; 375-Channel banks: 94

**Field Programmable Gate Arrays (1 or 2)**

- Xilinx Virtex-6 XC6VSX315T

**PCI-Express Interface**

- PCI Express Bus: Gen. 1 or 2; x4

**Environmental**

- Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

**Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 6U VPX</td>
</tr>
<tr>
<td>58663</td>
<td>2200-Channel GSM Channelizer with Octal A/D - 6U VPX</td>
</tr>
</tbody>
</table>

---

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8264</td>
<td>VPX Development System. See 8264 Datasheet for Options</td>
</tr>
</tbody>
</table>
**Models 72663, 73663 and 74663**

1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

**General Information**

Models 72663, 73663 and 74663 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71663 XMC modules mounted on a cPCI carrier board.

Model 72663 is a 6U cPCI board while the Model 73663 is a 3U cPCI board; both are equipped with one Model 71663 XMC. Model 74663 is a 6U cPCI board with two XMC modules rather than one.

This quad or octal, high-speed A/D converter with 1100 or 2200 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

**The Cobalt Architecture**

The Pentek Cobalt architecture connects all of the board's data converters, digital interfaces, clocks and timing signals to the FPGA. Here, four or eight factory-installed GSM channelizer IP cores are supported with additional FPGA functions including packet formation, four or eight DMA controllers, PCIe interface, gating, and triggering.

These models are complete, full-featured subsystems, ready to use with no additional FPGA development required.

**A/D Converter Stage**

The front end accepts four or eight analog IF inputs on front panel SSMC connectors and lower GSM bands.

Texas Instruments ADS5485 200 MHz, 16-bit A/D converters clocked at 180 MHz.

The digital outputs are delivered into the FPGA for GSM channelizer signal processing.

**Clocking and Synchronization**

The internal timing bus provides all timing and synchronization required by the A/D converters. It includes clock, sync and gate or trigger signals. One or two on-board clock generators accept external 180 MHz sample clocks from the front panel SSMC connectors. The clocks can be used directly by the A/Ds or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. ➤
1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

**GSM Channelizer Cores**

These models contain four or eight powerful GSM channelizer cores, two or four with 375 DDCs and two or four with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of four GSM channelizers.

The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to these models, the GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the four or eight A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must insure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

**Channelizer Output Formatting**

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x over sampling, and results in a reduction of the aggregate traffic by a factor of 4 to 2.383 GB/sec.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bits I + 26-bits Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank only contains three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCI-X bus. There are four superchannel mask words, one for each bank.

**Superchannel Packets and Headers**

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

**PCI-X Interface**

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73663: 32 bits only.

The PCI-X interface is also used as the programming interface for all status and control between these models and host.
1100- or 2200-Channel GSM Channelizer with Quad or Octal A/D - cPCI

Specifications
Model 72663 or Model 73663: 4 A/Ds
Model 74663: 8 A/Ds
Front Panel Analog Signal Inputs (4 or 8)
  Input Type: Transformer-coupled, front panel female SSMC connectors
  Transformer Type: Coil Craft
  WBC4-6TLB
  Full Scale Input: +8 dBm into 50 ohms
  3 dB Passband: 300 kHz to 700 MHz
A/D Converters (4 or 8)
  Type: Texas Instruments ADS5485
  Sampling Rate: 10 MHz to 200 MHz
  Resolution: 16 bits
Sample Clock Sources (1 or 2)
  On-board clock synthesizer
Clock Synthesizers (1 or 2)
  Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
  Synchronization: VCXO can be locked to an external 10 MHz system reference
External Clocks (1 or 2)
  Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
Timing Bus (1 or 2): 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Inputs (1 or 2)
  Type: Front panel female SSMC connector, LVTTL
  Function: Programmable functions include: trigger, gate, sync and PPS
GSM Channel Banks (1 or 2)
  DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
  Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
  IF (Center) Freq: 45, 135 or 225 MHz
DDC Channels
  Channel Spacing: 200 kHz, fixed
  DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187
  DDC Channel Filter Characteristics
    < 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)
    > 18 dB attenuation at ±100 kHz
    > 78 dB attenuation at ±170 kHz
    > 83 dB attenuation at ±600 kHz
    > 93 dB attenuation at ±800 KHz
    > 96 dB attenuation at > ±3 MHz
  DDC Output Rate $f_s$: Resampled to 180 MHz*13/2160 = 1.083333 MS/sec
  DDC Data Output Format: 24 bits I + 24 bits Q
Superchannels
  Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
  Frequency Offsets for each DDC:
    First: $-f_s/4$ (-270.8333 kHz)
    Second: 0 Hz
    Third: $+f_s/4$ (+270.8333 kHz)
    Fourth: $+f_s/2$ (+541.666 kHz)
  Superchannel Sample Rate: $f_s$
  Superchannel Output Format: 26 bits I + 26 bits Q
  Number of Superchannels per Bank:
    175-Channel banks: 44; 375-Channel banks: 94
Field Programmable Gate Arrays (1 or 2)
  Xilinx Virtex-6 XC6VSX315T
PCI-X Interface
  PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
  Model 73663: 32 bits only
Environmental
  Operating Temp: 0° to 50° C
  Storage Temp: -20° to 90° C
  Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 6U cPCI</td>
</tr>
<tr>
<td>73663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - 3U cPCI</td>
</tr>
<tr>
<td>74663</td>
<td>2200-Channel GSM Channelizer with Octal A/D - 6U cPCI</td>
</tr>
</tbody>
</table>
General Information

Model 56663 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This four-channel, high-speed A/D converter with 1100 GSM DDCs (digital downconverters) accepts IF signals from an RF tuner. It is ideal for capturing all transmit and receive signals in both upper and lower GSM bands.

It includes four A/Ds and four banks of DDCs. Channelizer data and control signals flow across the PCI Express Gen. 2 native interface, providing peak rates of up to 4 GB/sec.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator accepts an external 180 MHz sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board 180 MHz voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a reference clock, typically 10 MHz, for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56663’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

GSM Channelizer Cores

The 56663 contains four powerful GSM channelizer cores, two with 375 DDCs and two with 175 DDCs. Flexible input routing allows the independent, non-blocking assignment of any A/D converter to serve as the input source for any of the four GSM channelizers.
The 375-channel cores are designed for the upper GSM bands which contain two 75 MHz bands, one for uplink and one for downlink. The 175-channel cores are designed for the lower GSM band and handle two 35 MHz bands, one for uplink and one for downlink.

Before connection to the 56663, these GSM RF bands must first be separately downconverted to an IF frequency centered at 45 MHz, 135 MHz or 225 MHz using an external analog RF tuner.

These IF signals are then digitized by the 56663 A/Ds at 180 MS/sec in the first, second, or third Nyquist zones, respectively. In order to prevent aliasing, careful filtering must ensure that no signals appear in adjacent Nyquist zones.

Each of the channelizers is designed to accept real digital samples of the IF signal from the A/D converter. The first stage of the GSM channelizer is a complex mixer that shifts the center frequency of the IF signal (45, 135 or 225 MHz) to 0 Hz, thereby producing complex I+Q samples.

The DDCs split the IF input into either 175 or 375 parallel DDC baseband channels, equally spaced at 200 kHz. The DDC output sample rate is resampled to precisely 180 MHz*13/2160, or approximately 1.08333 MHz. This is four times the GSM symbol rate of 270.666 kSymbols/sec. The output passband of each DDC channel is nominally 160 kHz, with filter characteristics fully defined in the channel response chart in the specifications.

### Channelizer Output Formatting

All 1100 DDCs generate parallel, complex output sample streams. At a sample rate of 1.08333 MS/sec, this represents an aggregate output rate of 9.533 GB/sec, greatly exceeding the 4 GB/sec peak rate of PCIe Gen 2 x8 interface.

To mitigate this situation, every four DDC channels are frequency-multiplexed into a single “superchannel”. This is allowed because of the 4x oversampling, and results in a reduction of the aggregate PCIe traffic by a factor of 4 to 2.383 GB/sec, which is now well within the capability of the PCIe Gen 2 x8 interface.

During superchannel formation, the 24-bit I + 24-bit Q output samples from four DDCs are summed to superchannel samples with 26-bit I + 26-bit Q.

As a result, the two 375-channel banks each deliver 94 superchannels, while the two 175-channel banks each deliver 44 superchannels. The last superchannel in each bank contains only three DDC channels.

A superchannel enable mask word containing one enable bit for each superchannel allows independent selection of which superchannel samples are delivered across the PCIe. There are four superchannel mask words, one for each bank.

### Superchannel Packets and Headers

Superchannel packets are formed by appending enabled superchannel samples sequentially from each bank. Once complete, a unique superchannel packet header is inserted at the beginning of each packet for identification.

The header contains a time stamp, a sequential packet count, the number of enabled superchannels, the DMA channel identifier, and other information. By inspecting the header, the remaining superchannel data “payload” samples can be identified and recovered by the host.

### PCI Express Interface

The Model 56663 includes an industry-standard interface fully compliant with PCI Express Gen. 2 bus specifications. Supporting PCIe links up to x8, the interface includes four DMA controllers for efficient packet transfers from each of the four DDC banks to system memory.

The PCIe interface is also used as the programming interface for all status and control between the 56663 and host.

### AMC Interface

The Model 56663 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
### Specifications

**Front Panel Analog Signal Inputs**
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

**A/D Converters**
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

**Sample Clock Sources:** On-board clock synthesizer

**Clock Synthesizer**
- Clock Source: Selectable from on-board 180 MHz VCXO, front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 10 MHz system reference

**External Clock**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, 50 ohms, AC-coupled, accepts 180 MHz sample clock or 10 MHz system reference
- Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**GSM Channel Banks**
- DDCs per bank: two banks of 175 DDCs and two banks of 375 DDCs
- Overall bandwidth per bank: 35 MHz & 75 MHz for 175- & 375-channel banks
- IF (Center) Freq: 45, 135 or 225 MHz

<table>
<thead>
<tr>
<th>DDC Channels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Spacing: 200 kHz, fixed</td>
</tr>
<tr>
<td>DDC Center Freqs: IF Freq ± k * 200 kHz, where k = 0 to 87, or 0 to 187</td>
</tr>
<tr>
<td>DDC Channel Filter Characteristics</td>
</tr>
<tr>
<td>&lt; 0.1 dB passband flatness across ±80 kHz from center (160 kHz BW)</td>
</tr>
<tr>
<td>&gt; 18 dB attenuation at ±100 kHz</td>
</tr>
<tr>
<td>&gt; 78 dB attenuation at ±170 kHz</td>
</tr>
<tr>
<td>&gt; 83 dB attenuation at ±600 kHz</td>
</tr>
<tr>
<td>&gt; 93 dB attenuation at ±800 kHz</td>
</tr>
<tr>
<td>&gt; 96 dB attenuation at &gt; ±3 MHz</td>
</tr>
<tr>
<td>DDC Output Rate f_s: Resampled to 180 MHz*13/2160 = 1.0833333 MS/sec</td>
</tr>
<tr>
<td>DDC Data Output Format: 24 bits I + 24 bits Q</td>
</tr>
</tbody>
</table>

**Superchannels**
- Content: Four consecutive DDC channels are frequency-offset from each other and then summed together
- Frequency Offsets for each DDC:
  - First: -f_s/4 (-270.8333 kHz)
  - Second: 0 Hz
  - Third: +f_s/4 (+270.8333 kHz)
  - Fourth: +f_s/2 (+541.666 kHz)
- Superchannel Sample Rate: f_s
- Superchannel Output Format: 26 bits I + 26 bits Q
- Number of Superchannels per Bank:
  - 175-Channel banks: 44; 375-Channel banks: 94

**Field Programmable Gate Array:** Xilinx Virtex-6 XC6VSX315T

**PCI Express Interface**
- PCI Express Bus: Gen. 2 x8

**AMC Interface**
- Type: AMC.1
- Module Management: IPMI Version 2.0

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>56663</td>
<td>1100-Channel GSM Channelizer with Quad A/D - AMC</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.
Model 71670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC

General Information

Model 71670 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/A’s, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SX7 part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/A’s
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

D/A Waveform Playback IP Module

The Model 71670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7192 or 9192 Cobalt Synchronizers can drive multiple 71670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 71670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface

The Model 71670 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to a 3.125 GHz bit clock. With dual XMC connectors, the 71670 supports 8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

D/A Converters
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs
Quantity: Four D/A outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

Ordering Information

Model Description
71670 4-Channel 1.25 GHz D/A with Virtex-6 FPGA - XMC

Options:
-002* -2 FPGA speed grade
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus: 19-pin μSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as two 4X or one 8X gigabit serial links to the FPGA

Memory: Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen 2: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 78670 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78670 includes optional general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

The Pentek Cobalt Architecture includes an intellectual property (IP) module. The Cobalt Architecture organizes the FPGA as a container for data processing control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - x8 PCIe

**Digital Upconverter and D/A Stage**

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

**Clocking and Synchronization**

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator).

In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7892 or 9192 Cobalt Synchronizers can drive multiple 78670 µSync connectors enabling large, multi-channel synchronous configurations.

**Memory Resources**

The 78670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 78670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.

---

**D/A Waveform Playback IP Module**

The Model 78670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/A devices from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
**Specifications**

**D/A Converters**
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max.
- **with interpolation**
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**
- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:**
  - 10 to 945 MHz
  - 970 to 1134 MHz
  - 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clock**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Input**
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus:**
- 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**Field Programmable Gate Array**
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O**
- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

**Environmental**
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Half length PCIe card, 4.38 in. x 7.13 in.

---

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- -02* -2 FPGA speed grade
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS FPGA I/O through 68-pin ribbon cable connector
- -105 Gigabit serial FPGA I/O through two 4X top edge connectors
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

---

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

General Information

Model 53670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmission applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 53670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SX part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5392 or 9192 Cobalt Synchronizers can drive multiple 53670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 53670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 53670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the board.
# Model 53670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

- **Fabric-Transparent Crossbar Switch**
  The 53670 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

## Specifications

**D/A Converters**
- Type: TI DAC3484
- Input Data Rate: 312.5 MHz max.
- Output Bandwidth: 250 MHz max.
- Output Sampling Rate: 1.25 GHz max. with interpolation
- Interpolation: 2x, 4x, 8x or 16x
- Resolution: 16 bits

**Front Panel Analog Signal Outputs**
- Quantity: Four D/A outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Full Scale Output: Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- Full Scale Output Programming: \( 1.0x(G+1)/16 \) Vp-p, where 4-bit integer \( G = 0 \) to 15

**Clock Synthesizer**
- Clock Source: Selectable from on-board programmable VCXO or front panel external clock
- VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clock**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Input**
- Type: Front panel female SSMC connector
- Function: Programmable functions include: trigger, gate, sync and PPS

**Timing Bus**
- 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

## Field Programmable Gate Array

- **Standard**: Xilinx Virtex-6 XC6VLX130T-2
- **Optional**: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

## Custom I/O

- **Option -104**: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105**: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

**Memory**
- Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

## PCI-Express Interface

- **PCI Express Bus**: Gen. 1 or Gen 2: x4 or x8

## Environmental

- **Operating Temp**: 0° to 50° C
- **Storage Temp**: –20° to 90° C
- **Relative Humidity**: 0 to 95%, non-cond.
- **Size**: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

## VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Form Factor</strong></td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
</tr>
<tr>
<td><strong>PCIe path</strong></td>
</tr>
<tr>
<td><strong>PCIe width</strong></td>
</tr>
<tr>
<td><strong>Option -104 path</strong></td>
</tr>
<tr>
<td><strong>Option -105 path</strong></td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
</tr>
</tbody>
</table>

---

**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- -002*: -2 FPGA speed grade
- -062: XC6VLX240T FPGA
- -064: XC6VSX315T FPGA
- -104: LVDS FPGA I/O to VPX P2
- -105: Gigabit serial FPGA I/O to VPX P1
- -155*: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165*: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

---

**Contact Pentek for availability of rugged and conduction-cooled versions**

---

**Model 8267**

The Model 8267 VPX Development System. See 8267 Datasheet for Options.
Model 52670

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

General Information
Model 52670 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 over the 3U VPX backplane, the Model 52670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features
- Complete radar and software radio interface solution
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four 1.25 GHz 16-bit D/As
- Four digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- User-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX

➤ Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 592 or 9192 Cobalt Synchronizers can drive multiple 52670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 52670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 52670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x4 lane interface includes multiple DMA controllers for efficient transfers to and from the board. ➤

D/A Waveform Playback IP Module

The Model 52670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Data for Channel 1 and Channel 2 are interleaved for delivery to a dual channel D/A device. For this reason, they must share a common trigger/gate, sample rate, interpolation factor, and other parameters. The same rules apply to Channel 3 and Channel 4. Parameters including length of waveform, waveform repetition, etc. can be programmed for each channel.

Up to 64 individual link entries for each D/A channel can be chained together to create complex waveforms with a minimum of programming.
Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

D/A Converters
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Quantity:** Four D/A outputs
- **Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS
- **Timing Bus:** 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- **Type:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
**General Information**

Models 57670 and 58670 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a VPX carrier board.

Model 57670 is a 6U board with one Model 71670 module while the Model 58670 is a 6U board with two XMC modules rather than one.

These models include four or eight D/As, four or eight DUCs, and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670.

Option -105 supports serial protocols by providing a 4x gigabit link between the FPGA and VPX P2, Model 57670; one 4x link from each FPGA to P2 and an additional 4x link between the FPGAs, Model 58670.

---

**Features**

- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Four or eight 1.25 GHz 16-bit D/As
- Four or eight digital upconverters
- Programmable output levels
- 250 MHz max. output bandwidth
- 2 or 4 GB of DDR3 SDRAM
- PCIe Express (Gen. 1 & 2) interface up to x8
- Sample clock synchronization to an external system reference
- Dual-or Quad µSync clock/ sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
➤ Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four or eight front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Model 9192 Cobalt Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked-list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board. ➤
# Specifications

**Model 57670:** 4-Channel DUC, 4-channel D/A

**Model 58670:** 8-Channel DUC, 8-channel D/A

**D/A Converters (4 or 8):**
- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x, or 16x
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs (4 or 8):**
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** \(1.0x(G+1)/16\) Vp-p, where 4-bit integer \(G = 0\) to \(15\)

**Clock Synthesizers (1 or 2):**
- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

**External Clocks (1 or 2):**
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

**External Trigger Inputs (1 or 2):**
- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus (1 or 2):** 19-pin \(\mu\)Sync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

**Field Programmable Gate Arrays (1 or 2):**
- **Standard:** Xilinx Virtex-6 XC6VLX130T-2
- **Optional:** Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

**Custom I/O:**
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57670; P3 and P5, Model 58670
- **Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57670; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58670

**Memory Banks (1 or 2):**
- Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface:**
- **PCI Express Bus:** Gen. 1 or 2: x4 or x8

**Environmental:**
- **Level L1 & L2 air-cooled:**
- **Level L3 ruggedized, conduction-cooled:**
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**General Information**

Models 72670, 73670 and 74670 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71670 XMC modules mounted on a cPCI carrier board.

Model 72670 is a 6U cPCI board while the Model 73670 is a 3U cPCI board; both are equipped with one Model 71670 XMC. Model 74670 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight D/As, four or eight DUCs, and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include four or eight D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670.
Digital Upconverter and D/A Stage

Two or four Texas Instruments DAC3484s provide four or eight DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel μSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 7292, 7392 and 7492 or the 9192 Cobalt Synchronizers can drive multiple μSync connectors enabling large, multichannel synchronous configurations.

Memory Resources

The architecture of these models supports four or eight independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the board’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73670: 32 bits only.
4- or 8-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - cPCI

Specifications

Models 72670 and 73670: 4-Channel DUC, 4-channel D/A
Model 74670: 8-Channel DUC, 4-channel D/A

D/A Converters (4 or 8)
Type: TI DAC3484
Input Data Rate: 312.5 MHz max.
Output Bandwidth: 250 MHz max.
Output Sampling Rate: 1.25 GHz max. with interpolation
Interpolation: 2x, 4x, 8x or 16x
Resolution: 16 bits

Front Panel Analog Signal Outputs (4 or 8)
Output Type: Transformer-coupled, front panel female SSMC connectors
Full Scale Output: Programmable from -20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
Full Scale Output Programming: 1.0x(G+1)/16 Vp-p, where 4-bit integer G = 0 to 15

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS

Timing Bus (1 or 2): 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T-2
Optional: Xilinx Virtex-6 XC6VLX240T-2 or XC6VSX315T-2

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670

Memory Banks (1 or 2)
Four or eight 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73670: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74670</td>
<td>8-Channel 1.25 GHz D/A with Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:
- -002* -2 FPGA speed grade
- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -104 LVDS I/O between the FPGA and J2 connector, Model 73670; J3 connector, Model 72670; J3 and J5 connectors, Model 74670
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165* Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required
General Information

Model 56670 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56670 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

---

**Pentek, Inc.**  One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201 818-5904 • Email: info@pentek.com

www.pentek.com
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

Digital Upconverter and D/A Stage

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x. Analog output is through four front panel SSMC connectors.

Clocking and Synchronization

An internal timing bus provides all required D/A clocking. The bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided by 2, 4, 8, or 16 to provide lower frequency D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and trigger/gate signals. The Pentek Models 5692 or 9192 Cobalt Synchronizers can drive multiple 56670 µSync connectors enabling large, multi-channel synchronous configurations.

Memory Resources

The 56670 architecture supports four independent memory banks of DDR3 SDRAM. Each bank is 512 MB deep and is an integral part of the module’s DMA and waveform playback capabilities. Waveform tables can be loaded into the memories with playback managed by the linked list controllers.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56670 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).
4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - AMC

➤ PCI Express Interface

The Model 56670 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. The x8 lane interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

D/A Converters

- **Type:** TI DAC3484
- **Input Data Rate:** 312.5 MHz max.
- **Output Bandwidth:** 250 MHz max.
- **Output Sampling Rate:** 1.25 GHz max. with interpolation
- **Interpolation:** 2x, 4x, 8x or 16x
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

- **Quantity:** Four D/A outputs
- **Output Type:** Transformer-coupled, front panel female SSMC connectors
- **Full Scale Output:** Programmable from –20 dBm (0.063 Vp-p) to +4 dBm (1.0 Vp-p) in 16 steps
- **Full Scale Output Programming:** \(1.0x(G+1)/16\) Vp-p, where 4-bit integer \(G = 0\) to 15

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO or front panel external clock
- **VCXO Frequency Ranges:** 10 to 945 MHz, 970 to 1134 MHz and 1213 to 1417 MHz
- **Synchronization:** VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the D/A clock

External Clock

- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 500 MHz sample clock or 5 or 10 MHz system reference

External Trigger Input

- **Type:** Front panel female SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Timing Bus

- **Type:** 19-pin µSync bus connector includes, clock, reset and gate/trigger inputs and outputs, CML

Field Programmable Gate Array

- **Standard:** Xilinx Virtex-6
  - XC6VLX130T-2
- **Optional:** Xilinx Virtex-6
  - XC6VLX240T-2 or XC6VSX315T-2

Custom I/O

- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory

- **Type:** Four 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface

- **PCI Express Bus:** Gen. 1 or Gen 2: x4 or x8;

AMC Interface

- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

Environmental

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size

- **Single-width, full-height AMC module, 2.89 in. x 7.11 in.**

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>56670</td>
<td>4-Channel 1.25 GHz D/A with Virtex-6 FPGA - AMC</td>
</tr>
</tbody>
</table>

Options:

- **-002** -2 FPGA speed grade
- **-062** XC6VLX240T FPGA
- **-064** XC6VSX315T FPGA
- **-104** LVDS FPGA I/O through front panel connector
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* These options are always required

Contact Pentek for availability of rugged and conduction-cooled versions
Model 71690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - XMC

General Information
Model 71690 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71690 includes general purpose and gigabit serial connectors for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

Features
- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds digitize the I + Q signals synchronously
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multichannel synchronization
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
RF Tuner Stage
A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

A/D Converter Stage
The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization
An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources
The 71690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 8266**

The Model 8266 is a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>062</td>
<td>XC6VLX240T FPGA</td>
</tr>
<tr>
<td>064</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>010</td>
<td>LVDS FPGA I/O through P14 connector</td>
</tr>
<tr>
<td>015</td>
<td>Gigabit serial FPGA I/O through P16 connector</td>
</tr>
<tr>
<td>050</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>051</td>
<td>Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)</td>
</tr>
<tr>
<td>155</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>156</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

### Specifications

- **A/D Converters**
  - Type: Texas Instruments AD55485
  - Sampling Rate: 10 MHz to 200 MHz
  - Resolution: 16 bits

- **Sample Clock Sources**
  - On-board timing generator/synthesizer

- **A/D Clock Synthesizer**
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

- **Timing Generator External Clock Input**
  - Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

- **Timing Generator Bus**
  - 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

- **External Trigger Input**
  - Quantity: 2
  - Type: Front panel female SSMC connector, LVTTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

- **Field Programmable Gate Array**
  - Standard: Xilinx Virtex-6 XC6VLX130T
  - Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

- **Custom I/O**
  - Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
  - Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

- **Memory**
  - Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
  - Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

- **PCI-Express Interface**
  - PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4

- **Environmental**
  - Operating Temp: 0° to 50°C
  - Storage Temp: -20° to 90°C
  - Relative Humidity: 0 to 95%, non-cond.
  - Size: Standard XMC module, 2.91 in. x 5.87 in.
General Information

Model 78690 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78690 includes optional general-purpose and gigabit serial connectors for application-specific I/O protocols.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1 & 2) interface, up to x8
- Clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

A/D Acquisition IP Modules

The 78690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - PCIe</td>
</tr>
</tbody>
</table>

**Options:**
- -062  XC6VLX240T FPGA
- -064  XC6VSX315T FPGA
- -104  LVDS FPGA I/O through 68-pin ribbon cable connector
- -105  Gigabit serial FPGA I/O through two 4X top edge connectors
- -150  Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- -160  Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- -155  Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

### Model 78690

L-Band RF Tuner, 2-Channel 200 MHz A/D, Virtex-6 FPGA - x8 PCIe

- Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface
The Model 78690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Specifications

**Front Panel Analog Signal Input**
- Connector: Front panel female SSMC
- Impedance: 50 ohms

**L-Band Tuner**
- Type: Maxim MAX2112
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer:
  - freq\_VCO = (N.F) x freq\_REF
  - where integer N = 19 to 251 and fractional F is a 20-bit binary value
- PLL Reference (freq\_REF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100, 12 to 30 MHz
- LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
- Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
- *Usable Full-Input Range: -50 dBm to +10 dBm
- Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

**A/D Converters**
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

**Sample Clock Sources:** On-board timing generator/synthesizer
**A/D Clock Synthesizer**
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Timing Generator External Clock Input**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus:** 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- Quantity: 2
- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Custom I/O**
- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.
General Information

Model 53690 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 53690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). An Analog Devices MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**

The analog baseband I and Q analog tuner outputs are then applied to Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**A/D Clocking and Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

**Memory Resources**

The 53690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory. Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep.

---

**A/D Acquisition IP Modules**

The 53690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode.

All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
PCI Express Interface

The Model 53690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testifying a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model | Description
--- | ---
53690 | L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX

Options:
- 062 | XC6VLX240T FPGA
- 064 | XC6VSX315T FPGA
- 104 | LVDS FPGA I/O to VPX P1
- 105 | Gigabit serial FPGA I/O to VPX P2
- 150 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- 154 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 164 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 153 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 163 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- 104 | LVDS FPGA I/O to VPX P1
- 105 | Gigabit serial FPGA I/O to VPX P2
- 150 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 | Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms
L-Band Tuner
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
freq\(_{\text{VCO}}\) = (N.F) x freq\(_{\text{REF}}\)
where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference (freq\(_{\text{REF}}\)): Front panel SSMC connector or on-board 27 MHz crystal
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps
*Usable Full-Scale Input Range: -50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources: On-board timing generator/synthesizer
A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock
Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference
Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs
External Trigger Input
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T
Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector for serial protocols
Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4
Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>
General Information

Model 52690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The Model 52690 includes an L-Band RF tuner, two A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides dual 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
RF Tuner Stage

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 52690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

A/D Acquisition IP Modules

The 52690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
PCI Express Interface
The Model 52690 includes an industry standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Input
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuner
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
\[ f_{\text{VCO}} = (N \cdot f_\text{REF}) \]
where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference: Front panel SSMC connector or on-board 27 MHz crystal
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
*Usable Full-Scale Input Range: –50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

A/D Converters
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits
Sample Clock Sources: On-board timing generator/synthesizer

A/D Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 80 MHz), front panel external clock or LVPECL
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Input
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
Quantity: 2
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VX315T

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - 6U OpenVPX

**General Information**

Models 57690 and 58690 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a VPX carrier board.

Model 57690 is a 6U board with one Model 71690 module while the Model 58690 is a 6U board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57690; P3 and P5, Model 58690.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57690; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58690.

---

**Features**

- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or, 32 MB or 64 MB of QDRII+ SRAM
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
RF Tuner Stages

One or two front panel SSMC connectors accept L-Band signals between 925 MHz and 2175 MHz from the antenna LNBS (low noise blocks). The Maxim MAX2112 tuners directly convert these L-Band signals to baseband using broadband I/Q downconverters.

The devices include RF variable-gain LNAs (low noise amplifiers), PLL (phase-locked loops) synthesized local oscillators, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizers lock their VCOs to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNAs offer a programmable linear gain range of 60 dB.

The integrated lowpass filters with variable bandwidths provide bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

A/D Converter Stages

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGAs for signal processing, data capture or for routing to other board resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Options:**
- 58690 Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX
- 57690 L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58690</td>
<td>Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Specifications**

- **L-Band Tuners (1 or 2)**
  - Type: Maxim MAX2112
  - Input Frequency Range: 925 MHz to 2175 MHz
  - Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
  - Fractional-N PLL Synthesizer: freqVCO = (N.F) x freqREF where integer N = 19 to 251 and fractional F is a 20-bit binary value

- **Field Programmable Gate Arrays (1 or 2)**
  - Type: Xilinx Virtex-6 XC6VLX130T
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

- **CPU Interface**
  - Type: Pentek Inc.
  - Frequency programmable from 4 to 40 MHz with 8-bit resolution

- **Device Clock Sources (1 or 2)**
  - On-board timing generator/synthesizer
  - A/D Clock Synthesizers (1 or 2)
  - Clock Source: Selectable from an on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Sample Clock Sources (1 or 2)**

- On-board timing generator/synthesizer
- A/D Clock Synthesizers (1 or 2)
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

**Timing Generator External Clock Inputs (1 or 2)**

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**External Trigger Inputs (2 or 4)**

- Type: Front panel female SSMC connector, LVTTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Arrays (1 or 2)**

- Type: Xilinx Virtex-6 XC6VLX130T
- Standard: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

**Contact Pentek for availability of rugged and conduction-cooled versions**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8264</td>
<td>VPX Development System. See 8264 Datasheet for Options</td>
</tr>
</tbody>
</table>
One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

General Information
Models 72690, 73690 and 74690 are members of the Cobalt® family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71690 XMC modules mounted on a cPCI carrier board.

Model 72690 is a 6U cPCI board while the Model 73690 is a 3U cPCI board; both are equipped with one Model 71690 XMC. Model 74690 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two L-Band RF tuners, two or four A/Ds and four or eight banks of memory.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions in these models include two or four A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74690.

Features
- One or two L-Band tuners accept RF signals from 925 MHz to 2175 MHz
- One or two programmable LNAs boost LNB (low-noise block) antenna signal levels with up to 60 dB gain
- One or two programmable analog downconverters provide I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two or four 200 MHz 16-bit A/Ds
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM; or: 32 MB or 64MB of QDRII+ SRAM
- Clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

Pentek, Inc. One Park Way ♦ Upper Saddle River ♦ New Jersey 07458 Tel: 201-818-5900 ♦ Fax: 201-818-5904 ♦ Email: info@pentek.com www.pentek.com
A/D Acquisition IP Modules

These models feature two or four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

A/D Converter Stage

The analog baseband I and Q analog tuner outputs are then applied to two or four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

A/D Clocking and Synchronization

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the board. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave boards, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Cobalt architecture supports up to four or eight independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.
One or two L-Band RF Tuners, 2- or 4-Channel 200 MHz A/D, Virtex-6 FPGA - cPCI

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC</td>
</tr>
<tr>
<td>73690</td>
<td>2 RF tuners, four A/Ds</td>
</tr>
<tr>
<td>74690</td>
<td>2 RF tuners, four A/Ds</td>
</tr>
</tbody>
</table>

Options:

- 062 XCV6LX240T FPGA
- 064 XCV6VSX315T FPGA
- 104 LVDS I/O between the FPGA and J2 connector, Model 73690; J3 and J5 connectors, Model 74690
- 150 Two 8 MB QDRII+ SRAM Memory Banks (Banks 1 and 2)
- 160 Two 8 MB QDRII+ SRAM Memory Banks (Banks 3 and 4)
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Specifications

Model 72690 or Model 73690: 1 RF tuner, 2 A/Ds
Model 74690: 2 RF tuners, four A/Ds

Front Panel Analog Signal Inputs (1 or 2)
Connector: Front panel female SSMC
Impedance: 50 ohms

L-Band Tuners (1 or 2)
Type: Maxim MAX2112
Input Frequency Range: 925 MHz to 2175 MHz
Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
Fractional-N PLL Synthesizer:
freqVCO = (N.F) x freqREF where integer N = 19 to 251 and fractional F is a 20-bit binary value
PLL Reference (freqREF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz
LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter*
Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps*
*Usable Full-Scale Input Range: -50 dBm to +10 dBm
Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution
A/D Converters (2 or 4)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

PCI-X Interface

The models include an industry-standard interface compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73690: 32 bits only.

Sample Clock Sources (1 or 2)
On-board timing generator/synthesizer

A/D Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

Timing Generator External Clock Inputs (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

Timing Generator Bus (1 or 2): 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (2 or 4)
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T or XC6VSX315T

Custom I/O
Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73690; J3 connector, Model 72690; J3 and J5 connectors, Model 74950

Memory Banks (1 or 2)
Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface
PCI-X Bus: 32 or 64 bits at 33 or 66 MHz Model 73690: 32 bits only

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard 6U or 3U cPCI board
General Information

Model 56690 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56690 includes a front panel general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56690 factory-installed functions include two A/D acquisition IP modules.

IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56690 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

---

Features

- Accepts RF signals from 925 MHz to 2175 MHz
- Programmable LNA boosts LNB (low-noise block) antenna signal levels with up to 60 dB gain
- Programmable analog downconverter provides I + Q baseband signals with bandwidths ranging from 4 to 40 MHz
- Two 200 MHz 16-bit A/Ds digitize the I + Q signals synchronously
- Supports Xilinx Virtex-6 LXT and SXT FPGAs
- 2 GB of DDR3 SDRAM or 32 MB of QDRII+ SRAM
- Sample clock/sync to an external system reference
- Clock/sync bus for multiformate syncronization
- PCI Express (Gen. 1 & 2) interface, up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional front panel LVDS connections to the Virtex-6 FPGA for custom I/O
**RF Tuner Stage**

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB (low noise block). A Maxim MAX2112 tuner directly converts these L-Band signals to baseband using a broadband I/Q downconverter.

The device includes an RF variable-gain LNA (low noise amplifier), a PLL (phase-locked loop) synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters with programmable cutoff frequency, and variable-gain baseband amplifiers.

The fractional-N PLL synthesizer locks its VCO to the timing generator output, or to an external reference input between 12 and 30 MHz. Together, the baseband amplifiers and the RF LNA offer a programmable linear gain range of 60 dB.

An integrated lowpass filter with variable bandwidth provides bandwidths ranging from 4 to 40 MHz, programmable with 8 bits of resolution.

**A/D Converter Stage**

The analog baseband I and Q analog tuner outputs are then applied to two Texas Instruments ADS5485 200 MHz, 16-bit A/D converters. The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

**A/D Clocking and Synchronization**

An internal timing generator provides all timing, gating, triggering and synchronization functions required by the A/D converters. It also serves as an optional source for the L-Band tuner reference.

The front panel SSMC clock input can be used directly as the A/D sample clock. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (voltage-controlled crystal oscillator). In this mode, the front panel SSMC clock input connector accepts a 10 MHz reference signal for synchronizing the VCXO using a PLL.

The timing generator uses a front panel LVPECL 26-pin clock/sync connector for one clock, two sync, and two gate/trigger signals. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate/trigger signals within the module. In the master mode, the LVPECL bus drives output timing signals to synchronize multiple slave modules, supporting synchronous sampling and sync functions across all connected modules.

**Memory Resources**

The 56690 architecture supports up to four independent memory banks which can be configured with all QDRII+ SRAM, all DDR3 SDRAM, or as combination of two banks of each type of memory.

---

**A/D Acquisition IP Modules**

The 56690 features two A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from either of the two A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Each QDRII+ SRAM bank can be up to 8 MB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. For applications requiring deeper memory resources, DDR3 SDRAM banks can each be up to 512 MB deep. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

The factory-installed A/D acquisition modules use memory banks 1 & 2. Banks 3 & 4 can be optionally installed to support custom user-installed IP within the FPGA.

**AMC Interface**

The Model 56690 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56690 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Specifications**

**Front Panel Analog Signal Input**
- Connector: Front panel female SSMC
- Impedance: 50 ohms

**L-Band Tuner**
- Type: Maxim MAX2112
- Input Frequency Range: 925 MHz to 2175 MHz
- Monolithic VCO Phase Noise: -97 dBc/Hz at 10 kHz
- Fractional-N PLL Synthesizer: 
  - freq\_VCO = (N.F) x freq\_REF
  - where integer N = 19 to 251 and fractional F is a 20-bit binary value
- PLL Reference (freq\_REF): Front panel SSMC connector or on-board 27 MHz crystal (Option -100), 12 to 30 MHz LNA Gain: 0 to 65 dB, controlled by a programmable 12-bit D/A converter
- Baseband Amplifier Gain: 0 to 15 dB, in 1 dB steps
- *Usable Full-Scale Input Range: -50 dBm to +10 dBm
- Baseband Low Pass Filter: Cutoff frequency programmable from 4 to 40 MHz with 8-bit resolution

**A/D Converters**
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

**Sample Clock Sources**: On-board timing generator/synthesizer

**A/D Clock Synthesizer**
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, for the A/D clock

**Timing Generator External Clock Input**
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 200 MHz (up to 800 MHz when Timing Generator divider is enabled) or PLL system reference

**Timing Generator Bus**: 26-pin front panel connector LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

**External Trigger Input**
- Quantity: 2
- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array**
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**
- Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**
- Option 150 or 160: Two 8 MB QDRII+ SRAM memory banks, 400 MHz DDR
- Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**PCI-Express Interface**
- PCI Express Bus: Gen. 1 x4 or x8; Gen. 2 x4

**AMC Interface**
- Type: AMC.1
- Module Management: IPMI Version 2.0

**Environmental**
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
General Information

Model 71760 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Advanced reconfigurability features
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458 Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com www.pentek.com
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an

---

**A/D Acquisition IP Modules**

The 71760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Options:
- 71760 4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - XMC
  - Xilinx Virtex-7 XC7VX690T-2
  - Xilinx Virtex-7 XC7VX330T-2

Memory Resources
The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

XMC Interface
The Model 71760 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71760 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

PCI Express Interface
The Model 71760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coilcraft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters
- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input
- Type: Front panel female SSMC connector, LV TTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard XMC module, 2.91 in. x 5.87 in.

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 78760 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78760 includes optional general-purpose and gigabit-serial connectors for application-specific I/O protocols.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

**Clocking and Synchronization**

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an...
Model 78760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - x8 PCIe

➤ external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 78760’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 78760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel female SSMC connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS5485
- Sampling Rate: 10 MHz to 200 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

- Type: Front panel female SSMC connector, LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

- Option -104: Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

Environmental

- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half length PCIe card, 4.38 in. x 7.13 in.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Model 53760

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

**General Information**

Model 53760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 53760 includes four A/Ds and four banks of memory. It features built-in support for PCIe Express over the 3U VPX backplane.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

---

Model 53760 COTS (left) and rugged version

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Advanced reconfigurability features
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 53760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel.

Model 53760: 4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - 3U VPX

PCI Express Interface

The Model 53760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Support PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Fabric-Transparent Crossbar Switch

The 53760 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model 53760

Description: 4-Channel 200 MHz A/D with Virtex-7 FPGA - 3U VPX

Options:
- 073 XC7VX330T-2 FPGA
- 076 XC7VX690T-2 FPGA
- 104 LVDS FPGA I/O to VPX P2
- 105 Gigabit serial FPGA I/O to VPX P1

Model 8267

Description: VPX Development System

Contact Pentek for availability of rugged and conduction-cooled versions

SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/ Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple 53760’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The 53760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

Transformation Type: Coil Craft WBC4-6TLL

Full Scale Output: +8 dBm into 50 ohms

3 dB Passband: 300 kHz to 700 MHz

A/D Converters

Type: Texas Instruments ADS5485

Sampling Rate: 10 MHz to 200 MHz

Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector

Timing Bus: 26-pin front panel connector; LVPECL bus includes clock sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX690T-2

Optional: Xilinx Virtex-7 XC7VX330T-2

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen 1 or Gen 2: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
General Information

Model 52760 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

The 52760 includes four A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt Family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 200 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel.
PCI Express Interface
The Model 52760 includes an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Options</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>52760</td>
<td>4-Channel 200 MHz A/D with Virtex-7 FPGA - 3U VPX</td>
<td>-073</td>
<td>XC7VX330T-2 FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-076</td>
<td>XC7VX690T-2 FPGA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-104</td>
<td>LVDS FPGA I/O to VPX P2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-105</td>
<td>Gigabit serial FPGA I/O to VPX P1</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267 Description
VPX Development System
See 8267 Datasheet for Options

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMM connectors
- Transformer Type: Coil Craft
- WBC4-6TLB
- Full Scale Input: +8 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz
- A/D Converters
  - Type: Texas Instruments ADS5485
  - Sampling Rate: 10 MHz to 200 MHz
  - Resolution: 16 bits
- Sample Clock Sources: On-board clock synthesizer
- Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
  - Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
  - Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
- Type: Front panel female SSMM connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference
- Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1 or Gen. 2: x4

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td>One XMC</td>
</tr>
<tr>
<td># of XMCs</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4 or x8</td>
<td>x4 or x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
General Information

Models 57760 and 58760 are members of the Onyx™ family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a VPX carrier board.

Model 57760 is a 6U board with one Model 71760 module while the Model 58760 is a 6U board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57760; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58760.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four or eight 200 MHz 16-bit A/Ds
- 4 or 8 GB of DDR3 SDRAM
- PCIe Express (Gen. 1, 2 & 3) interface up to x8
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.
Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Model 57760: 4 A/Ds
Model 58760: 8 A/Ds

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T
Optional: Xilinx Virtex-7 XC7VX690T

Custom I/O
Option -104: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57760; P3 and P5, Model 58760
Option -105: Supports serial protocols by providing a 4x gigabit link between the FPGA and VPX P2, Model 57760; or one 4x link from each FPGA to P2 and an additional 4x link between the FPGAs, Model 58760.

Memory Banks (4 or 8)
Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)

Contact Pentek for availability of rugged and conduction-cooled versions

Options:

Model 57760
4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U VPX
Model 58760
8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U VPX

Options:

-076 XCVX690T-2 FPGA
-104 LVDS I/O between the FPGA and P3 connector, Model 57760; P3 and P5 connectors, Model 58760
-105 Gigabit link between the FPGA and P2 connector, Model 57760; gigabit links from each FPGA to P2 connector, Model 78760

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
### General Information

Models 72760, 73760 and 74760 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71760 XMC modules mounted on a cPCI carrier board.

Model 72760 is a 6U cPCI board while the Model 73760 is a 3U cPCI board; both are equipped with one Model 71760 XMC. Model 74760 is a 6U cPCI board with two XMC modules rather than one.

These models include four or eight A/Ds and four or eight banks of memory.

### The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include four or eight A/D acquisition IP modules for simplifying data capture and data transfer.

### Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- Four or eight 200 MHz 16-bit A/Ds
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- LVPECL clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

### Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760.

---

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four or eight full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four or eight Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

A/D Acquisition IP Modules

These models feature four or eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of four A/Ds or the test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple boards to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple boards.

Multiple boards can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73760: 32 bits only.

Specifications

Model 72760 or Model 73760: 4 A/Ds
Model 74760: 8 A/Ds

Front Panel Analog Signal Inputs (4 or 8)

<table>
<thead>
<tr>
<th>Input Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer-coupled, front panel female SSMC connectors</td>
<td></td>
</tr>
</tbody>
</table>

Transformer Type: Coil Craft
WBC4-6TLB

Full Scale Input: +8 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

Ordering Information

Model Description
72760 4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U cPCI
73760 4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U cPCI
74760 8-Channel 200 MHz 16-bit A/D with two Virtex-7 FPGAs - 6U cPCI

Options:
-073 XC7VX330T-2 FPGA
-076 XC7VX690T-2 FPGA
-104 LVDS I/O between the FPGA and J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760

A/D Converters (4 or 8)
Type: Texas Instruments ADS5485
Sampling Rate: 10 MHz to 200 MHz
Resolution: 16 bits

Sample Clock Sources: (1 or 2)
On-board clock synthesizer

Clock Synthesizers (1 or 2)
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clocks (1 or 2)
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus (1 or 2)
26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Inputs (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73760; J3 connector, Model 72760; J3 and J5 connectors, Model 74760

Memory Banks (1 or 2)
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board
General Information

Model 56760 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multi-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 56760 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
A/D Acquisition IP Modules

The 56760 features four A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the four A/Ds or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-Pcie configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts four full-scale analog HF or IF inputs on front panel SSMC connectors at +8 dBm into 50 ohms with transformer coupling into four Texas Instruments ADS5485 200 MHz, 16-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives

---

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201.818.5900 ● Fax: 201.818.5904 ● Email: info@pentek.com
www.pentek.com

Model 56760
4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA - AMC
➤ an external sample clock from the front panel SSMC connector. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable voltage-controlled crystal oscillator. In this mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel 26-pin LVPECL Clock/Sync connector allows multiple modules to be synchronized. In the slave mode, it accepts LVPECL inputs that drive the clock, sync and gate signals. In the master mode, the LVPECL bus can drive the timing signals for synchronizing multiple modules.

Multiple 56760’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules.

Memory Resources

The 56760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

AMC Interface

The Model 56760 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface

The Model 56760 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

<table>
<thead>
<tr>
<th>Type</th>
<th>Texas Instruments ADS5485</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sampling Rate</td>
<td>10 MHz to 200 MHz</td>
</tr>
<tr>
<td>Resolution</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

Timing Bus: 26-pin front panel connector; LVPECL bus includes, clock/sync/gate/PPS inputs and outputs; TTL signal for gate/trigger and sync/PPS inputs

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8; Gen. 3 available only with the VX330T-2 and VX690T-2 FPGAs

AMC Interface

Type: AMC.1

Module Management: IPMI Version 2.0

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.

Contact Pentek for availability of rugged and conduction-cooled versions.
Model 71730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - XMC

General Information

Model 71730 is a member of the Onyx® family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connections to HF or IF ports of communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 71730 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.
**A/D Acquisition IP Module**

The 71730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 71730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to Rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture, or for routing to other module resources.

**D/A Converter Stage**

The 71730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GS/sec, allowing it to accept full-rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
XMC Interface

The Model 71730 complies with the VITA 42.0 XMC specification. Two connectors each provide dual 4X links or a single 8X link with up to 10 Gb/sec per lane. With dual XMC connectors, the 71730 supports x8 PCIe on the first XMC connector leaving the second connector free to support user-installed transfer protocols specific to the target application.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals. The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 71730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADS5400

Sampling Rate: 100 MHz to 1 GHz

Resolution: 12 bits

D/A Converter

Type: Texas Instruments DAC5681Z

Input Data Rate: 1 GHz max.

Interpolation Filter: bypass, 2x or 4x

Output Sampling Rate: 1 GHz max.

Resolution: 16 bits

Front Panel Analog Signal Outputs

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA

Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.
**General Information**

Model 78730 is a member of the Onyx® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and 1 GHz D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 78730 includes optional general-purpose and gigabit serial card connectors for application specific I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

---

**Features**

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O

---

**Diagram**

The diagram illustrates the board's connectivity and components, highlighting the integration of the PCIe, DDR3 SDRAM, and other key features of the Model 78730.
**A/D Acquisition IP Module**

The 78730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The Model 78730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

---

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-Pcie configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx IMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments ADS5400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other board resources.

**D/A Converter Stage**

The 78630 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator provides a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7892 and Model 9192 Cobalt Synchronizers can drive multiple 78730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The 78730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78630 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

 Specifications

Front Panel Analog Signal Inputs

| Type: Transformer-coupled, front panel female SSMC converters |

A/D Converter

| Type: Texas Instruments ADS5400 |
| Sampling Rate: 100 MHz to 1 GHz |
| Resolution: 12 bits |

D/A Converter

| Type: Texas Instruments DAC5681Z |
| Input Data Rate: 1 GHz max. |

Clock Synthesizer

| Clock Source: Selectable from on-board programmable VCXO or front panel external clock |

VCXO Frequency Ranges:

- 10 to 945 MHz
- 970 to 1134 MHz
- 1213 to 1214 MHz

Synchronization:

- VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock

| Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference |

Timing Bus:

- 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

| Type: Front panel female SSMC connector, LVTTL |

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

| Standard: Xilinx Virtex-7 XC7VX330T-2 |
| Optional: Xilinx Virtex-7 XC7VX690T-2 |

Custom I/O

| Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O. |
| Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board |

Memory

| Type: DDR3 SDRAM |
| Size: Four banks, 1 GB each |
| Speed: 800 MHz (1600 MHz DDR) |

PCI-Express Interface

| PCI Express Bus: Gen. 1, 2 or 3: x4 or x8 |

Environmental

| Operating Temp: 0° to 50° C |
| Storage Temp: -20° to 90° C |
| Relative Humidity: 0 to 95%, non-cond. |
| Size: Half length PCIe card, 4.38 in. x 7.13 in. |

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

Options:

| -073 | XC7VX330T-2 FPGA |
| -076 | XC7VX690T-2 FPGA |
| -104 | LVDS FPGA I/O through 68-pin ribbon cable connector |
| -105 | Gigabit serial FPGA I/O through two 4X top edge connectors |

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266

PC Development System

See 8266 Datasheet for Options

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
Model 53730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

General Information
Model 53730 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Module

The 53730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 53730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software switch setting. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments AD85400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 53730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤
Model 53730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

Memory Resources
The Model 53730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board's DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface
The Model 53730 includes an industry-standard interface fully compliant with PCI Express Gen 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267
The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

Crossbar Switch
The Model 8267 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- A/D Converter
  - Type: Texas Instruments ADS5400
  - Input Data Rate: 100 MHz to 1 GHz
  - Resolution: 12 bits
- D/A Converter
  - Type: Texas Instruments DAC5681Z
  - Input Data Rate: 1 GHz max.
  - Interpolation Filter: bypass, 2x or 4x
  - Output Sampling Rate: 1 GHz max.
  - Resolution: 16 bits

Front Panel Analog Signal Outputs
- Output Type: Transformer-coupled, front panel female SSMC connectors
- Sample Clock Sources: On-board clock generates two clocks: one A/D clock and one D/A clock
- Clock Synthesizer
  - Clock Source: Selectable from on-board programmable VCXO or front panel external clock
  - VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
  - Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
- Type: Front panel female SSMC connector
- LVTTL
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1 or Gen. 2: x4 or x8;

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
Model 52730

1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX

General Information

Model 52730 is a member of the Onyx® family of high performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution.

It includes 1 GHz A/D and D/A converters and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance of the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One 1 GHz 12-bit A/D
- One 1 GHz 16-bit D/A
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1 and 2) interface up to x4
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
FPGA DATAFLOW

IP Module

A/D Acquisition IP Module

The 52730 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The Model 52730 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reconfiguring the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a Texas Instruments AD85400 1 GHz, 12-bit A/D converter.

The digital outputs are delivered into the Virtex-6 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

The 52730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a front panel SSMC connector. ➤
### Memory Resources
The 52730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D and D/A data capture, tagging and streaming.

### PCI Express Interface
The Model 52730 includes an industry-standard interface fully compliant with PCI Express Gen. 1 & 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

#### Model 8267
The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

#### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>52730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

#### Options:
- 073  | XC7VX330T-2 FPGA                                   |
- 076  | XC7VX690T-2 FPGA                                   |
- 104  | LVDS FPGA I/O to VPX P2                           |
- 105  | Gigabit serial FPGA I/O to VPX P1                 |

Contact Pentek for availability of rugged and conduction-cooled versions

---

### External Clock
- **Type:** Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

### Timing Bus
- **Option -104:** Provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

### Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Optional:** Xilinx Virtex-7 XC7VX690T-2

### Custom I/O
- **Option -104**
- **Option -105**

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

### VPX Families
Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

### VPX Family Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td></td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td></td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x4 or x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>24 pairs on VPX P2</td>
<td>20 pairs on VPX P2</td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>
1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

**General Information**

Models 57730 and 58730 are members of the Onyx® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a VPX carrier board.

Model 57730 is a 6U board with one Model 71730 module while the Model 58730 is a 6U board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory

**The Onyx Architecture**

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730.

Option -105 supports serial protocalls by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730.

---

**Features**

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- 4 or 8 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Dual-µSync clock/sync bus for multiboard synchronization
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

---

**GateXpress ReadyFlow Board Support Package**

---

**Support Models**

- Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458
  Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
  www.pentek.com
FPGA DATAFLOW

IP Modules

A/D Acquisition IP Module

These models feature one or two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, a test signal generator, or from the D/A Waveform Playback IP Module in loopback mode. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface.

This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGAs. At power-up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGAs time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user. In this case, it’s programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image to load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGAs with new IP images. The first option is to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGAs through JTAG using Xilinx iMPACT.

In all three FPGA-loading scenarios, GateXpress handles the hardware negotiation thereby simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without the need to reset the host computer so it can rediscover the board. After the reload, the host computer simply continues to see the board with the expected device ID.

A/D Converter Stages

The front end accepts one or two analog HF or IF inputs on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.

D/A Converter Stages

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2- or 1/4-rate input data. Analog output is through front panel SSMC connectors.

The digital outputs are delivered into the Virtex-7 FPGAs for signal processing, data capture or for routing to other board resources.

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - 6U OpenVPX

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8264

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57730</td>
<td>1 GHz A/D and D/A with Virtex-7 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58730</td>
<td>Two 1 GHz A/Ds and D/As, with two Virtex-7 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:

- 076  | XC7VX690T-2 FPGA
- 104  | LVDS I/O between the FPGA and P3 connector, Model 57730; P3 and P5 connectors, Model 58730
- 105  | Gigabit link between the FPGA and P2 connector, Model 57730; gigabit links from each FPGA to P2 connector, Model 78730

Contact Pentek for availability of rugged and conduction-cooled versions

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple boards to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 9192 Cobalt or Onyx Synchronizer can drive multiple µSync connectors enabling large, multichannel synchronous configurations. Also, an LVLTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 57730: 1 A/D, 1 D/A
Model 58730: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converters (1 or 2)

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, LVLTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O (1 or 2)

Option -04: Provides 24 LVDS pairs between the FPGA and the VPX P3 connector, Model 57730; P3 and P5, Model 58730
Option -05: Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57730; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58730

Memory Banks (4 or 8)

Type: DDR3 SDRAM
Size: 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 72730, 73730 and 74730 are members of the Onyx® family of high-performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71730 XMC modules mounted on a cPCI carrier board.

Model 72730 is a 6U cPCI board while the Model 73730 is a 3U cPCI board; both are equipped with one Model 71730 XMC. Model 74730 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two 1 GHz A/D and D/A converters and four or eight banks of memory.

The Onyx Architecture

The Pentek Onyx Architecture features Virtex-7 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, trigger and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition and one or two D/A waveform playback IP modules for simplifying data capture and data transfer.

Features

- Complete radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCI/PCI-X bus
- One or two 1 GHz 12-bit A/D
- One or two 1 GHz 16-bit D/A
- Four or eight GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- Dual-µSync clock/sync bus for multimodule synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730.
GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCI-X discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCI-X interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCI-X interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCI-X configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts one or two analog HF or IF input on front panel SSMC connectors with transformer coupling into one or two Texas Instruments ADS5400 1 GHz, 12-bit A/D converters. The digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

D/A Converter Stage

These models feature one or two TI DAC5681Z 1 GHz, 16-bit D/As. The converters have an input sample rate of 1 GSPS, allowing them to accept full rate data from the FPGA. Additionally, the D/As include a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through front panel SSMC connectors.

The factory-installed functions include one or two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board memory or off-board host memory to the D/A. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 or 128 individual link entries can be chained together to create complex waveforms with a minimum of programming.
1- or 2-Channel 1 GHz A/D, 1- or 2-Channel 1 GHz D/A with Virtex-7 FPGA - cPCI

Clocking and Synchronization

Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths. Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 7192 and Model 9192 Cobalt Synchronizers can drive multiple 71630 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources

The Onyx architecture supports four or eight independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications

Model 72730 or Model 73730: 1 A/D, 1 D/A
Model 74730: 2 A/Ds, 2 D/As

Front Panel Analog Signal Inputs (1 or 2)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits

D/A Converters (1 or 2)

Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs (1 or 2)

Output Type: Transformer-coupled, front panel female SSMC connectors

Sample Clock Sources (1 or 2)

On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizers (1 or 2)

Clock Source: Selectable from on-board programmable VCXO or front panel external clock

VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz

Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clocks (1 or 2)

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730

Memory Banks (1 or 2)

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz
Model 73730: 32 bits only

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73730</td>
<td>1 GHz A/D and D/A, Virtex-7 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74730</td>
<td>Two 1 GHz A/D and D/A, Virtex-7 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:

-073  XC7VX330T-2 FPGA
-076  XC7VX690T-2 FPGA
-104  LVDS I/O between the FPGA and J2 connector, Model 73730; J3 connector, Model 72730; J3 and J5 connectors, Model 74730
Model 56730

1 GHz A/D and 1 GHz D/A, Virtex-7 FPGA - AMC

General Information

Model 56730 is a member of the Onyx® family of high performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen.3 as a native interface, the Model 56730 includes a front panel general-purpose connector for application-specific I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56730 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.
**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is especially useful in security situations where there can be no latency in user image control. For volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The 56730 features a TI DAC5681Z 1 GHz, 16-bit D/A. The converter has an input sample rate of 1 GSPS, allowing it to accept full rate data from the FPGA. Additionally, the D/A includes a 2x or 4x interpolation filter for applications that provide 1/2 or 1/4 rate input data. Analog output is through a PCI Express PCIe interface.

**D/A Converter Stage**

The 56730 features an A/D and D/A with a sampling rate of 1 GSPS for signal processing, data capture or for routing to other module resources.
AMC Interface
The Model 56730 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56730 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization
Two internal timing buses provide either a single clock or two different clock rates to the A/D and D/A signal paths.

Each timing bus includes a clock, sync and a gate or trigger signal. An on-board clock generator receives a sample clock either from the front panel SSMC connector or from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this latter mode, the front panel SSMC connector can be used to provide a 10 MHz reference clock to phase-lock the VCXO. Either clock source (front panel or VCXO) can be used directly or can be divided independently by 2, 4, 8, or 16 to provide different lower frequency A/D and D/A clocks.

A pair of front panel µSync connectors allows multiple modules to be synchronized. They accept CML inputs that drive the board’s sync and gate/trigger signals.

The Pentek Model 5692 and Model 9192 Cobalt Synchronizers can drive multiple 56730 µSync connectors enabling large, multichannel synchronous configurations. Also, an LVTTL external gate/trigger input is accepted on a front panel SSMC connector.

Memory Resources
The 56730 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include an A/D data transient capture mode and D/A waveform playback mode.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: Texas Instruments ADS5400
Sampling Rate: 100 MHz to 1 GHz
Resolution: 12 bits
D/A Converter
Type: Texas Instruments DAC5681Z
Input Data Rate: 1 GHz max.
Interpolation Filter: bypass, 2x or 4x
Output Sampling Rate: 1 GHz max.
Resolution: 16 bits

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel female SSMC connectors
Sample Clock Sources: On-board clock synthesizer generates two clocks: one A/D clock and one D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO or front panel external clock
VCXO Frequency Ranges: 10 to 945 MHz, 970 to 1134 MHz, and 1213 to 1417 MHz
Synchronization: VCXO can be phase-locked to an external 4 to 200 MHz system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16, independently for the A/D clock and D/A clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 100 MHz to 1 GHz divider input clock, or PLL system reference
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LV TTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2
Custom I/O
Option -104: Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

General Information

Model 71741 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- μSync clock/sync bus for multmodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Module

The 71741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in a FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel IP sample-accurate time stamp and a rate of \( f_s/N \). Each DDC delivers a complex output stream consisting of 16-bit I \( + \) 16-bit Q samples at a rate of \( f_s/N \).

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

---

**1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC**

- **Virtex-7 FPGA Dataflow Detail**
- **Two channel mode shown**
- **Programmable decimation of 8, 16 or 32 available in one channel mode.**

---

**Pentek, Inc.**
One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

[www.pentek.com](http://www.pentek.com)
Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

Memory Resources

The 71741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Options:
- Option -105: Gigabit serial FPGA I/O
- Option -104: LVDS FPGA I/O through P14 connector
- Option -105: Gigabit serial FPGA I/O through P16 connector

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

PCI Express Interface

The Model 71741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 71741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71741’s can be synchronized with a simple cable. For larger systems, multiple 71741’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: +2 dBm to +4 dBm, programmable

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xxx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model Description
71741 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC

Option:
- Option -076: XC7VX690T-2 FPGA
- Option -104: LVDS FPGA I/O through P14 connector
- Option -105: Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8266 PC Development System See 8266 Datasheet for Options

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard XMC module, 2.91 in. x 5.87 in.
Model 78741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

**General Information**

Model 78741 is a member of the Onyx® family of high-performance PCIe modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

**The Onyx Architecture**

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-7 FPGA**

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.

---

**Features**

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 V7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Module

The 78741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_0 \), where \( f_s \) is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - x8 PCIe

Model 78741

Memory Resources

The 78741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards (Models 78xx). It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC</td>
</tr>
</tbody>
</table>

Options:

-073   | XC7VX330T-2 FPGA                                |
-076   | XC7VX690T-2 FPGA                                |
-104   | LVDS FPGA I/O through 68-pin ribbon cable connector |
-105   | Gigabit serial FPGA I/O through two 4X top edge connectors |

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converter

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters

Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector

Clocking and Synchronization

The 78471 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC connector accepts a TTL signal that can function as Gate, PPS or Sync.

Front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 78471’s can be synchronized with a simple cable. For larger systems, multiple 78471’s can be synchronized using the Model 7892 high-speed sync board to drive the sync bus.

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A&D Converter

Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters

Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to f_s
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Connects 24 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
Option -105: Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half-length PCIe card, 4.38 in. x 7.13 in.
1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Model 53741

Features
- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- µSync clock(sync) bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)

General Information
Model 53741 is a member of the Onyx® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture
Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA
The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.
Model 53741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 53741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

Clocking and Synchronization
The 53741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel μSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The μSync bus includes gate, reset, and in and out reference clock signals. Two 53741’s can be synchronized with a simple cable. For larger systems, multiple 53741’s can be synchronized using the Model 5392 high-speed sync board to drive the sync bus.

PCI Express Interface
The Model 53741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers.

Specifications
Front Panel Analog Signal Inputs
- Input Type: Transformer-coupled, front panel female SSMC connectors
- A/D Converter
  - Type: Texas Instruments ADC12D1800
  - Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
  - Resolution: 12 bits
  - Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
  - Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
- Modes: One or two channels, programmable
- Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
- Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel: 4x, 8x, or 16x

Location
- LO Tuning Freq. Resolution: 32 bits, 0 to $f_s$
- LO SFDR: >120 dB
- Phase Offset Resolution: 32 bits, 0 to 360 degrees
- FIR Filter: User-programmable 18-bit coefficients
- Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector
- Timing Bus: 19-pin μSync bus connector includes sync and gate/trigger inputs, CML
- External Trigger Input
  - Type: Front panel female SSMC connector, LVTTL
  - Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
- Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 to support serial protocols

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: −20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: 3.937 in x 6.717 in. (100 mm x 170.6 mm)

VPX Families
Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td></td>
<td>VPX Development System See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>

Options:
- -073: XC7VX330T-2 FPGA
- -076: XC7VX690T-2 FPGA
- -104: LVDS FPGA I/O to VPX P2
- -105: Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions.

 penalties. Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>52xxx</td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>53741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX</td>
</tr>
<tr>
<td></td>
<td>VPX Development System See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>

Options:
- -073: XC7VX330T-2 FPGA
- -076: XC7VX690T-2 FPGA
- -104: LVDS FPGA I/O to VPX P2
- -105: Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions.

Tele: 201.818.5900 Fax: 201.818.5904 Email: info@pentek.com
Model 52741 is a member of the Onyx family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48A1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P1 connector for custom I/O. Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
A/D Acquisition IP Module

The 52741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel A/D, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver 80% output bandwidth is better than 100 dB. Adjacent-band components within the 80% output bandwidth need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply...
Memory Resources

The 52741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

PCI Express Interface

The Model 52741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model Description
52741 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - 3U VPX

Options:
-073 XC7VX330T-2 FPGA
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O to VPX P2
-105 Gigabit serial FPGA I/O to VPX P1

Contact Pentek for availability of rugged and conduction-cooled versions

VPX Family Comparison

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>3U VPX</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td>One XMC</td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1</td>
<td>VPX P1 or P2</td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4</td>
<td>x8</td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1 or P2</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Development Systems

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - 3U VPX

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: ±2 dBm to ±4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable

Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x

LO Tuning Freq. Resolution: 32 bits, 0 to ƒs

LO SFDR: >120 dB

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
Model 71741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - XMC

General Information

Model 71741 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution.

It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with dual 4X gigabit links to the FPGA to support serial protocols.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- μSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Module

The 71741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of acquiring a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core. The core supports a single-channel IP core.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to fₛ/ₙ, where fₛ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8fₛ/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of fₛ/N.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.
Memory Resources
The 71741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

SPARK Development Systems

Ordering Information
Model | Description
--- | ---
71741 | 1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - XMC

Options:
-073 | XC7VX330T-2 FPGA
-076 | XC7VX690T-2 FPGA
-104 | LVDS FPGA I/O through P14 connector
-105 | Gigabit serial FPGA I/O through P16 connector

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
PC Development System
See 8266 Datasheet for Options

Model 71741
The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converter Stage
The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing the 71741 to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple modules.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other module resources.

PCI Express Interface
The Model 71741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization
The 71741 accepts a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync. A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two 71741’s can be synchronized with a simple cable. For larger systems, multiple 71741’s can be synchronized using the Model 7192 high-speed sync module to drive the sync bus.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to 7
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.
### General Information

Models 72741, 73741 and 74741 are members of the Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA. They consist of one or two Model 71741 XMC modules mounted on a cPCI carrier board.

Model 72741 is a 6U cPCI board while the Model 73741 is a 3U cPCI board; both are equipped with one Model 71741 XMC. Model 74741 is a 6U cPCI board with two XMC modules rather than one. These models include one or two 3.6 GHz, 12-bit A/D converters, four or eight banks of memory, and one or two wideband DDCs.

### The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules and one or two wideband DDCs.

In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

### Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741.

---

### Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDCs (Digital Downconverters)
- 4 or 8 GB of DDR3 SDRAM
- μSync clock/sync bus for multiboard synchronization
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

---

![Block Diagram, Model 72741](https://example.com/block-diagram.png)

![Features Diagram](https://example.com/features-diagram.png)

---

The Onyx® family of high performance CompactPCI boards based on the Xilinx Virtex-7 FPGA is available from Pentek, Inc., with a wide range of options and configurations to meet the needs of radar and software radio applications. For more information, please visit www.pentek.com or contact us at 201-818-5900.
**FPGA DATAFLOW**

In single-channel mode, all banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

---

**DDC IP Cores**

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to $8x$, $16x$ or $32x$. In dual-channel mode, both channels share the same decimation rate, programmable to $4x$, $8x$ or $16x$.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_s / N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s / N$.

---

**GateXpress for FPGA Configuration**

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
½ on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx IMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz.

The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm. A built-in AutoSync feature supports A/D synchronization across multiple boards.

The A/D digital outputs are delivered into the Virtex-7 FPGA for signal processing, data capture or for routing to other board resources.

**Clocking and Synchronization**

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSSM connector. A second front panel SSSM accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two boards can be synchronized with a simple cable. For larger systems, multiple boards can be synchronized using the Models 7292, 7392 or 7492 high-speed sync boards to drive the sync bus.

**Specifications**

Model 72741 or Model 73741: One A/D

Model 74741: Two A/Ds

Front Panel Analog Signal Inputs (2 or 4)

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converters (1 or 2)

Type: Texas Instruments ADC12D1800

Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz

Resolution: 12 bits

Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz

Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters (2 or 4)

Modes: One or two channels, programmable

Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz

Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x or 16x

LO Tuning Freq. Resolution: 32 bits, 0 to 14 GHz

LO SFDR: >120 dB

Phase Offset Resolution: 32 bits, 0 to 360 degrees

FIR Filter: User-programmable 18-bit coefficients

Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation

Sample Clock Sources (1 or 2)

Front panel SSMC connector

Timing Bus (1 or 2)

19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input (1 or 2)

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)

Standard: Xilinx Virtex-7 XC7VX330T-2

Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O

Option -104: Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73741; J3 connector, Model 72741; J3 and J5 connectors, Model 74741

Memory Banks (1 or 2)

Type: DDR3 SDRAM

Size: Four banks, 1 GB each

Speed: 800 MHz (1600 MHz DDR)

PCI-X Interface

PCI-X Bus: 32 or 64 bits at 33 or 66 MHz

Model 73741: 32 bits only

Environmental

Operating Temp: 0° to 50° C

Storage Temp: –20° to 90° C

Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board
Model 56741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

General Information

Model 56741 is a member of the Onyx® family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56741 includes an optional front-panel connection to the Virtex-7 FPGA for custom I/O.

The Onyx Architecture

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module. Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56741 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow Design Kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The Virtex-7 FPGA site can be populated with one of two FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 installs a front panel connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- One-channel mode with 3.6 GHz, 12-bit A/D
- Two-channel mode with 1.8 GHz, 12-bit A/Ds
- Programmable one- or two-channel DDC (Digital Downconverter)
- 4 GB of DDR3 SDRAM
- μSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Module

The 56741 features an A/D Acquisition IP Module for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated memory banks for buffering data in FIFO mode or for storing data in transient capture mode. In single-channel mode, all four banks are used to store the single-channel of input data. In dual-channel mode, memory banks 1 and 2 store data from input channel 1 and memory banks 3 and 4 store data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory banks are supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

DDC IP Cores

Within the FPGA is a powerful DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D’s 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_a$, where $f_a$ is the A/D sampling frequency.

In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of $f_s/N$.

GateXpress for FPGA Configuration

The Onyx architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored.
Model 56741

1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D, w/ Wideband DDC, Virtex-7 FPGA - AMC

Memory Resources
The 56741 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

AMC Interface
The Model 56741 complies with the AMC.1 specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

PCI Express Interface
The Model 56741 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>56741</td>
<td>1-Ch. 3.6 GHz or 2-Ch. 1.8 GHz, 12-bit A/D with Wideband DDC, Virtex-7 FPGA - AMC</td>
</tr>
</tbody>
</table>

Options:
- 073  XC7VX330T-2 FPGA
- 076  XC7VX690T-2 FPGA
- 104  LVDS FPGA I/O to front panel connector

Contact Pentek for availability of rugged and conduction-cooled versions

A/D Converter
Type: Texas Instruments ADC12D1800
Sampling Rate: Single-channel mode: 500 MHz to 3.6 GHz; dual-channel mode: 150 MHz to 1.8 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 1.75 GHz; dual-channel mode: 2.8 GHz
Full Scale Input: +2 dBm to +4 dBm, programmable

Digital Downconverters
Modes: One or two channels, programmable
Supported Sample Rate: One-channel mode: 3.6 GHz, two-channel mode: 1.8 GHz
Decimation Range: One-channel mode: 8x, 16x or 32x, two-channel mode: 4x, 8x, or 16x
LO Tuning Freq. Resolution: 32 bits, 0 to \( f_s \)
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: User-programmable 18-bit coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Virtex-7 XC7VX330T-2
Optional: Xilinx Virtex-7 XC7VX690T-2

Custom I/O
Option -104: Installs a front panel connector with 24 LVDS pairs to the FPGA

Memory
Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

AMC Interface
Type: AMC.1
Module Management: IPMI Version 2.0

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Single-width, full-height AMC module, 2.89 in. x 7.11 in.
General Information

Model 71610 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O to the carrier board.

Option -105 installs the P16 XMC connector with one 8X or two 4X gigabit links to the FPGA to support serial protocols.

---

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board

---

 MODEL 71610 LVDS Digital I/O with Virtex-6 FPGA - XMC

---

80-pin Front Panel Connector

- 32 Pairs LVDS Data
- LVDS Clock
- Data Valid
- Data Suspend

---

VIRTTEX-6 FPGA

LX130T, LX240T or SX315T

---

Memory Banks 1 & 2

Memory Banks 3 & 4

Config FLASH 64 MB

DDR3 SDRAM 512 MB

DDR3 SDRAM 512 MB

Optional FPGA GPIO

Option 165

Optional 8X PCIe

PMC P14

XMC P15

XMC P16

---

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
Model 71610
LVDS Digital I/O with Virtex-6 FPGA - XMC

➤ Acquisition IP Module

The module can be configured for digital input mode by setting a jumper on the board. In this case, the module accepts input data Clock and input Data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The module can optionally generate a Data Suspend output signal indicating that the 71610 is no longer capable of accepting data. The module accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Module

The module can be configured for digital output mode by setting a jumper on the board. In this case, the module generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The module can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

PCI Express Interface

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Memory Resources

The 71610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

Specifications

Front Panel Input/Output
Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
Clock: One LVDS differential pair, 2.5 V compliant
Data Valid: One LVDS differential pair, 2.5 V compliant
Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array
Standard: Xilinx Virtex-6 XC6VLX130T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Option -105: Installs the XMC P16 connector configurable as one 8X or two 4X gigabit serial links to the FPGA

Memory
Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
Option 16: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8

Environmental
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information
Model Description
71610 LVDS Digital I/O with Virtex-6 FPGA - XMC
Options:
-062 XC6VLX240T
-064 XC6VSX315T
-104 LVDS FPGA I/O through P14 connector
-105 Gigabit serial FPGA I/O through P16 connector
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
* This option is always required

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8266
PC Development System
See 8266 Datasheet for Options
General Information

Model 78610 is a member of the Cobalt® family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 78610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 78610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 78610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Option -105 connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board.
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt and Onyx PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Ordering Information**

**Model Description**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - PCIe</td>
</tr>
</tbody>
</table>

**Options:**

- **-062** XC6VLX240T
- **-064** XC6VSX315T
- **-104** LVDS FPGA I/O through 68-pin ribbon cable connector
- **-105** Gigabit serial FPGA I/O through two 4X top edge connectors
- **-155** Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- **-165** Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

---

**LVDS Digital I/O with Virtex-6 FPGA - x8 PCIe**

**Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 78610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**PCI Express Interface**

The Model 78610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 78610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

**Specifications**

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.
- **Option -105:** Connects two 4X gigabit serial links from the FPGA on XMC P16 to two 4X gigabit serial connectors along the top edge of the PCIe board

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** Half-length PCIe card, 4.38 in. x 7.13 in.
Model 53610 is a member of the Cobalt® family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 53610 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 53610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 53610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Features

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
**Fabric-Transparent Crossbar Switch**

The 53610 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output preemphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

**Model 8267**

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

**Model Description**

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
<th>Options:</th>
</tr>
</thead>
<tbody>
<tr>
<td>53610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - 3U VPX</td>
<td></td>
</tr>
</tbody>
</table>

**Options:**

- 062: XC6VLX240T
- 064: XC6VSX315T
- 104: LVDS FPGA I/O to VPX P2
- 105: Gigabit serial FPGA I/O to VPX P1
- 155*: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

**Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 53610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**PCI Express Interface**

The Model 53610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 53610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

**Specifications**

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
- **Option -105:** Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 163:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**VPX Families**

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>52xxx</strong></td>
</tr>
<tr>
<td><strong>Form Factor</strong></td>
</tr>
<tr>
<td><strong># of XMCs</strong></td>
</tr>
<tr>
<td><strong>Crossbar Switch</strong></td>
</tr>
<tr>
<td><strong>PCIe Path</strong></td>
</tr>
<tr>
<td><strong>Option -104 Path</strong></td>
</tr>
<tr>
<td><strong>Option -105 Path</strong></td>
</tr>
<tr>
<td><strong>Lowest Power</strong></td>
</tr>
<tr>
<td><strong>Lowest Price</strong></td>
</tr>
</tbody>
</table>
Model 52610 is a member of the Cobalt™ family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 52610 includes a general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 52610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 52610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -105 provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

---

**Features**

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAs
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt and Onyx VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Option -104 LVDS FPGA I/O to VPX P1 or P2
Option -105 Gigabit serial FPGA I/O

Ordering Information

Model Description
52610 LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T
-064 XC6VSX315T
-104 LVDS FPGA I/O to VPX P1 or P2
-105 Gigabit serial FPGA I/O to VPX P1 or P2
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

VPX Development System
See 8267 Datasheet for Options

LVDS Digital I/O with Virtex-6 FPGA - 3U VPX

 Acquisition IP Module

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 52610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Module

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

PCI Express Interface

The Model 52610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 52610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM.

Specifications

Front Panel Input/Output

Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
Clock: One LVDS differential pair, 2.5 V compliant
Data Valid: One LVDS differential pair, 2.5 V compliant
Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array

Standard: Xilinx Virtex-6 XC6VLX315T
Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O

Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Option -105: Provides one 8X or two 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Memory

Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-Express Interface

PCI Express Bus: Gen. 1: x4

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.
General Information

Models 57610 and 58610 are members of the Cobalt® family of high-performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71610 XMC modules mounted on a VPX carrier board.

Model 57610 is a 6U board with one Model 71610 module while the Model 58610 is a 6U board with two XMC modules rather than one.

These models include one or two general-purpose connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The factory-installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, controllers for all data clocking, test signal generators, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610.

Option -105 supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 58610.

Features

- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3
- PCI Express (Gen. 1 & 2) interface up to x8
- Optional user-configurable gigabit serial interface
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
- Ruggedized and conduction-cooled versions available

New! New! New! New! New!

32 or 64 bits of LVDS digital I/O
One or two LVDS clocks
One or two LVDS data valid
One or two LVDS data suspend
Supports LXT and SXT Virtex-6 FPGAS
One or two DMA controllers move data to and from system memory
Up to 2 or 4 GB of DDR3
PCI Express (Gen. 1 & 2) interface up to x8
Optional user-configurable gigabit serial interface
Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
Ruggedized and conduction-cooled versions available
**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57610</td>
<td>Single LVDS Digital I/O with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58610</td>
<td>Dual LVDS Digital I/O with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**
- 062 XC6VLX240T
- 064 XC6VSX315T
- 104 LVDS I/O between the FPGA and P3 connector, Model 57610; P3 and P5 connectors, Model 58610
- 105 Gigabit link between the FPGA and P2 connector, Model 57610; gigabit links from each FPGA to P2 connector, Model 78610
- 155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

**Model 57610 and 58610**

**Specifications**

**Memory Resources**

The hardware architecture supports up to four or eight independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 4 GB.

**Front Panel Input/Output (1 or 2)**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Custom I/O**

**Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57610; P3 and P5, Model 58610
**Option -105:** Supports serial protocols by providing a 4X gigabit link between the FPGA and VPX P2, Model 57610; or one 4X link from each FPGA to P2 and an additional 4X link between the FPGAs, Model 85610

**Memory Banks (1 or 2)**

**Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
**Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**PCI Express Interface**

**PCI Express Bus:** Gen. 1 or 2: x4 or x8
**Environmental:** Level L1 & L2 air-cooled;
Level L3 ruggedized, conduction-cooled
**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Models 72610, 73610 and 74610 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71610 XMC modules mounted on a cPCI carrier board.

Model 72610 is a 6U cPCI board while the Model 73610 is a 3U cPCI board; both are equipped with one Model 71610 XMC. Model 74610 is a 6U cPCI board with two XMC modules rather than one.

These models include one or two general-purpose connectors for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The factory-installed functions of these models include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, controllers for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610.

Features

- 32 or 64 bits of LVDS digital I/O
- One or two LVDS clocks
- One or two LVDS data valid
- One or two LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- One or two DMA controllers move data to and from system memory
- Up to 2 or 4 GB of DDR3 SDRAM
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board

Block Diagram, Model 72610

Model 74610 doubles all resources except the PCI-to-PCI Bridge

<table>
<thead>
<tr>
<th>MODEL 73610 INTERFACES ONLY</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>VIRTEx-6 FPGA</strong></td>
</tr>
<tr>
<td>LDVS</td>
</tr>
<tr>
<td>PCIe</td>
</tr>
<tr>
<td>32-bit, 33/66 MHz</td>
</tr>
<tr>
<td>Optional FPGA I/O (Option-104)</td>
</tr>
<tr>
<td>PCI/PCI-X BUS</td>
</tr>
<tr>
<td>32-bit, 33/66 MHz</td>
</tr>
<tr>
<td>PCIe-to-PCI Bridge</td>
</tr>
<tr>
<td>PCIe</td>
</tr>
<tr>
<td>32-bit, 33/66 MHz</td>
</tr>
<tr>
<td>Optional FPGA I/O (Option-104)</td>
</tr>
<tr>
<td>From/To Other XMC Module of MODEL 74610</td>
</tr>
<tr>
<td>PCIe</td>
</tr>
<tr>
<td>32-bit, 33/66 MHz</td>
</tr>
</tbody>
</table>
Single or Dual LVDS Digital I/O with Virtex-6 FPGA - cPCI

➤ Acquisition IP Module
These models can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that these models are no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

Generation IP Module
These models can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

PCI-X Interface
These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73610: 32 bits only.

Memory Resources
The hardware architecture supports up to four or eight independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM for Models 72610 and 73610 or a total of 4 GB for Model 74610.

Specifications
Model 72610 or Model 73610: Single LVDS Digital I/O
Model 74610: Dual LVDS Digital I/O

Front Panel Input/Output (1 or 2)
- Data Lines: 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- Clock: One LVDS differential pair, 2.5 V compliant
- Data Valid: One LVDS differential pair, 2.5 V compliant
- Data Suspend: One LVDS differential pair, 2.5 V compliant

Field Programmable Gate Array (1 or 2)
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

Custom I/O
- Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610

Memory Banks (1 or 2)
- Standard: Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- Option 165: Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

PCI-X Interface
- PCI-X Bus: 32 or 64 bits at 33 or 66 MHz

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Standard 6U or 3U cPCI board

Ordering Information

Model Description
72610 Single LVDS Digital I/O with Virtex-6 FPGA - 6U cPCI
73610 Single LVDS Digital I/O with Virtex-6 FPGA - 3U cPCI
74610 Dual LVDS Digital I/O with Virtex-6 FPGAs - 6U cPCI

Options:
- -062 XC6VLX240T
- -064 XC6VSX315T
- -104 LVDS I/O between the FPGA and J2 connector, Model 73610; J3 connector, Model 72610; J3 and J5 connectors, Model 74610
- -155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required
**General Information**

Model 56610 is a member of the Cobalt® family of high-performance AMC boards based on the Xilinx Virtex-6 FPGA. This digital I/O board provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to supporting PCI Express Gen. 1 as a native interface, the Model 56610 includes a general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions for data flow and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an IP (intellectual property) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s interface. The 56610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T, or SX315T. The SXT part features up to 1344 DSP48E slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, one of the lower-cost LXT FPGAs can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.

---

**Features**

- 32 bits of LVDS digital I/O
- One LVDS clock
- One LVDS data valid
- One LVDS data suspend
- Supports LXT and SXT Virtex-6 FPGAS
- DMA controller moves data to and from system memory
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface
- AMC.1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O to the carrier board
**Model 56610**

**LVDS Digital I/O with Virtex-6 FPGA - AMC**

➤ **Acquisition IP Module**

The board can be configured for digital input mode by the setting of a jumper. In this case, the board accepts input data Clock and input data Valid signals. This supports a continuous input Clock with data accepted only when the Data Valid line is true. The board can optionally generate a Data Suspend output signal indicating that the 56610 is no longer capable of accepting data. The board accepts 32 bits from the front panel connector or from an on-board test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. Memory banks are supported with DMA engines for easily moving input data through the PCIe interface.

**Generation IP Module**

The board can be configured for digital output mode by the setting of a jumper. In this case, the board generates output data Clock and output Data Valid signals. This supports a continuous output Clock with data valid only when the Data Valid line is true. The board can optionally accept a Data Suspend input signal to halt data generation when the destination device is no longer capable of accepting data.

A linked-list controller allows users to generate 32-bit digital words out through the front panel LVDS connector from tables stored in either on-board or off-board host memory. Parameters including length of table, delay from software trigger, table repetition, etc. can be programmed for entry. Up to 64 individual link entries can be chained together to create complex output patterns with minimum programming.

**AMC Interface**

The Model 56610 complies with the AMC specification by providing an x8 PCIe connection to AdvancedTCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

**PCI Express Interface**

The Model 56610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Memory Resources**

The 56610 hardware architecture supports up to four independent 512 MB memory banks of DDR3 SDRAM. The board is always configured with 1 GB of memory (Banks 1 and 2).

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes. For customers who need more memory to support their IP, Banks 3 and 4 can be optionally added for a total of 2 GB of DDR3 SDRAM

**Ordering Information**

**Model Description**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>56610</td>
<td>LVDS Digital I/O with Virtex-6 FPGA - PCIe</td>
</tr>
</tbody>
</table>

**Options:**

-062  XC6VLX240T
-064  XC6VSX315T
-104  LVDS FPGA I/O through 68-pin ribbon cable connector
-105  Gigabit serial FPGA I/O through two 4X top edge connectors
-155* Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165  Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)

* This option is always required

**Contact Pentek for availability of rugged and conduction-cooled versions**

---

**Specifications**

**Front Panel Input/Output**

- **Data Lines:** 35 LVDS differential pairs (32 pairs supported in factory-installed functions), 2.5 V compliant
- **Clock:** One LVDS differential pair, 2.5 V compliant
- **Data Valid:** One LVDS differential pair, 2.5 V compliant
- **Data Suspend:** One LVDS differential pair, 2.5 V compliant

**Field Programmable Gate Array**

- **Standard:** Xilinx Virtex-6 XC6VLX130T
- **Optional:** Xilinx Virtex-6 XC6VLX240T, or XC6VSX315T

**Custom I/O**

- **Option -104:** Installs a front panel connector with 20 LVDS pairs to the FPGA

**Memory**

- **Standard:** Two 512 MB DDR3 SDRAM memory banks (1 and 2), 400 MHz DDR
- **Option 165:** Two 512 MB DDR3 SDRAM memory banks (3 and 4), 400 MHz DDR

**AMC Interface**

- **Type:** AMC.1
- **Module Management:** IPMI Version 2.0

**PCI-Express Interface**

- **PCI Express Bus:** Gen. 1: x4 or x8

**Environmental**

- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.
Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

Model 7811

**General Information**

Model 7811 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 7811 serves as a flexible platform for developing and deploying custom FPGA processing IP.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 7811 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized function, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA can be populated with two different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX130T, LX240T or SX315T. The SX315T part features 1,344 DSP48E slices and is ideal for modulation/demodulation, encoding/decryption, and channelization of the signals between transmission and reception.

For applications not requiring large DSP resources, the lower-cost LX130T FPGA can be installed.

---

**Features**

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fibre optic or copper serial interfaces
- PCI Express interface up to x8

---

**Specifications**

<table>
<thead>
<tr>
<th>CH 1</th>
<th>CH 2</th>
<th>CH 3</th>
<th>CH 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>RX_TX</td>
<td>RX_TX</td>
<td>RX_TX</td>
<td>RX_TX</td>
</tr>
<tr>
<td>FIBER OPTIC or COPPER INTERFACE</td>
<td>FIBER OPTIC or COPPER INTERFACE</td>
<td>FIBER OPTIC or COPPER INTERFACE</td>
<td>FIBER OPTIC or COPPER INTERFACE</td>
</tr>
</tbody>
</table>

**VIRTEX-6 FPGA**

LX130T, LX240T or SX315T

---

**Config FLASH**

16 MB

---

**GTX**

8X

x8 PCIe

PCIe
Model 7811

Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

➤ Serial FPDP Interface

The 7811 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces or copper interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

PCI Express Interface

The Model 7811 includes an industry-standard interface fully compliant with PCI Express bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs
- Number of Connectors: 4
- Fiber Optic Connector Type: LC
  - Laser: 850 nm (standard, other options available)
- Copper Connector Type: SFP+
  - Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array
- Standard: Xilinx Virtex-6 XC6VLX130T
- Optional: Xilinx Virtex-6 XC6VLX240T

PCI-Express Interface
- PCI Express Bus: Gen. 1: x4 or x8

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

Model 8266

PC Development System See 8266 Datasheet for Options

Options:
- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 280 Copper serial interfaces
- 281 Multi-mode optical serial interfaces
General Information
Model 71611 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture
The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 71611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA
The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs the P14 PMC connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
Quad Serial FPDP Interface with Virtex-6 FPGA - XMC

Model 71611

➤ Serial FPDP Interface

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 71611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 71611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the module.

Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Copper Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port
Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T
Custom I/O
Option -104: Installs the PMC P14 connector with 20 LVDS pairs to the FPGA
Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
PCI Express Bus: Gen. 1: x4 or x8
Environmental
Operating Temp: 0° to 50° C
Storage Temp: –20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Standard XMC module, 2.91 in. x 5.87 in.

Ordering Information

Model Description
71611 Quad Serial FPDP Interface with Virtex-6 FPGA - XMC
Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O through P14 connector
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8266 PC Development System See 8266 Datasheet for Options
Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe

**General Information**

Model 78611 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 78611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 78611 includes a general purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 78611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

---

**Features**

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O
**Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe**

**Serial FPDP Interface**

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

**Memory Resources**

The 78611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

The Model 78611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

---

**Specifications**

**Front Panel Serial FPDP Inputs/Outputs**

- Number of Connectors: 4
- Fiber Optic Connector Type: LC
- Laser: 850 nm (standard, other options available)
- Copper Connector Type: Micro Twinax
- Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

**Field Programmable Gate Array:** Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

**Custom I/O**

- Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

**Memory**

- Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- Option 280: Copper serial interfaces
- Option 281: Multi-mode optical serial interfaces

---

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe</td>
</tr>
<tr>
<td></td>
<td><strong>Options:</strong></td>
</tr>
<tr>
<td>-062</td>
<td>XC6VLX240T FPGA</td>
</tr>
<tr>
<td>-064</td>
<td>XC6VSX315T FPGA</td>
</tr>
<tr>
<td>-065</td>
<td>XC6VSX475T FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O through 68-pin ribbon cable connector</td>
</tr>
<tr>
<td>-155</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)</td>
</tr>
<tr>
<td>-165</td>
<td>Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)</td>
</tr>
<tr>
<td>-280</td>
<td>Copper serial interfaces</td>
</tr>
<tr>
<td>-281</td>
<td>Multi-mode optical serial interfaces</td>
</tr>
</tbody>
</table>

- Model 8266: PC Development System
  - See 8266 Datasheet for Options

---

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe

General Information

Model 78611 is a member of the Cobalt® family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 78611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 78611 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 78611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Features

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x8
- LVDS connections to the Virtex-6 FPGA for custom I/O

Memory Banks1 & 2 DDR3 option 155
Memory Banks 3 & 4 DDR3 option 165
Config FLASH 64 MB
Option -104

GTX
LVDS

Optional FPGA GPIO
68-pin Header
x8 PCIe
x8 PCI Express
Model 78611

Quad Serial FPDP Interface with Virtex-6 FPGA - x8 PCIe

➤ Serial FPDP Interface

The 78611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 78611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 78611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Specifications

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: Connects 20 pairs of LVDS signals from the FPGA on PMC P14 to a 68-pin DIL ribbon-cable header on the PCIe board for custom I/O.

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR PCI-Express Interface

PCI Express Bus: Gen. 1: x4 or x8

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.
Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model | Description
--- | ---
78611 | Quad Serial FPDP Interface with Virtex-6 FPGA - PCIe

Options:

-062 | XC6VLX240T FPGA
-064 | XC6VSX315T FPGA
-065 | XC6VSX475T FPGA
-104 | LVDS FPGA I/O through 68-pin ribbon cable connector
-155 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 | Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 | Copper serial interfaces
-281 | Multi-mode optical serial interfaces

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

General Information

Model 53611 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 53611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express over the 3U VPX backplane, the Model 53611 includes a general purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 53611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.
Serial FPDP Interface

The 53611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 53611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 53611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Crossbar Switch

The 53611 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Programmable signal input equalization and output pre-emphasis settings enable optimization. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4
Fiber Optic Connector Type: LC
   Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port
Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T
Custom I/O
   Option -104: Provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
Memory
   Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR
PCI-Express Interface
   PCI Express Bus: Gen. 1: x4 or x8
Environmental
   Operating Temp: 0° to 50° C
   Storage Temp: -20° to 90° C
   Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 53xxx and the 52xxx. For more information on a 52xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Ordering Information

Model 53611
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O to VPX P2
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267
VPX Development System
See 8267 Datasheet for Options

Model 8267
The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Model 52611

Model 52611 COTS (left) and rugged version

General Information

Model 52611 is a member of the Cobalt® family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 52611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 52611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express over the 3U VPX backplane, the Model 52611 includes a general-purpose connector for application-specific I/O.

The Cobalt Architecture

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 52611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Features

- Complete Serial FPDP solution
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- Up to 2 GB of DDR3 SDRAM
- PCI Express interface up to x4
- LVDS connections to the Virtex-6 FPGA for custom I/O
- 3U VPX form factor provides a compact, rugged platform
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
PCl Express Interface

The Model 52611 includes an industry-standard interface fully compliant with PCl Express Gen. 1 bus specifications. Supporting PCIe links up to x4, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the board.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system for Pentek Cobalt, Onyx and integrated development system versions.

Ordering Information

Model 52611 Quad Serial FPDP Interface with Virtex-6 FPGA - 3U VPX

Options:
- 062 XC6VLX240T FPGA
- 064 XC6VSX315T FPGA
- 065 XC6VSX475T FPGA
- 104 LVDS FPGA I/O to VPX P2
- 155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- 165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- 280 Copper serial interfaces
- 281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267 VPX Development System

See 8267 Datasheet for Options

Specifications

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4
Fiber Optic Connector Type: LC Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Serial FPDP Interface

The 52611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 52611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Environmental

Operating Temp: 0° to 50°C
Storage Temp: -20° to 90°C
Relative Humidity: 0 to 95%, non-cond.
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their main features.

VPX Family Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>52xxx</th>
<th>53xxx</th>
</tr>
</thead>
<tbody>
<tr>
<td>Form Factor</td>
<td>3U VPX</td>
<td></td>
</tr>
<tr>
<td># of XMCs</td>
<td>One XMC</td>
<td></td>
</tr>
<tr>
<td>Crossbar Switch</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>PCIe path</td>
<td>VPX P1, VPX P1 or P2</td>
<td></td>
</tr>
<tr>
<td>PCIe width</td>
<td>x4, x8</td>
<td></td>
</tr>
<tr>
<td>Option -104 path</td>
<td>20 pairs on VPX P2</td>
<td></td>
</tr>
<tr>
<td>Option -105 path</td>
<td>Two x4 or one x8 on VPX P1</td>
<td>Two x4 or one x8 on VPX P1</td>
</tr>
<tr>
<td>Lowest Power</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Lowest Price</td>
<td>Yes</td>
<td>No</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions.

Pentek, Inc. One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com

www.pentek.com
General Information

Models 57611 and 58611 are members of the Cobalt family of high performance 6U OpenVPX boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71611 XMC modules mounted on a VPX carrier board.

Model 57611 is a 6U board with one Model 71611 module while the Model 58611 is a 6U board with two XMC modules rather than one.

These models are fully compatible with the VITA 17.1 Serial FPDP specification. Their built-in data transfer features make them complete turnkey solutions. For users who require application-specific functions, they serve as flexible platforms for developing and deploying custom FPGA processing IP.

The Cobalt Architecture

The Pentek Cobalt Architecture features one or two Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-6 FPGA

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611.

Features

- Four or eight channels of Serial FPDP interface
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- One or two Virtex-6 FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM
- PCI Express interface up to x8
- Optional LVDS connections to the Virtex-6 FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Block Diagram, Model 57611.
Model 58611 doubles all resources except the PCIe-to-PCIe Switch and provides 20 LVDS pairs from the 2nd FPGA to VPX-P5
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - 6U OpenVPX

**Model 8264**

The Model 8264 is a fully-integrated development system for Pentek Cobalt and Onyx 6U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Memory Resources**

The architecture supports up to four or eight independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

**PCI Express Interface**

These models include an industry-standard interface fully compliant with PCI Express Gen. 1 and 2 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**Specifications**

**Front Panel Serial FPDP Inputs/Outputs**

- Number of Connectors: 4 or 8
- Fiber Optic Connector Type: LC
- Laser: 850 nm (standard, other options available)
- Copper Connector Type: Micro Twinax
- Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
- Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

**Field Programmable Gate Arrays:** Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

**Custom I/O**

- **Option -104:** Provides 20 LVDS pairs between the FPGA and the VPX P3 connector, Model 57611; P3 and P5, Model 58611

**Memory**

- **Option 155 or 165:** Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

**Environmental:** Level L1 & L2 air-cooled; Level L3 ruggedized, conduction-cooled

**Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 6U VPX</td>
</tr>
<tr>
<td>58611</td>
<td>Octal Serial FPDP Interface with two Virtex-6 FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

**Options:**

- -062 XC6VLX240T FPGA
- -064 XC6VSX315T FPGA
- -065 XC6VSX475T FPGA
- -104 LVDS I/O between the FPGA and P3 connector, Model 57611; P3 and P5, Model 58611
- -155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
- -165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
- -280 Copper serial interfaces
- -281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions.

**Model 8264**

VPX Development System. See 8264 Datasheet for Details.
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - cPCI

**General Information**

Models 72611, 73611 and 74611 are members of the Cobalt® family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71611 XMC modules mounted on a cPCI carrier board.

Model 72611 is a 6U cPCI board while the Model 73611 is a 3U cPCI board; both are equipped with one Model 71611 XMC. Model 74611 is a 6U cPCI board with two XMC modules rather than one.

These models are fully compatible with the VITA 17.1 Serial FPDP specification. Their built-in data transfer features make them complete turnkey solutions. For users who require application-specific functions, they serve as flexible platforms for developing and deploying custom FPGA processing IP.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features one or two Virtex-6 FPGAs. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a cPCI interface complete the factory-installed functions and enable these models to operate as a complete turnkey solutions without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611.

---

**Features**

- Four or eight channels of Serial FPDP interface
- Fully compliant with VITA 17.1 specification
- Fiber optic or copper serial interfaces
- One or two Virtex-6 FPGAs
- Up to 2 or 4 GB of DDR3 SDRAM
- LVDS connections to the Virtex-6 FPGA for custom I/O

---

**Block Diagram, Model 72611**

Model 74611 doubles all resources except the PCI-to-PCI Bridge
Quad or Octal Serial FPDP Interface with Virtex-6 FPGA - cPCI

➤ Serial FPDP Interface

These models are fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the boards can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The architecture supports up to four or eight independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits (32 bits only, Model 73611) and data rates of 33 and 66 MHz are supported.

Specifications

Front Panel Serial FPDP Inputs/Outputs

Number of Connectors: 4 or 8
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)

Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)

Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O

Option -104: provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611

Memory

Option 155 or 165: Two 512 MB DDR3 SDRAM memory banks, 400 MHz DDR

PCI-X Interface

PCI-X Bus: 32- or 64-bit at 33 or 66 MHz
Model 73611: 32-bit at 33 or 66 MHz

Environmental

Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-cond.

Size: Standard 6U or 3U cPCI board

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73611</td>
<td>Quad Serial FPDP Interface with Virtex-6 FPGA - 3U cPCI</td>
</tr>
<tr>
<td>74611</td>
<td>Octal Serial FPDP Interface with Virtex-6 FPGA - 6U cPCI</td>
</tr>
</tbody>
</table>

Options:

-062    XC6VLX240T FPGA
-064    XC6VSX315T FPGA
-065    XC6VSX475T FPGA
-104    LVDS I/O between the FPGA and J2 connector, Model 73611; J3 connector, Model 72611; J3 and J5 connectors, Model 74611
-155    Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165    Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280    Copper serial interfaces
-281    Multi-mode optical serial interfaces
Quad Serial FPDP Interface with Virtex-6 FPGA - AMC

**General Information**

Model 56611 is a member of the Cobalt® family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A multi-channel, gigabit serial interface, it is ideal for interfacing to Serial FPDP data converter boards or as a chassis-to-chassis data link.

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 56611 serves as a flexible platform for developing and deploying custom FPGA processing IP. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56611 includes a front panel general-purpose connector for application-specific I/O.

**The Cobalt Architecture**

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 56611 to operate as a complete turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

**Xilinx Virtex-6 FPGA**

The Virtex-6 FPGA site can be populated with a variety of different FPGAs to match the specific requirements of the processing task. Supported FPGAs include: LX240T, SX315T, or SX475T. The SXT parts feature up to 2016 DSP48E slices and are ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources, the lower-cost LXT FPGA can be installed.

Option -104 installs a front panel connector with 20 pairs of LVDS connections to the FPGA for custom I/O.
Model 56611

Quad Serial FPDP Interface with Virtex-6 FPGA - AMC

➤ Serial FPDP Interface

The 56611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop modes.

Memory Resources

The 56611 architecture supports up to four independent memory banks of DDR3 SDRAM. Each memory is 512 MB deep and an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

PCI Express Interface

The Model 56611 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting PCIe links up to x8, the interface includes eight DMA controllers. Each of the four Serial FPDP channels includes dedicated DMA engines for transmit and receive for efficient transfers to and from the module.

Specifications

Front Panel Serial FPDP Inputs/Outputs
Number of Connectors: 4
Fiber Optic Connector Type: LC
Laser: 850 nm (standard, other options available)
Copper Connector Type: Micro Twinax
Fiber Optic or Copper Link Rates: 1.0625, 2.125, 2.5, 3.125 or 4.25 Gbaud (copper rate depends on cable length)
Fiber Optic or Copper Data Transfer Rates: 105, 210, 247, 309 or 420 MB/sec (depending on link rate) per serial FPDP port

Field Programmable Gate Array: Xilinx
Virtex-6 XC6VLX240T, XC6VSX315T, or XC6VSX475T

Custom I/O
Option -104: Installs a front panel connector with 20 LVDS pairs to the FPGA

Memory
Option 155 or 165: Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
Option 280: Copper serial interfaces
Option 281: Multi-mode optical serial interfaces

Ordering Information

Model Description
56611 Quad Serial FPDP Interface with Virtex-6 FPGA - AMC
Options:
-062 XC6VLX240T FPGA
-064 XC6VSX315T FPGA
-065 XC6VSX475T FPGA
-104 LVDS FPGA I/O through front panel connector
-155 Two 512 MB DDR3 SDRAM Memory Banks (Banks 1 and 2)
-165 Two 512 MB DDR3 SDRAM Memory Banks (Banks 3 and 4)
-280 Copper serial interfaces
-281 Multi-mode optical serial interfaces

Contact Pentek for availability of rugged and conduction-cooled versions

Pentek, Inc.  One Park Way  •  Upper Saddle River  •  New Jersey 07458  Tel: 201-818-5900  •  Fax: 201-818-5904  •  Email: info@pentek.com  www.pentek.com
Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

General Information

Model 71141 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KL035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit D/As
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multimodule synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- VITA 42.0 XMC compatible with switched fabric interfaces
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Ruggedized and conduction-cooled versions available

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com
www.pentek.com
Model 71141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC

A/D Acquisition IP Module

The 7141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 71141 installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

➤ and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs the P14 PMC connector with 24 pairs of LVDS connections to the FPGA for custom I/O.

Option -105 installs the P16 XMC connector with 8X gigabit link to the FPGA to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, inter-polate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 7141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 7141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 7141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple modules to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7192 high-speed sync module can be used to drive the sync bus to synchronize multichannel systems. ➤
Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converters
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
- **Option -104:** Installs the PMC P14 connector with 24 LVDS pairs to the FPGA
- **Option -105 (only available with option -084 or -087):** Installs the XMC P16 connector configurable as one 8X gigabit serial link to the FPGA

Memory
- **Type:** DDR4 SDRAM
- **Size:** 5 GB
- **Speed:** 1200 MHz (2400 MHz DDR)

Environmental
- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** -20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** -20° to 65° C
  - **Storage Temp:** -40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -713:** L3 (conduction cooled)
  - **Operating Temp:** -40° to 70° C
  - **Storage Temp:** -50° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Size:** XMC module 2.910 in x 5.870 in (74.00 mm x 149.00 mm)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - XMC</td>
</tr>
</tbody>
</table>

Options:
- **-084** XCKU060-2 FPGA
- **-087** XCKU115-2 FPGA
- **-104** LVDS FPGA I/O through P14 connector
- **-105** Gigabit serial FPGA I/O through P16 connector
- **-702** Air cooled, Level L2
- **-713** Conduction-cooled, Level L3

Contact Pentek for complete specifications of rugged and conduction-cooled versions

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
General Information

Model 78141 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 78141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KL035 through KL115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

A/D Acquisition IP Module

The 78141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 78141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

A/D and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 78141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 78141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 78141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 7892 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
Model 78141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe

➤ Specifications

Front Panel Analog Signal Inputs
  - **Input Type:** Transformer-coupled, front panel female SSMC connectors

A/D Converter
  - **Type:** ADC12DJ3200
  - **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
  - **Resolution:** 12 bits

Input Bandwidth:
  - Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
  - **Type:** Texas Instruments DAC38RF82
  - **Output Sampling Rate:** 6.4 GHz.
  - **Resolution:** 14 bits

Sample Clock Source:
  - Front panel SSMC connector

Timing Bus:
  - 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
  - **Type:** Front panel female SSMC connector, LVTTL
  - **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
  - **Standard:** Xilinx Kintex UltraScale XCKU035-2
  - **Option -084:** Xilinx Kintex UltraScale XCKU060-2
  - **Option -087:** Xilinx Kintex UltraScale XCKU115-2

Custom I/O
  - **Option -104:** installs 24 pairs of LVDS connections from the FPGA to a 68-pin header for custom I/O
  - **Option -105 (only available with option -084 or -087):** provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols

Memory
  - **Type:** DDR4 SDRAM
  - **Size:** 5 GB
  - **Speed:** 1200 MHz (2400 MHz DDR)

PCI-Express Interface
  - **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
  - **Standard:** L0 (air cooled)
    - **Operating Temp:** 0° to 50° C
    - **Storage Temp:** -20° to 90° C
    - **Relative Humidity:** 0 to 95%, non-condensing
  - **Option -702:** L2 (air cooled)
    - **Operating Temp:** -20° to 65° C
    - **Storage Temp:** -40° to 100° C
    - **Relative Humidity:** 0 to 95%, non-condensing

Size:
  - PCIe card 4.380 in x 7.130 in (111.25 mm x 181.10 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>78141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - PCIe</td>
</tr>
</tbody>
</table>

Options:
- **084** XCKU060-2 FPGA
- **087** XCKU115-2 FPGA
- **104** LVDS FPGA I/O
- **105** Gigabit serial FPGA I/O
- **702** Air cooled, Level L2

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
Model 53141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

General Information

Model 53141 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 53141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/As and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 53141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 53141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multinode synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

The 53141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by the DMA engine need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 53141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/A waveforms stored in either on-board memory or off-board host memory.

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for serial and parallel interfaces.

Option -105 provides one 8x gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or routing to other module resources.

Digital Upconverter and D/A Stage

A Texas Instruments DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 53141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 53141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 53141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Fabric-Transparent Crossbar Switch
The 53161 features a unique high-speed switching configuration. A fabric-transparent crossbar switch bridges numerous interfaces and components on the board using gigabit serial data paths with no latency. Data paths can be selected as single (1X) lanes, or groups of four lanes (4X).

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML
External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS
Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -105 provides one 4X gigabit link between the FPGA and the VPX P1 connector to support serial protocols.

Memory
Type: DDR4 SDRAM
Size: 5 GB
Speed: 1200 MHz (2400 MHz DDR)
PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing
Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 3U VPX board 3.037 in. x 6.717 in. (100.0 mm x 170.6 mm)

Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

SPARK Development Systems

Ordering Information
Model Description
53141 1-Ch. 6.4 GHz or 2-Ch.
3.2 GHz A/D, 2-Ch.
6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
General Information

Model 52141 is a member of the Jade™ family of high-performance PCIe modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/A and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 52141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 52141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 52141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.
A/D Acquisition IP Module

The 52141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The Model 52141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 installs 24 pairs of LVDS connections from the FPA to a 68-pin header for custom I/O.

Option -105 provides one 8X gigabit link between the FPGA and a serial connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital down-converters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The 52141 architecture supports a 5 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

The Model 52141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

The 52141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PFS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5292 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits

Sample Clock Source: Front panel SSMC connector
Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

VPX Families

Pentek offers two families of 3U VPX products: the 52xxx and the 53xxx. For more information on a 53xxx product, please refer to the product datasheet. The table below provides a comparison of their many features.

<table>
<thead>
<tr>
<th>VPX Family Comparison</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>52xxx</strong></td>
</tr>
<tr>
<td>Form Factor</td>
</tr>
<tr>
<td># of XMCs</td>
</tr>
<tr>
<td>Crossbar Switch</td>
</tr>
<tr>
<td>PCIe path</td>
</tr>
<tr>
<td>PCIe width</td>
</tr>
<tr>
<td>Option -104 path</td>
</tr>
<tr>
<td>Option -105 path</td>
</tr>
<tr>
<td>Lowest Power</td>
</tr>
<tr>
<td>Lowest Price</td>
</tr>
</tbody>
</table>

Ordering Information

Model | Description
--- | ---
52141 | 1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 3U VPX

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.
General Information

Models 57141 and 58141 are members of the Jade™ family of high-performance 6U VPX boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a VPX carrier board. Model 57141 is a 6U board with one Model 71141 module while the Model 58141 is a 6U board with two XMC modules rather than one.

They include two or four A/DS, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. In addition to supporting PCI Express Gen. 3 as a native interface, these models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include two or four A/D acquisition and two or four D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM, controllers for all data clocking and synchronization functions, one or two test signal generators and a PCIe interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One or two-channel mode with 6.4 GHz, 12-bit A/DS
- Two- or four-channel mode with 3.2 GHz, 12-bit A/DS
- Programmable DDCs (Digital Downconverters)
- Two or four-Channel 6.4 GHz, 14-bit D/As
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/A's waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.

Option -105 provides two 4x gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

A/D Converter Stage

The front end accepts analog HF or IF inputs on front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

Digital Upconverter and D/A Stage

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

Memory Resources

The architecture supports 5 or 10 GB bank of DDR4 SDRAM memory.

User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA can take advantage of the memory for custom applications.

PCI Express Interface

These models include an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Clocking and Synchronization

These models accept a sample clock via front panel SSMC connectors. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
Models 57141 & 58141

1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - 6U VPX

➤ for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5792 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.

Specifications
Model 57141 One A/D
Model 58141 Two A/Ds
Front Panel Analog Signal Inputs (2 or 4)
Input Type: Transformer-coupled, front panel female SSMC connectors
A/D Converters (1 or 2)
Type: ADC12DJ3200
Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
Resolution: 12 bits
Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz
D/A Converters (2 or 4)
Type: Texas Instruments DAC38RF82
Output Sampling Rate: 6.4 GHz.
Resolution: 14 bits
Sample Clock Source (1 or 2)
Front panel SSMC connector
Timing Bus (1 or 2)
19-pin µSync bus connector includes sync and gate/trigger inputs, CML.
External Trigger Input (1 or 2)
Type: Front panel female SSMC connector, LVTTL
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Arrays (1 or 2)
Standard: Xilinx Kintex UltraScale XCKU035-2
Option -084: Xilinx Kintex UltraScale XCKU060-2
Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O
Option -104 provides 24 pairs of LVDS connections between the FPGA and the VPX P3 connector, Model 57141; P3 and P5 connectors, Model 58141.
Option -105 provides two 4X gigabit links between the FPGA and the VPX P2 connector to support serial protocols.

Memory (1 or 2)
Type: DDR4 SDRAM
Size: 5 or 10 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing
Size: 6U Board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PC rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information
Model 57141

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>57141</td>
<td>1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - 6U VPX</td>
</tr>
<tr>
<td>58141</td>
<td>2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, 4-Ch. 6.4 GHz D/A, 2 8a. Ultra-Scale FPGAs - 6U VPX</td>
</tr>
</tbody>
</table>

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 105 Gigabit serial FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458
Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com
1 or 2-Ch. 6.4 GHz, or 2 or 4-Ch. 3.2 GHz A/D, 2 or 4-Ch. 6.4 GHz D/A, 1 or 2 Kintex UltraScale FPGAs - cPCI

General Information

Models 72141, 73141 and 74141 are members of the Jade family of high-performance cPCI boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71141 XMC modules mounted on a cPCI carrier board. Model 72141 is a 6U cPCI board while the Model 73141 is a 3U cPCI board; both are equipped with one Model 71141 XMC. Model 74141 is a 6U cPCI board with two XMC modules rather than one. They include two or four A/Ds, complete multiboard clock and sync sections, large DDR4 memories, two or four DDCs, two or four DUCs and two or four D/As. These models include optional high-bandwidth connections to the Kintex UltraScale FPGAs for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions include two or four A/D acquisition IP modules.

Each of the acquisition IP modules contains a programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCI-X interface complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications, thereby saving the cost and time of custom IP development.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115.
A/D Acquisition IP Module

These models feature two or four A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP modules have associated 5 or 10 GB of DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

These models support factory-installed functions which include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the D/A's waveforms stored in either on-board memory or off-board host memory.

Clocking and Synchronization

These models accept a 1.8 GHz dual-edge sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. Two units can be synchronized with a simple cable. For larger systems, multiple units can be synchronized using the Model 7292 high-speed sync boards to drive the sync bus.

Memory Resources

The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core(s) within the FPGA(s) can take advantage of the memory for custom applications.

PCI-X Interface

These models include an industry-standard interface fully compliant with PCI-X bus specifications. The interface includes multiple DMA controllers for efficient transfers to and from the board. Data widths of 32 or 64 bits and data rates of 33 and 66 MHz are supported. Model 73141: 32 bits only.

Pentek, Inc.  One Park Way ● Upper Saddle River ● New Jersey 07458  Tel: 201 818-5900 ● Fax: 201 818-5904 ● Email: info@pentek.com  www.pentek.com
### Specifications

**Model 72141 or Model 73141:**
- Two A/Ds

**Model 74141:**
- Four A/Ds
- Two D/A
- Four D/A

**Front Panel Analog Signal Inputs (2 or 4):**
- **Input Type:** Transformer-coupled, front panel female SSMC connectors

**A/D Converter (2 or 4):**
- **Type:** ADC12DJ3200
- **Sampling Rate:** Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz
- **Resolution:** 12 bits
- **Input Bandwidth:** Single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

**D/A Converters (2 or 4):**
- **Type:** Texas Instruments DAC38RF82
- **Output Sampling Rate:** 6.4 GHz.
- **Resolution:** 14 bits

**Sample Clock Source (1 or 2):**
- Front panel SSMC connector

**Timing Bus (1 or 2):**
- 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

**External Trigger Input (1 or 2):**
- **Type:** Front panel female SSMC connector, LVTTL
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Field Programmable Gate Array (1 or 2):**
- **Standard:** Xilinx Kintex UltraScale XCKU035-2
- **Option -084:** Xilinx Kintex UltraScale XCKU060-2
- **Option -087:** Xilinx Kintex UltraScale XCKU115-2

**Custom I/O**
- **Option -104:** Provides 20 LVDS pairs between the FPGA and the J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74141

**Memory (1 or 2):**
- **Type:** DDR4 SDRAM
- **Size:** GB
- **Speed:** 1200 MHz (2400 MHz DDR)

**PCI-X Interface**
- **PCI-X Bus:** 32 or 64 bits at 33 or 66 MHz
- Model 73141: 32 bits only

**Environmental**
- **Standard:** L0 (air cooled)
  - **Operating Temp:** 0° to 50° C
  - **Storage Temp:** –20° to 90° C
  - **Relative Humidity:** 0 to 95%, non-condensing
- **Option -702:** L2 (air cooled)
  - **Operating Temp:** –20° to 65° C
  - **Storage Temp:** –40° to 100° C
  - **Relative Humidity:** 0 to 95%, non-condensing

**Size:**
- 6U board 9.187 in x 6.717 in (233.3 mm x 170.6 mm)
- 3U board 3.937 in. x 6.717 in. (100.00 mm x 170.61 mm)

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>72141</td>
<td>1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI</td>
</tr>
<tr>
<td>73141</td>
<td>1 or 2-Ch. 6.4 GHz or 2 or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and one Kintex UltraScale FPGA - 6U cPCI</td>
</tr>
<tr>
<td>74141</td>
<td>2-Ch. 6.4 GHz or 4-Ch. 3.2 GHz A/D, with 2 or 4-Ch. 6.4 GHz D/A and two Kintex UltraScale FPGAs - 6U cPCI</td>
</tr>
</tbody>
</table>

**Options:**
- **-084** XCKU060-2 FPGA
- **-087** XCKU115-2 FPGA
- **-104** LVDS I/O between the FPGA and J2 connector, Model 73141; J3 connector, Model 72141; J3 and J5 connectors, Model 74841
- **-702** Air cooled, Level L2
Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A,
Kintex UltraScale FPGA - AMC

General Information

Model 56141 is a member of the Jade™ family of high-performance AMC boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek’s new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 56141 is a high-speed analog-to-digital and digital-to-analog converter with programmable DDCs (digital downconverters) and DUCs (digital upconverters). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and generator features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 6.4 GHz, 12-bit A/D converter, dual 6.4 GHz, 14-bit D/A and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 56141 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The Jade Architecture

Evolved from the proven designs of the Pentek Cobalt and Onyx families, Jade raises the processing performance with the new flagship family of Kintex UltraScale FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Jade architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 56141 factory-installed functions include two A/D acquisition and two D/A waveform generator IP modules. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 56141 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek Navigator FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The Kintex UltraScale FPGA site can be populated with a range of FPGAs to match the specific requirements of the processing task, spanning the KU035 through KU115. The KU115 features 5520 DSP48E2 slices.

Features

- Ideal radar and software radio interface solution
- Supports Xilinx Kintex UltraScale FPGAs
- One-channel mode with 6.4 GHz, 12-bit A/D
- Two-channel mode with 3.2 GHz, 12-bit A/Ds
- Programmable DDCs (Digital Downconverters)
- Two 6.4 GHz, 14-bit D/A
- Programmable DUCs (Digital Upconverters)
- 5 GB of DDR4 SDRAM
- µSync clock/sync bus for multiboard synchronization
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional LVDS and gigabit serial connections to the FPGA for custom I/O
- AMC 1 compliant
- IPMI 2.0 compliant MMC (Module Management Controller)
- Ruggedized and conduction-cooled versions available

Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458
Tel: 201 818-5900  Fax: 201 818-5904  Email: info@pentek.com
www.pentek.com
**A/D Acquisition IP Module**

The Model 56141 features two A/D Acquisition IP Modules for easy capture and data moving. The IP module can receive data from the A/D, or a test signal generator. The IP module has associated a 5 GB DDR4 memory for buffering data in FIFO mode or for storing data in transient capture mode.

In single-channel mode, all of 5 GB are used to store the single-channel of input data. In dual-channel mode, one half of the memory stores data from input channel 1 and the other half stores data from input channel 2. In both modes, continuous, full-rate transient capture of 12-bit data is supported.

The memory bank is supported with a DMA engine for moving A/D data through the PCIe interface. This powerful linked-list DMA engine is capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Generator IP Module**

The Model 56141 factory-installed functions include a sophisticated D/A Waveform Generator IP module. It allows users to easily record to the dual D/As waveforms stored in either on-board memory or off-board host memory.

and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, a lower-cost FPGA can be installed.

Option -104 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

**A/D Converter Stage**

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer-coupling into a Texas Instruments ADC12DJ3200 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 6.4 GHz and an input bandwidth of 7.9 GHz; or, in dual-channel mode with a sampling rate of 3.2 GHz and input bandwidth of 8.1 GHz.

The A/D’s built-in digital downconverters support 2x decimation in real output mode and 4x, 8x, or 16x decimation in complex output mode. The A/D digital outputs are delivered into the Kintex UltraScale FPGA for signal processing, data capture or for routing to other module resources.

**Digital Upconverter and D/A Stage**

A TI DAC38RF82 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconverter, interpolate and dual D/A stages. When operating as a DUC, it interpolates and translates real or complex baseband input signals. It delivers real or quadrature (I+Q) analog outputs to the dual 14-bit D/A converter. Analog output is through a pair of front panel SSMC connectors.

If translation is disabled, the DAC38RF82 acts as a dual interpolating 14-bit D/A. In both modes, the DAC38RF82 provides interpolation factors from 1x to 24x.

**Memory Resources**

The 56141 architecture supports a 5 GB bank of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

**PCI Express Interface**

The Model 56141 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x4, the interface includes multiple DMA controllers for efficient transfers to and from the module.

**Clocking and Synchronization**

The 56141 accepts a sample clock via a front panel SSMC connector. A second front panel SSMC accepts a TTL signal that can function as Gate, PPS or Sync.

A front panel µSync bus connector allows multiple boards to be synchronized, ideal for multichannel systems. The µSync bus includes gate, reset, and in and out reference clock signals. The Model 5692 high-speed sync board can be used to drive the sync bus to synchronize multichannel systems.
Model 56141

1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

➤ AMC Interface

The Model 56141 complies with the AMC1 specification by providing an x8 PCIe connection to Advanced TCA carriers or µTCA chassis. Module management is provided by an IPMI 2.0 MMC (Module Management Controller).

Specifications

Front Panel Analog Signal Inputs

Input Type: Transformer-coupled, front panel female SSMC connectors

A/D Converter

Type: ADC12DJ3200

Sampling Rate: Single-channel mode: 6.4 GHz; dual-channel mode: 3.2 GHz

Resolution: 12 bits

Input Bandwidth: single-channel mode: 7.9 GHz; dual-channel mode: 8.1 GHz

D/A Converters

Type: Texas Instruments DAC38RF82

Output Sampling Rate: 6.4 GHz.

Resolution: 14 bits

Sample Clock Source: Front panel SSMC connector

Timing Bus: 19-pin µSync bus connector includes sync and gate/trigger inputs, CML

External Trigger Input

Type: Front panel female SSMC connector, LVTTL

Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU035-2

Option -084: Xilinx Kintex UltraScale XCKU060-2

Option -087: Xilinx Kintex UltraScale XCKU115-2

Custom I/O

Option -014 provides 24 pairs of LVDS connections between the FPGA and a front-panel connector for custom I/O.

Memory

Type: DDR4 SDRAM

Size: 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -713: L3 (conduction cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Size: Single-width, full-height AMC module 2.890 in x 7.110 in (73.40 mm x 180.60 mm)

Note: Not all combinations of sample rates, decimations and interpolations are available due to JESD204B and PCIe rate limitations.

Ordering Information

Model  Description
56141  1-Ch. 6.4 GHz or 2-Ch. 3.2 GHz A/D, 2-Ch. 6.4 GHz D/A, Kintex UltraScale FPGA - AMC

Options:
- 084 XCKU060-2 FPGA
- 087 XCKU115-2 FPGA
- 104 LVDS FPGA I/O
- 702 Air cooled, Level L2
- 713 Convection cooled, Level L3

 Pentek, Inc.  One Park Way  Upper Saddle River  New Jersey 07458  Tel: 201-818-5900  Fax: 201-818-5904  Email: info@pentek.com  www.pentek.com
General Information

The Flexor® Model 5973 is a high-performance 3U OpenVPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions. That include data multiplexing, channel selection, data packing, gating, triggering and memory control.

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

---

New! New! New! New! New!
FlexorSet Model 5973-312
FlexorSet Model 5973-320
FlexorSet Model 5973-324

SPARK
Development Systems

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

FMC Product Combinations

If you wish to purchase this FMC Carrier in combination with an A/D FMC module, please see:
- FlexorSet Model 5973-312
- FlexorSet Model 5973-316
- FlexorSet Model 5973-320
- FlexorSet Model 5973-324

Xilinx Virtex-7 FPGA

The 5973 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5973 supports the emerging VITA-66.4 standard, that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The 5973 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Specifications

I/O Module Interface: VITA-57.1, High Pin Count FMC site
Field Programmable Gate Array
- Standard: Xilinx Virtex-7 XC7VX330T-2
- Optional: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- Parallel Option -104: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Optical Option -110: VITA-66.4, 12X duplex lanes

Memory
- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Contact Pentek for availability of rugged and conduction-cooled versions

Model 8267

VPX Development System
See 8267 Datasheet for Options
### General Information

The JadeFX™ Model 5983 is a high-performance 3U OpenVPX board based on the Xilinx Kintex UltraScale FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications. The 5983 includes a VITA-57.4 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface Flexor® FMCs to create a FlexorSet, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

### Board Architecture

Based on the proven design of the Pentek Jade family of Kintex UltraScale products, the JadeFX 5983 retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data-processing applications where each function exists as an intellectual property (IP) module. When integrated with a Pentek FMC, the 5983 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform generation engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel timing and sample-count information.

IP modules for DDR4 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

### Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition to the block diagrams, all source code and complete IP core documentation is included. Developers can

---

**Features**

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGAs
- 9 GB of DDR4 SDRAM
- On-board GPS receiver
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- User-configurable gigabit serial interface
- LVDS connections to the Kintex UltraScale FPGA for custom I/O
- Optional optical Interface for backplane gigabit serial interboard communication
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4, VITA-57.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Model 5983

3U OpenVPX Kintex UltraScale Processor and FMC Carrier

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O.

For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

The 5983 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications

I/O Module Interface: VITA-57.4, High Serial Pin-Count FMC site

Field Programmable Gate Array

Standard: Xilinx Kintex UltraScale XCKU060-2

Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O

Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

Type: DDR4 SDRAM

Size: Two banks, one 4 GB and one 5 GB

Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

Standard: L0 (air cooled)

Operating Temp: 0° to 50° C

Storage Temp: -20° to 90° C

Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)

Operating Temp: -20° to 65° C

Storage Temp: -40° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)

Operating Temp: -40° to 70° C

Storage Temp: -50° to 100° C

Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:

SLT3-PAY-2F12U1E-14.6.6-1

Ordering Information

Model Description
5983 3U OpenVPX Kintex UltraScale Processor and FMC Carrier

Options:
-087 XCKU115-2 FPGA
-110 VITA-66.4 12X optical interface
-180 GPS Support
-702 Air cooled, Level L2
-763 Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

Model Description
8267 VPX Development System
See 8267 Datasheet for Options

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx, OnyxFx and JadeFX 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

FlexorSet Product Combinations

If you wish to purchase this FMC Carrier in combination with an FMC module, please see:

- FlexorSet Model 5983-313
- FlexorSet Model 5983-317
- FlexorSet Model 5983-320
- FlexorSet Model 5983-324

Contact Pentek for availability of rugged and conduction-cooled versions

FlexorSet Model 5983-313

FlexorSet Model 5983-317

FlexorSet Model 5983-320

FlexorSet Model 5983-324
PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

Model 7070

General Information

The Flexor® Model 7070 is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of I/O options. When combined with any of Pentek’s analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

Board Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 retains all of the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the main board and the FMC module, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

The architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board’s analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample-count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070 and installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- VITA-57.1 FMC site offers access to a wide range of possible I/O
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- 4 GB of DDR3 SDRAM
- PCI Express (Gen. 1, 2 and 3) interface up to x8
- Optional user-configurable 12X optical gigabit serial interface
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Commercial and extended-temperature versions available
**Model 7070**

PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe

**Xilinx Virtex-7 FPGA**

The 7070 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and a card edge connector for custom I/O. For applications requiring custom gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTP optical connector is presented on a PCIe slot panel that can be installed in an empty, adjacent PCIe slot.

When configured with a VX330T FPGA, four duplex lanes are available.

**GateXpress for FPGA Configuration**

The 7070 architecture includes GateXpress, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately pre-presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most SBCs.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**Specifications**

I/O Module Interface: VITA-57.1, High Pin Count FMC site

Field Programmable Gate Array

- **Standard**: Xilinx Virtex-7 XC7VX330T-2
- **Optional**: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

- **Parallel, Option -104**: 16 pairs of LVDS connections between the FPGA and a card-edge connector.
- **Optical (Option -110)**: User-configurable 12X (VX690T) or 4X (VX 330T) optical gigabit serial interface, MTP connector installed in an empty adjacent slot

Memory

- **Type**: DDR3 SDRAM
- **Size**: Four banks, 1 GB each
- **Speed**: 800 MHz (1600 MHz DDR)

PCI-Express Interface

- **PCI Express Bus**: Gen. 1, 2 or 3: x4 or x8;
- **Environmental**: Level L1 & L2 air cooled,
- **Size**: Half-length PCIe card

---

**FMC Product Combinations**

If you wish to purchase this FMC Carrier in combination with an A/D FMC module, please see:

- FlexorSet Model 7070-312
- FlexorSet Model 7070-316
- FlexorSet Model 7070-320
- FlexorSet Model 7070-324

**Ordering Information**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070</td>
<td>PCI Express Virtex-7 Processor and FMC Carrier - x8 PCIe</td>
</tr>
</tbody>
</table>

**Options:**

- **-076**: XC7VX690T-2 FPGA
- **-104**: 16 pairs LVDS FPGA I/O
- **-110**: 12x gigabit serial optical I/O

Contact Pentek for availability of extended-temperature versions

**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Contact Pentek for availability of extended-temperature versions**

**Model 8266**

PC Development System

See 8266 Datasheet for Options
General Information
The Flexor® Model 3312 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3312 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-312 3U VPX or the FlexorSet 7070-312 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters
The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3312
The true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules
With the 3312 installed on either the 5973 or the 7070 carrier, the board-set features four A/D acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s task of identifying and executing on the data.

D/A Waveform Playback IP Module
With the 5973 or the 7070, the 3312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with minimum programming.

Features
- Sold as the:
  - FlexorSet Model 5973-312
  - FlexorSet Model 7070-312
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carriers
- Ruggedized and conduction-cooled versions available
**Model 8266**

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

**Model 8267**

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

---

**Model 3312 Specifications**

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**A/D Converters**
- **Type:** Texas Instruments ADS42LB69
- **Sampling Rate:** 10 MHz to 250 MHz
- **Resolution:** 16 bits

**D/A Converters**
- **Type:** Texas Instruments DAC5688
- **Input Data Rate:** 250 MHz max.
- **Output IF:** DC to 400 MHz max.
- **Output Sampling Rate:** 800 MHz max. with interpolation
- **Resolution:** 16 bits

**Front Panel Analog Signal Outputs**
- **Output Type:** Transformer-coupled, front panel connector
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

**Sample Clock Sources**
- **On-board clock generator:** Can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks
- **Front panel LVTTTL Gate/Trigger/Sync connector:** Can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

**Clock Synthesizer**
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front panel external clock
- **Synchronization:** VCXO can be phase-locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

**Clock Dividers**
- **External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D or D/A clocks**

---

**Digital Upconverter and D/A Stage**

A TI DAC5688 DUC (digital upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

**Clocking and Synchronization**

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTTL Gate/Trigger/Sync connector can receive an external timing signal allowing multiple modules to be synchronized thereby creating larger multi-board systems.

**ReadyFlow Board Support Package**

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3312’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

**Extendable IP Design**

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3312 or 7070/3312 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

**FMC Interface**

The Model 3312 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3312 and the FMC carrier.
General Information
Model 5973-312 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture
Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include multiplexing, channel selection, data packaging, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-312 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to simply play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design
For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Pentek, Inc. One Park Way Upper Saddle River New Jersey 07458 Tel: 201-818-5900 Fax: 201-818-5904 Email: info@pentek.com www.pentek.com
**A/D Acquisition IP Modules**

The 5973-312 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

**D/A Waveform Playback IP Module**

The 5973-312 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

**Xilinx Virtex-7 FPGA**

The 5973-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.
PCI Express Interface

The Model 5973-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5973-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

A/D Converter Stage

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LV/TTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz

Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

Parallel Option -104: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical Option -110: VITA-66.4, 12X duplex lanes

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-313 FlexorSet™ combines the Model 5983 and the Model 3313 Flexor™ FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-313 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a powerful DDC core.

The 5983-313 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-313 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can

Features

- VITA-57.4 HSPC FMC+ site offers access to a wide range of possible I/O
- Supports Xilinx Kintex UltraScale FPGA
- Four 250 MHz 16-bit A/Ds
- Four multiband DDCs
- One digital upconverter
- Two 800 MHz 16-bit D/As
- Extended Interpolation
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- LVDS connections to the Kintex UltraScale FPGA for custom I/O and synchronization
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

Pentek, Inc. • One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201-818-5900 • Fax: 201-818-5904 • Email: info@pentek.com

www.pentek.com
A/D Acquisition IP Modules

The 5983-313 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Generator IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Module

The 5983-313 factory-installed functions include a sophisticated D/A Waveform Generator IP module. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

DDC IP Cores

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving all four DDCs or each of the four A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s, where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

➤ integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

Xilinx Kintex UltraScale FPGA

The 5983-313 can be optionally populated with one of two Kintex UltraScale FGAs to match the specific requirements of the processing task. Supported FGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are optionally provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.
The 5983-313 supports the VITA-66.4 standard, that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

A/D Converter Stage

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.

Digital Upconverter and D/A Stage

A TI DAC5688 DUC and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency from DC to the sampling frequency. It delivers the output to the 16-bit D/A converter. Analog outputs are through front panel connectors.

If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz. In both modes the DAC5688 provides interpolation factors of 2x, 4x and 8x.

In addition, the FPGA-based interpolator provides a range of 2x to 65536x in two stages of 2x to 256x. Including the DAC5688 interpolation, the overall available interpolation range equals 2x to 524,288x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

PCI Express Interface

The Model 5983-313 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 5983-313 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Specifications

Front Panel Analog Signal Inputs

- **Input Type**: Transformer-coupled, front panel connectors
- **Transformer Type**: Coil Craft WBC4-6TLB
- **Full Scale Input**: +4 dBm into 50 ohms
- **3 dB Passband**: 300 kHz to 700 MHz

A/D Converters

- **Type**: Texas Instruments ADS42LB69
- **Sampling Rate**: 10 MHz to 250 MHz
- **Resolution**: 16 bits

4-Channel Digital Downconverter

- **Decimation Range**: 2x to 65,536x in two stages of 2x to 256x
- **LO Tuning Freq.**: 2x to fs
- **LO SFDR**: >120 dB
- **Phase Offset Resolution**: 32 bits, 0 to 360 degrees
- **FIR Filter**: 18-bit user-programmable coefficients, 24-bit output
- **Default Filter Set**: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
- **Phase Shift Coefficients**: I & Q with 16-bit resolution
- **Gain Coefficients**: 16-bit resolution
FlexorSet
Model 5983-313

4-Ch. 250 MHz 16-bit A/D with DDCs, 2-Ch. 800 MHz 16-bit D/A with DUC and Extended Interpolation - 3U VPX

Specifications, Continued

D/A Converters
Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Digital Interpolator
Interpolation Range: 2x to 65,536x in two stages of 2x to 256x
Total Interpolation Range D/A and digital combined: 2x to 524,288x

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel connector
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock
Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-1464.6-1

Contact Pentek for availability of rugged and conduction-cooled versions

SPARK Development Systems
The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards.
Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

Ordering Information

Model  Description
5983-313 4-Channel 250 MHz 16-bit A/D, with DDCs, 2-Channel 800 MHz 16-bit D/A with DUC, Extended Interpolation and Kintex Ultra-Scale FPGA - 3U VPX

Options:
-087 XCKU115-2 FPGA
-110 VITA-66.4 12X optical interface
-180 GPS Support
-702 Air cooled, Level L2
-763 Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 7070-312 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3312 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HP or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-312 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-312 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-312 features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-312 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 250 MHz 16-bit A/Ds
- One digital upconverter
- Two 800 MHz 16-bit D/As
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
A/D Acquisition IP Modules

The 7070-312 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Module in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Module

The 7070-312 factory-installed functions include a sophisticated D/A Waveform Playback IP module. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the dual D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

➤ Xilinx Virtex-7 FPGA

The 7070-312 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX990T. The VX990T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MT-1Poptical connector is presented on the PCIe slot panel.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the

www.pentek.com
PCI Express Interface

The Model 7070-312 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources

The 7070-312 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-312</td>
<td>4-Channel 250 MHz A/D, 2-Channel 800 MHz 16-bit D/A - x8 PCIe</td>
</tr>
</tbody>
</table>

Options:

- 076   | XC7VX690T-2 FPGA                                                             |
- 104   | LVDS FPGA I/O to card-edge connector                                        |
- 110   | 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T          |

Model 8266

See 8266 Datasheet for Options

4-Ch. 250 MHz 16-bit A/D, 2-Ch. 800 MHz 16-bit D/A - x8 PCIe

A/D Converters

Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

D/A Converters

Type: Texas Instruments DAC5688
Input Data Rate: 250 MHz max.
Output IF: DC to 400 MHz max.
Output Sampling Rate: 800 MHz max. with interpolation
Resolution: 16 bits

Front Panel Analog Signal Outputs

Type: Transformer-coupled, front panel connector
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Output: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz
Sample Clock Sources: On-board clock synthesizer generates two clocks: an A/D clock and a D/A clock

Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock

Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Option-076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled, Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
8-Channel 250 MHz, 16-bit A/D - FMC

General Information

The Flexor® Model 3316 is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3316 is sold as a complete turnkey data acquisition solution as the FlexorSet™ 5973-316 3U VPX or the FlexorSet 7070-316 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Performance of the Model 3316

The true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

Features

- Sold as the:
  - FlexorSet Model 5973-316
  - FlexorSet Model 7070-316
- Eight 250 MHz, 16-bit A/Ds
- On-board timing bus generator with multiboard synchronization
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Complete radar or software radio interface solution when combined with the Model 5973 3U OpenVPX or Model 7070 PCIe Virtex-7 FMC carrier
- Ruggedized and conduction-cooled versions available

A/D Acquisition IP Modules

With the 3316 installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Each IP module can have an associated memory bank on the Pentek FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s task of identifying and executing on the data.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized to create larger multiboard systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3316’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3316 or 7070/3316 IP modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3316 complies with the VITA 57 High Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3316 and the FMC carrier.

Model 3316 Specifications

Front Panel Analog Signal Inputs

| Input Type | Transformer-coupled, front panel connectors |
| Sample Clock Source | Transformer Type: Coil Craft WBC4-6TLB |
| Full Scale Input | Texas Instruments ADS42LB69 |
| Sampling Rate | 3 dB Passband: 300 kHz to 700 MHz |
| Resolution | 10 MHz to 250 MHz |
| Clock Synthesizer | 16 bits |

Ordering Information

| Model 3316 | 8-Channel 250 MHz, 16-bit A/D - FMC |

Contact Pentek for availability of rugged and conduction-cooled versions

| Model 8266 | PC Development System |
| Model 8267 | VPX Development System |

See 8266 Datasheet for Options

See 8267 Datasheet for Options

Pentek, Inc., One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com
www.pentek.com
General Information

Model 5973-316 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all dataclocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for backplane gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O. Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit backplane communications between boards independent of the PCIe interface.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters.
Memory Resources

The 5973-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 5973-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: CoilCraft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits
- Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

- 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
- Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory

- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
- Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-317 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor™ FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the IF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Jade products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-317 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains a powerful, programmable DDC FPGA core. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-317 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the back-plane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit back-plane communications between boards independent of the PCIe interface.
A/D Acquisition IP Modules

The 5983-317 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from its corresponding A/D or a test signal generator. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

be programmed from 2 to 32,768 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*f_s/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s/N.

Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

In addition, each DDC core includes a threshold detector to automatically send an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

A/D Converter Stage

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit.

In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

Memory Resources

The 5983-317 architecture supports two independent DDR3 SDRAM memory banks. These banks are 4 GB and 5 G deep and are an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-317 includes an industry-standard interface fully compliant with PCIe Gen. 1, 2 and 3 bus specifications. PCIe links up to x8, are supported.
FlexorSet
Model 5983-317
8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA - 3U VPX

GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Specifications
Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel connectors
Transformer Type: Coil Craft WBC4-6TLB
Full Scale Input: +4 dBm into 50 ohms
3 dB Passband: 300 kHz to 700 MHz

A/D Converters
Type: Texas Instruments ADS42LB69
Sampling Rate: 10 MHz to 250 MHz
Resolution: 16 bits

Digital Downconverters
Quantity: Eight channels
Decimation Range: 2x to 32,768x in three stages of 32x
LO Tuning Freq. Resolution: 32 bits, 0 to ƒs
LO SFDR: >120 dB
Phase Offset Resolution: 32 bits, 0 to 360 degrees
FIR Filter: 18-bit coefficients, 24-bit output, user-programmable coefficients
Default Filter Set: 80% bandwidth, <0.3 dB passband ripple, >100 dB stopband attenuation
Phase Shift Coefficients: I & Q with 16-bit resolution
Gain Coefficients: 16-bit resolution

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer
Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D clock

External Clock
Type: Front panel female MMCX connector, sine wave, 0 to +10 dBm
AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-317 is compatible with the following module profile, as defined by the VITA 65 OpenVPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1
General Information

Model 7070-316 is a member of the Flexor® family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3316 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-316 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-316 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-316 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-316 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulating/demodulating, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Features

- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Eight 250 MHz 16-bit A/Ds
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110: For applications requiring optical gigabit links, up to 12 high-speed, full-duplex FPGA GTX lanes driven via an optical transceiver support serial protocols. A 12-lane MTPOptical connector is presented on the PCIe slot panel.

**GateXpress for FPGA Configuration**

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**A/D Converter Stage**

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 dual 250 MHz, 16-bit A/D converters. 

**A/D Acquisition IP Modules**

The 7070-316 features eight A/D Acquisition IP Modules for easily capturing and moving data. Each IP module can receive data from any of the eight A/Ds or a test signal generator.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the PCIe interface. These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a linked-list DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data length information. These actions simplify the host processor’s job of identifying and executing on the data.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Memory Resources

The 7070-316 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

In addition to the factory-installed functions, custom user-installed IP within the FPGA can take advantage of the memories for many other purposes.

Clocking and Synchronization

An internal timing bus provides all timing and synchronization required by the A/D converters. Included are a clock, sync and gate or trigger signals. An on-board clock generator can receive an external sample clock from the front-panel coaxial connector. This clock can be used directly by the A/D section or divided by a built-in clock synthesizer circuit. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple boards to be synchronized to create larger multiboard systems.

PCI Express Interface

The Model 7070-316 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Specifications

Front Panel Analog Signal Inputs

- Input Type: Transformer-coupled, front panel connectors
- Transformer Type: Coil Craft WBC4-6TLB
- Full Scale Input: +4 dBm into 50 ohms
- 3 dB Passband: 300 kHz to 700 MHz

A/D Converters

- Type: Texas Instruments ADS42LB69
- Sampling Rate: 10 MHz to 250 MHz
- Resolution: 16 bits

Sample Clock Sources: On-board clock synthesizer

Clock Synthesizer

- Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- Synchronization: VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- Clock Dividers: External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D clock

External Clock

- Type: Front panel female SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

- Type: Front panel connector
- Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array

- Standard: Xilinx Virtex-7 XC7VX330T-2
- Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O

- Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the card-edge connector for custom I/O
- Optical (Option -110): 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory

- Type: DDR3 SDRAM
- Size: Four banks, 1 GB each
- Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8

Environmental

- Level L1 & L2 air-cooled,
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-316</td>
<td>8-Channel 250 MHz A/D with Virtex-7 FPGA - x8 PCIe</td>
</tr>
<tr>
<td>Options:</td>
<td></td>
</tr>
<tr>
<td>-076</td>
<td>XC7VX690T-2 FPGA</td>
</tr>
<tr>
<td>-104</td>
<td>LVDS FPGA I/O to card-edge connector</td>
</tr>
<tr>
<td>-110</td>
<td>12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
</tbody>
</table>
The Flexor™ Model 3320 is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

The 3320 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-320 3U VPX or the FlexorSet 7070-320 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

Performance of the Model 3320

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

A/D and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

A/D Acquisition IP Modules

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode. Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.

---

**Features**

- Sold as the:
  - FlexorSet Model 5973-320
  - FlexorSet Model 7070-320
- Supports Xilinx Virtex-7 VXT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- VITA 57 FMC compatible
- Ruggedized and conduction-cooled versions available

---

**Performance of the Model 3320**

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**A/D and Digital Downconverter Stage**

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the last page for supported modes.

**A/D Acquisition IP Modules**

With the 3320 installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the two D/A waveform playback IP modules in loopback mode. Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.
Digital Upconverter and D/A Stage

Two Texas Instruments DAC32784 D/As accept two baseband real or complex data streams from the FPGA. Each stream then goes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide interpolation factors from 1x to 16x.

D/A Waveform Playback IP Modules

A Texas Instruments DAC32784 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then goes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 5973 or the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the pre-defined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built-in frequency synthesizer that allows the board to operate without the need for an external clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3320’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/320 or 7070/320 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3320 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3320 and the FMC carrier.

Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.
Model 3320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

➤ Model 3320 Specifications

Front Panel Analog Signal Inputs
Input Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Mini-Circuits TC1-1-13M
Full Scale Input: +6.6 dBm into 50 ohms
3 dB Passband: 4.5 to 3000 MHz
A/D Converters
Type: Texas Instruments ADC32RF45
Sampling Rate and Resolution: See table below

Front Panel Analog Signal Outputs
Output Type: Transformer-coupled, front panel SSMC connectors
Transformer Type: Coil Craft WBC4-14L
Full-Scale Output: +4 dBm into 50 ohms
3 dB Passband: 1.5 MHz to 1200 MHz
D/A Converters
Type: Texas Instruments DAC39J84
Sampling Rate and Resolution: See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks
Timing Bus Generator
Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference
External Clock
Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms
External Trigger Input
Type: Front panel SSMC connector
Function: Programmable functions include: trigger, gate, sync and PPS
Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>Converter Sample Rate</th>
<th>Output Resolution</th>
<th>Decimation</th>
<th>Output Data Rate**</th>
<th>Real / Complex</th>
<th>Interpolation</th>
<th>Input Data Rate**</th>
<th>Real / Complex</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>3.0 GB/sec</td>
<td>complex</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>2</td>
<td>5.6 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
<td>bypass</td>
<td>5.0 GB/sec</td>
<td>real</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>4.0 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>2.0 GB/sec</td>
<td>real</td>
<td>1</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user
** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

Ordering Information

Model Description
5973-320 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX
Options:
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O to VPX P2
-110 VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

8267 VPX Development System See 8267 Datasheet for Options
7070-320 2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - x8 PCIe
Options:
-076 XC7VX690T-2 FPGA
-104 LVDS FPGA I/O to card-edge connector
-110 VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

8266 PC Development System See 8266 Datasheet for Options
**General Information**

Model 5973-320 is a member of the Flexor® family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**Features**

- Supports Xilinx Virtex-7 VXT FGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/A’s
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: V/ITA-46, V/ITA-48, V/ITA-66.4 and V/ITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available

**The Flexor Architecture**

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-320 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The Model 5973-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back the D/A’s waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

---

**Model 3320 FMC**

**Model 5973 FMC Carrier**

---

*See last page for configuration profiles*
A/D Acquisition IP Modules

The 5973-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator, or from the two D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in a FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command. ➤
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

**Memory Resources**

The 5973-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s waveform playback capabilities, providing local storage for user waveforms.

**PCI Express Interface**

The Model 5973-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

**A/D Converter and Digital Downconverter Stage**

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

**Digital Upconverter and D/A Stage**

A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

**Clocking and Synchronization**

The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.
FlexorSet
Model 5973-320

2-Ch. 3.0 GHz A/D, 2-Ch. 2.8 GHz D/A w/ Virtex-7 - 3U VPX

Specifications

Front Panel Analog Signal Inputs
  Input Type: Transformer-coupled, front panel SSMC connectors
  Transformer Type: Mini-Circuits TC1-1-13M
  Full Scale Input: +6.6 dBm into 50 ohms
  3 dB Passband: 4.5 to 3000 MHz

A/D Converters
  Type: Texas Instruments ADC32RF45
  Sampling Rate and Resolution: See table below

Front Panel Analog Signal Outputs
  Output Type: Transformer-coupled, front panel SSMC connectors
  Transformer Type: Coil Craft WBC4-14L
  Full-Scale Output: +4 dBm into 50 ohms
  3 dB Passband: 1.5 MHz to 1200 MHz

D/A Converters
  Type: Texas Instruments DAC39J84
  Sampling Rate and Resolution: See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
  Clock Source: Selectable from on-board frequency synthesizer or front panel external clock
  Synchronization: Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
  Type: Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
  Type: Front panel SSMC connector
  Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
  Standard: Xilinx Virtex-7 XC7VX330T-2
  Option -076: Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
  4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
  Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O
  Optical (Option -110): User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
  Type: DDR3 SDRAM
  Size: Four banks, 1 GB each
  Speed: 800 MHz (1600 MHz DDR)

PCI-Express Interface
  PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;
  Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
  Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model  Description
5973-320  2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 9U VPX

Options:
-076      XC7VX690T-2 FPGA
-104      LVDS FPGA I/O to VPX P2
-110      VITA-66.4 12X (with VX690T), 4X (with VX330T) optical interface

Contact Pentek for availability of rugged and conduction-cooled versions

Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>Converter</th>
<th>Sample Rate</th>
<th>Output Resolution</th>
<th>Decimation</th>
<th>Output Data Rate**</th>
<th>Real / Complex</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td></td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
<td>bypass</td>
<td>5.0 GB/sec</td>
<td>real</td>
<td></td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td></td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>2.0 GB/sec</td>
<td>real</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Interpolation</th>
<th>Input Data Rate**</th>
<th>Real / Complex</th>
</tr>
</thead>
<tbody>
<tr>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2</td>
<td>5.6 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2</td>
<td>4.0 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
<tr>
<td>1</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user
** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer

Model  Description
8267  VPX Development System
See 8267 Datasheet for Options
General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-320 FlexorSet™ combines the Model 5983 and the Model 3317 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances between them.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983-320 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-320 to operate as a turnkey solution without the need to develop any FPGA IP.
A/D Acquisition IP Modules

The 5983-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator or from the two D/A Waveform Generator IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Generator IP Modules

The 5983-320 factory-installed functions include two sophisticated D/A Waveform Generator IP modules. A linked-list controller allows users to easily record waveforms stored in either onboard or off-board host memory to the two D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board’s entire FPGA design as a block diagram that can be edited in Xilinx’s Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-320 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulating/demodulating, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X-8X-4X-32 connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

Memory Resources

The 5983-320 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage

The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on the next page for supported modes.
### GPS
An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

### Digital Upconverter and D/A Stage
A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

### Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

### Specifications

**Front Panel Analog Signal Inputs**
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

**A/D Converters**
- **Type:** Texas Instruments ADC32RF45
- **Sampling Rate and Resolution:** See the 3320 preconfigured modes table

**Front Panel Analog Signal Outputs**
- **Output Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Coil Craft WBC4-14L
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 1.5 MHz to 1200 MHz

**D/A Converters**
- **Type:** Texas Instruments DAC39J84
- **Sampling Rate and Resolution:** See the 3320 preconfigured modes table

**External Clock**
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

**External Trigger Input**
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

**Timing Bus Generator**
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

**Digital Upconverter and D/A Stage**
A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

### Clocking and Synchronization
Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LVTTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.
FlexorSet Model 5983-320

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Kintex UltraScale FPGA - 3U VPX

Field Programmable Gate Array
- Standard: Xilinx Kintex UltraScale XCKU060-2
- Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
- Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
- Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
- Type: DDR4 SDRAM
- Size: Two banks, one 4 GB and one 5 GB
- Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
- PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
- Environmental
  - Standard: L0 (air cooled)
    - Operating Temp: 0° to 50° C
    - Storage Temp: -20° to 90° C
    - Relative Humidity: 0 to 95%, non-condensing
  - Option -702: L2 (air cooled)
    - Operating Temp: -20° to 65° C
    - Storage Temp: -40° to 100° C
    - Relative Humidity: 0 to 95%, non-condensing
  - Option -763: L3 (conduction cooled)
    - Operating Temp: -40° to 70° C
    - Storage Temp: -50° to 100° C
    - Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5983-320</td>
<td>2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A with Virtex-7 FPGA - 3U VPX</td>
</tr>
</tbody>
</table>

Options:
- 087  XCKU115-2 FPGA
- 110  VITA-66.4 12X optical interface
- 180  GPS Support
- 702  Air cooled, Level L2
- 763  Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions
General Information

Model 7070-320 is a member of the Flexor family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3320 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-320 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-320 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-320 features two sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/A waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Features

- Supports Xilinx Virtex-7 VX7 FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Two 3.0 GHz* A/Ds
- Two 2.8 GHz* D/As
- Two digital downconverters
- Two digital upconverters
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- Optional optical Interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O

* See last page for configuration profiles
A/D Acquisition IP Modules

The 7070-320 features two A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the two A/Ds, a test signal generator, or from the two D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-320 factory-installed functions include two sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the two D/As.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-320 to operate as a turnkey solution without the need to develop any FPGA IP.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 7070-320 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

Option -104 provides 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides up to 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Memory Resources
The 7070-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface
The Model 7070-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage
The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.

Digital Upconverter and D/A Stage
A Texas Instruments DAC39J84 D/A accepts two baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the dual 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If translation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 2.8 GHz. In both modes the D/As provide programmable interpolation.

Clocking and Synchronization
The 3320 architecture includes a timing bus generator, responsible for providing clocking to the data converters, FPGA and all synchronization circuits. When paired with the 7070, the FlexorSet’s built-in functions include setup and support of the timing generator to produce the predefined data conversion profiles. This simplifies operation by allowing users to easily change profiles through software.

The timing bus generator has a built in frequency synthesizer that allows the board to operate without the need of an external sample clock. If users prefer, an external clock can be accepted on a front panel coax connector. In addition, the connector can be programmed to accept a 10 MHz system reference, locking the on-board clock to the reference that enables synchronization across multiple boards.

A front panel LVTTL Gate/Trigger/Sync connector is also included on the board. Users can program the connector’s function to operate in one of three modes to match the application requirements.

Memory Resources
The 7070-320 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s waveform playback capabilities, providing local storage for user waveforms.

PCI Express Interface
The Model 7070-320 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Digital Downconverter Stage
The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic countermeasures applications. The ADC32RF45 can operate within a range of different conversion speeds and resolutions. See the table on next page for supported modes.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Mini-Circuits TC1-1-13M
- **Full Scale Input:** +6.6 dBm into 50 ohms
- **3 dB Passband:** 4.5 to 3000 MHz

A/D Converters
- **Type:** Texas Instruments ADC32RF45
  - **Sampling Rate and Resolution:** See table below

Front Panel Analog Signal Outputs
- **Type:** Transformer-coupled, front panel SSMC connectors
- **Transformer Type:** Coil Craft WBC4-14L
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 1.5 MHz to 1200 MHz

D/A Converters
- **Type:** Texas Instruments DAC39J84
  - **Sampling Rate and Resolution:** See table below

Sample Clock Sources: Timing bus generator provides A/D and D/A clocks

Timing Bus Generator
- **Clock Source:** Selectable from on-board frequency synthesizer or front panel external clock
- **Synchronization:** Frequency synthesizer can be locked to an external 10 MHz PLL system reference

External Clock
- **Type:** Front panel SSMC connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms

External Trigger Input
- **Type:** Front panel SSMC connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option -076:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** User configurable VITA-66.4, 12X (with VX690T) or 4X (with VX330T) duplex lanes

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8
- **Environmental:** Level L1 & L2 air-cooled
- **Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Pre-configured Conversion Profiles*

<table>
<thead>
<tr>
<th>Converter Sample Rate</th>
<th>Output Resolution</th>
<th>Decimation</th>
<th>Output Data Rate**</th>
<th>Real / Complex</th>
<th>Interpolation</th>
<th>Input Data Rate**</th>
<th>Real / Complex</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.0 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>3.0 GB/sec</td>
<td>complex</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>2</td>
<td>5.6 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.8 GHz</td>
<td>16 bit</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
<td>4</td>
<td>2.8 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.5 GHz</td>
<td>12 bit</td>
<td>bypass</td>
<td>5.0 GB/sec</td>
<td>real</td>
<td>n/a</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>4.0 GB/sec</td>
<td>complex</td>
</tr>
<tr>
<td>2.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>4.0 GB/sec</td>
<td>real</td>
<td>2</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
<tr>
<td>1.0 GHz</td>
<td>14 bit</td>
<td>bypass</td>
<td>2.0 GB/sec</td>
<td>real</td>
<td>1</td>
<td>2.0 GB/sec</td>
<td>real</td>
</tr>
</tbody>
</table>

* Other modes can be custom-configured by the user

** Per channel, output data rates are subject to maximum PCIe bus speeds of the host computer
Model 3324

4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A-FMC

General Information

The Flexor® Model 3324 is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channelcount systems.

The 3324 is sold as a complete turnkey data acquisition and signal generation solution as the FlexorSet™ 5973-324 3U VPX or the FlexorSet 7070-324 PCIe board. For applications that require custom processing, the FlexorSets are ideal for IP development and deployment.

A/D Converters

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

Performance of the Model 3324

The true performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

A/D Acquisition IP Modules

With the 3324 installed on either the 5973 or the 7070 carrier, the board-set features four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

Each IP module can have an associated memory bank on the FMC carrier for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for easily moving A/D data through the FMC carrier’s PCIe interface.

These powerful linked-list DMA engines are capable of a unique acquisition gate-driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample-accurate time stamp and data-length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

With the 5973 or the 7070, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/A waveforms stored in either on-board or off-board host memory.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.
Model 8266

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Model 8267

The Model 8267 is a fully-integrated VPX development system for Pentek Cobalt, Onyx and Flexor VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Digital Upconverters and D/As

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconvert, interpolate and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency. The data is then delivered to the 16-bit D/A converter stages. Analog outputs are through front panel connectors.

If interpolation is disabled, the D/As act as interpolating 16-bit D/As with output sampling rates up to 1.5 GHz. In both modes the D/As provide interpolation factors of 2x, 4x, 8x and 16x.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector. This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO (Voltage-Controlled Crystal Oscillator). In this mode, the front panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel Gate/Trigger/PPS connector can receive an external timing signal allowing multiple modules to be synchronized and create larger multiboard systems.

ReadyFlow Board Support Package

When used with the 5973 or the 7070, Pentek’s ReadyFlow® BSP provides control of all the 3324’s hardware and IP-based functions. Ready to run examples and a fully-sourced C library provide a quick-start and powerful platform to create custom applications. ReadyFlow is compatible with Windows and Linux operating systems.

Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek’s GateFlow® FPGA Design Kits include all of the factory-installed Virtex-7-based 5973/3324 or 7070/3324 modules as documented source code. Using Xilinx Vivado tools, developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek 5973/7070 IP with their own.

FMC Interface

The Model 3324 complies with the VITA 57 High-Pin Count FMC specification. The interface provides all data, clocking, synchronization, control and status signals between the 3324 and the FMC carrier.

Model 3324 Specifications

Front Panel Analog Signal Inputs

- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Texas Instruments ADS54J60
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 250 kHz to 750 MHz

A/D Converters

- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs

- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits
- **Sample Clock Source:** On-board clock synthesizer

Clock Synthesizer

- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz) or front-panel external clock
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for the A/D and D/A clocks

External Clock

- **Type:** Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input

- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Environmental

- **Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized**
- **I/O Module Interface:** VITA-57.1, High-pin-count FMC

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3324</td>
<td>4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A - FMC</td>
</tr>
</tbody>
</table>

Contact Pentek for availability of rugged and conduction-cooled versions

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8266</td>
<td>PC Development System See 8266 Datasheet for Options</td>
</tr>
<tr>
<td>8267</td>
<td>VPX Development System See 8267 Datasheet for Options</td>
</tr>
</tbody>
</table>
General Information

Model 5973-324 is a member of the Flexor family of high-performance 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet™ integrated solution, the Model 3324 FMC is factory-installed on the 5973 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 5973-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

The Flexor Architecture

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 5973 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5973-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 5973-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973-324 to operate as a turnkey solution without the need to develop any FPGA IP.

---

Features

- Supports Xilinx Virtex-7 XVT FPGAs
- GateXpress supports dynamic FPGA reconfiguration across PCIe
- Four 500 MHz 16-bit A/Ds
- Four digital upconverters
- Four 2 GHz 16-bit D/As (500 MHz input sample rate, 2 GHz output sample rate with interpolation)
- 4 GB of DDR3 SDRAM
- Sample clock synchronization to an external system reference
- PCI Express (Gen. 1, 2 & 3) interface up to x8
- User-configurable gigabit serial interface
- Optional optical interface for gigabit serial interboard communication
- Optional LVDS connections to the Virtex-7 FPGA for custom I/O
- Compatible with several VITA standards including: VITA-46, VITA-48, VITA-66.4 and VITA-65 (OpenVPX™ System Specification)
- Ruggedized and conduction-cooled versions available
A/D Acquisition IP Modules

The 5973-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Playback IP modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 5973-324 factory-installed functions include four sophisticated D/A Waveform Playback IP modules. A linked-list controller allows users to easily play back waveforms stored in either on-board or off-board host memory to the four D/A peripherals.

Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

➤ Extendable IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow® FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Xilinx Virtex-7 FPGA

The 5973-324 can be optionally populated with one of two Virtex-7 FPGAs to match the specific requirements of the processing task. Supported FPGAs are VX330T or VX690T. The VX690T features 3600 DSP48E1 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost VX330T can be installed.

A 4X connection between the FPGA and the VPX P1 connector supports gigabit serial protocols.

Option -104 provides 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O.

Option -110 supports the VITA-66.4 standard that provides 12 optical duplex lanes to the backplane. With the installation of a serial protocol, the VITA-66.4 interface enables gigabit communications between boards independent of the PCIe interface.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. ➤
FlexorSet
Model 5973-324

### PCI Express Interface

The Model 5973-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

### Memory Resources

The 5973-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

### Model 8267

The Model 8267 is a fully-integrated development system for Pentek Cobalt, Onyx and Flexor 3U VPX boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5973-324</td>
<td>4-Ch. 500 MHz 16-bit A/D, 4-Ch. 2 GHz 16-bit D/A - 3U VPX</td>
</tr>
</tbody>
</table>

### Front Panel Analog Signal Inputs

<table>
<thead>
<tr>
<th>Input Type</th>
<th>Transformer-coupled, front panel connectors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer Type</td>
<td>Cool Craft WBC4-6TBB</td>
</tr>
</tbody>
</table>

### Clock Synthesizer

Clock Source: Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus

### Field Programmable Gate Array

Standard: Xilinx Virtex-7 XC7VX330T-2
Option -076: Xilinx Virtex-7 XC7VX690T-2

### Custom FPGA I/O

4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.

### Parallel (Option -104): 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

### Optical (Option -110): VITA-66.4, 12X duplex lanes

### Memory

Type: DDR3 SDRAM
Size: Four banks, 1 GB each
Speed: 800 MHz (1600 MHz DDR)

### PCI-Express Interface

PCI Express Bus: Gen. 1, 2 or 3: x4 or x8
Environmental: Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized
Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

---

Contact Pentek for availability of rugged and conduction-cooled versions.

---

Pentek, Inc. One Park Way • Upper Saddle River • New Jersey 07458
Tel: 201 818-5900 • Fax: 201-818-5904 • Email: info@pentek.com
www.pentek.com
General Information

Model 5983 is a member of the JadeFX™ family of high-performance 3U VPX baseboards with a Xilinx Kintex UltraScale FPGA and an available FMC I/O slot.

As an integrated solution, the Model 5983-324 FlexorSet™ combines the Model 5983 and the Model 3324 Flexor® FMC as a factory-installed set. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the IF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

In addition to the Gen. 3 x8 PCIe interface, the 5983 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on a VITA-66.4 connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5983s mounted in the same chassis or even over extended distances.

The Flexor Architecture

Based on the proven design of the Pentek Jade family of Kintex products, the 5983 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 5983-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

The 5983-324 features a sophisticated D/A waveform generator IP module. A linked-list controller allows users to easily record to the D/A wavesforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform.

Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.
A/D Acquisition IP Modules

The 5983-324 features four A/D Acquisition IP Modules for easy capture and data moving. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the four D/A Waveform Recorder IP modules in loopback mode. Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor's job of identifying and executing on the data.

D/A Waveform Recorder IP Modules

The 5983-324 factory-installed functions include four sophisticated D/A Waveform Recorder IP modules. A linked-list controller allows users to easily record waveforms stored in either on-board or off-board host memory to the four D/As.

Parameters including length of waveform, delay from trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries per module can be chained together to create complex waveforms with a minimum of programming.

Extensible IP Design

For applications that require specialized functions, users can install their own custom IP for data processing. The Pentek Navigator FPGA Design Kits include the board's entire FPGA design as a block diagram that can be edited in Xilinx's Vivado tool suite. In addition, all source code and complete IP core documentation is included. Developers can integrate their own IP along with the Pentek factory-installed functions or use the Navigator kit to completely replace the Pentek IP with their own.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5983-324 to operate as a turnkey solution without the need to develop any FPGA IP.

Xilinx Kintex UltraScale FPGA

The 5983-324 can be optionally populated with one of two Kintex UltraScale FPGAs to match the specific requirements of the processing task. Supported FPGAs are KU060 or KU115. The KU115 features 5520 DSP48E2 slices and is ideal for modulation/demodulation, encoding/decoding, encryption/decryption, and channelization of the signals between transmission and reception. For applications not requiring large DSP resources or logic, the lower-cost KU060 can be installed.

Sixteen pairs of LVDS connections are provided between the FPGA and the VPX P2 connector for custom I/O. For applications requiring custom gigabit links, a 4X connection is supported between the FPGA and the VPX P1 connector to support serial protocols.

Memory Resources

The 5983-324 architecture supports two independent DDR3 SDRAM memory banks. The banks are four and five gigabytes each and are part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

PCI Express Interface

The Model 5983-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

A/D Converter and Downconverter

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconverter, interpolator and D/A stages of the converter.

When operating as DUCs (digital upconverters), the converters interpolate and translate real or complex baseband input signals to a programmable IF center frequency.

Digital Upconverter and D/A

Four D/As accept baseband real or complex data streams from the FPGA. Each stream then passes through the upconverter, interpolator and D/A stages of the converter.
GPS

An optional GPS receiver provides time and position information to the FPGA. This information can be used for precise data tagging.

Clocking and Synchronization

Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters. Each includes a clock, sync and gate or trigger signals. An on-board clock generator receives an external sample clock from the front panel coaxial connector.

This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer circuit to provide different A/D and D/A clocks. In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front-panel coaxial connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A front panel LV TTL Gate/Trigger/Sync connector can receive an external timing signal to synchronize multiple modules.

Specifications

Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-6TLB
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources:
- **Type:** On-board clock
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks
SPARK Development Systems

The SPARK Development Systems are fully-integrated platforms for Pentek Cobalt, Onyx, Jade and Flexor boards. Available in a PCIe rackmount (Model 8266), a 3U VPX chassis (Model 8267) or a 6U VPX chassis (Model 8264), they were created to save engineers and system integrators the time and expense associated with building and testing a development system. Each SPARK system is delivered with the Pentek board(s) and required software installed and equipped with sufficient cooling and power to ensure optimum performance.

FlexorSet Model 5983-324

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A
Kintex UltraScale FPGA - 3U VPX

Ordering Information

Model  Description
5983-324  4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Kintex UltraScale FPGA - 3U VPX

Options:
-087  XCKU115-2 FPGA
-110  VITA-66.4 12X optical interface
-180  GPS Support
-702  Air cooled, Level L2
-763  Conduction-cooled, Level L3

Contact Pentek for availability of rugged and conduction-cooled versions

External Clock
Type: Front panel connector, sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
Type: Front panel connector
Function: Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
Standard: Xilinx Kintex UltraScale XCKU060-2
Optional: Xilinx Kintex UltraScale XCKU115-2

Custom FPGA I/O
Serial: 4X gigabit links between the FPGA and the VPX P1 connector to support serial protocols.
Parallel: 16 pairs of LVDS connections between the FPGA and the VPX P2 connector for custom I/O

Optical (Option -110): VITA-66.4, 12X duplex lanes

Memory
Type: DDR4 SDRAM
Size: Two banks, one 4 GB and one 5 GB
Speed: 1200 MHz (2400 MHz DDR)

PCI-Express Interface
PCI Express Bus: Gen. 1, 2 or 3: x4 or x8;

Environmental
Standard: L0 (air cooled)
Operating Temp: 0° to 50° C
Storage Temp: -20° to 90° C
Relative Humidity: 0 to 95%, non-condensing

Option -702: L2 (air cooled)
Operating Temp: -20° to 65° C
Storage Temp: -40° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Option -763: L3 (conduction cooled)
Operating Temp: -40° to 70° C
Storage Temp: -50° to 100° C
Relative Humidity: 0 to 95%, non-condensing

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

OpenVPX Compatibility: The Model 5983-313 is compatible with the following module profile, as defined by the VITA 65 Open-VPX Specification:
SLT3-PAY-2F1F2U1E-14.6.6-1

Data Plane – 2 Fat Pipes
Expansion Plane – 8 Pairs
Control Plane* – 2 Ultra-Thin Pipes
VITA 65 Aperture E (VITA 66.4)

* not connected on board
**General Information**

Model 7070-324 is a member of the Flexor™ family of high-performance PCIe boards based on the Xilinx Virtex-7 FPGA.

As a Flexor™ integrated solution, the Model 3324 FMC is factory-installed on the 7070 FMC carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, the Model 7070-324 includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

**The Flexor Architecture**

Based on the proven design of the Pentek Onyx family of Virtex-7 products, the 7070 FMC carrier retains all the key features of that family. As a central foundation of the board architecture, the FPGA has access to all data and control paths of both the carrier board and the FMC module, enabling factory-installed functions that include data multiplexing, channel selection, data packing, gating, triggering and memory control.

When delivered as an assembled board set, the 7070-324 includes factory-installed applications ideally matched to the board’s analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer.

Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

The 7070-324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 7070-324 to operate as a turnkey solution without the need to develop any FPGA IP.

**Extendable IP Design**

For applications that require specialized functions, users can install their custom IP modules.
A/D Acquisition IP Modules

The 7070-324 features four A/D Acquisition IP Modules for easy capture and data movement. Each IP module can receive data from any of the four A/Ds, a test signal generator or from the D/A Waveform Playback IP Modules in loopback mode.

Each IP module has an associated memory bank for buffering data in FIFO mode or for storing data in transient capture mode. All memory banks are supported with DMA engines for moving A/D data through the PCIe interface.

These powerful linked-list DMA engines are capable of a unique Acquisition Gate Driven mode. In this mode, the length of a transfer performed by a link definition need not be known prior to data acquisition; rather, it is governed by the length of the acquisition gate. This is extremely useful in applications where an external gate drives acquisition and the exact length of that gate is not known or is likely to vary.

For each transfer, the DMA engine can automatically construct metadata packets containing A/D channel ID, a sample accurate time stamp, and data length information. These actions simplify the host processor’s job of identifying and executing on the data.

D/A Waveform Playback IP Modules

The 7070-324 factory-installed functions include four sophisticated D/A Waveform Playback IP Modules. A linked-list controller allows users to easily play back waveforms stored in either volatile or non-volatile memory when power is removed. In applications where the D/A IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT or through the board’s PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

GateXpress for FPGA Configuration

The Flexor architecture includes GateXpress®, a sophisticated FPGA-to-PXI configuration manager for loading and reloading the FPGA. At power-up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on many systems.

The board’s configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board’s PCIe interface. At power-up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first option to load is an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in non-volatile memory when power is removed. In applications where the FPGA IP is expected to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT. In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space.
PCI Express Interface
The Model 7070-324 includes an industry-standard interface fully compliant with PCI Express Gen. 1, 2 and 3 bus specifications. Supporting PCIe links up to x8, the interface includes multiple DMA controllers for efficient transfers to and from the board.

Memory Resources
The 7070-324 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the board’s DMA capabilities, providing FIFO memory space for creating DMA packets.

Model 8266
The Model 8266 is a fully-integrated PC development system for Pentek Cobalt, Onyx and Flexor PCI Express boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7070-324</td>
<td>4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A with Virtex-7 FPGA - x8 PCIe</td>
</tr>
</tbody>
</table>

Options:
- 076: XC7VX690T-2 FPGA
- 104: LVDS FPGA I/O to card-edge connector
- 110: 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x w. XC7VX330T

Model 8266
See 8266 Datasheet for Options

Specifications
Front Panel Analog Signal Inputs
- **Input Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC1-1TLB
- **Full-Scale Input:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 750 MHz

Clocking and Synchronization
- Two internal timing buses provide all timing and synchronization required by the A/D and D/A converters.
- Each includes a clock, sync and gate or trigger signals.
- An on-board clock generator receives an external signal from the front panel coaxial connector.
- This clock can be used directly by the A/D or D/A sections or divided by a built-in clock synthesizer to provide different A/D and D/A clocks.
- In an alternate mode, the sample clock can be sourced from an on-board programmable VCXO. In this mode, the front coaxial panel connector can be used to provide a 10 MHz reference clock for synchronizing the internal oscillator.

A/D Converters
- **Type:** Texas Instruments ADS54J60
- **Sampling Rate:** Up to 500 MHz
- **Resolution:** 16 bits

Front Panel Analog Signal Outputs
- **Output Type:** Transformer-coupled, front panel connectors
- **Transformer Type:** Coil Craft WBC4-4TLB
- **Full-Scale Output:** +4 dBm into 50 ohms
- **3 dB Passband:** 300 kHz to 700 MHz

D/A Converters
- **Type:** Texas Instruments DAC38J84
- **Input Data Rate:** Up to 500 MHz
- **Output Sample Rate:** Up to 2 GHz (with interpolation)
- **Resolution:** 16 bits

Sample Clock Sources:
- On-board clock
- DUCs (Digital Upconverters) generate clocks: an A/D clock and a D/A clock

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 810 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference, typically 10 MHz
- **Clock Dividers:** External clock or VCXO can be divided by 1, 2, 4, 8 or 16 for the A/D and D/A clocks

External Clock
- **Type:** Front panel connector, sine wave, or trigger, gate, sync and PPS
- Accepts 10 to 800 MHz divider input clock or PLL system reference

External Trigger Input
- **Type:** Front panel connector
- **Function:** Programmable functions include: trigger, gate, sync and PPS

Field Programmable Gate Array
- **Standard:** Xilinx Virtex-7 XC7VX330T-2
- **Option:** Xilinx Virtex-7 XC7VX690T-2

Custom FPGA I/O
- **Parallel (Option -104):** 16 pairs of LVDS connections between the FPGA and a card-edge connector for custom I/O
- **Optical (Option -110):** 12x gigabit serial optical I/O with XC7VX690T FPGA, 4x with XC7VX330T

Memory
- **Type:** DDR3 SDRAM
- **Size:** Four banks, 1 GB each
- **Speed:** 800 MHz (1600 MHz DDR)

PCI-Express Interface
- **PCI Express Bus:** Gen. 1, 2 or 3: x4 or x8

Environmental
- **Level L1 & L2 air-cooled, Level L3 conduction-cooled, ruggedized Size:** 3.937 in. x 6.717 in. (100 mm x 170.6 mm)
**Bandit Two-Channel Analog RF Wideband Downconverter - PMC/XMC**

**General Information**

The Bandit® Model 7120 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PMC/XMC module with front-panel connectors for easy integration into RF systems, the module offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7120 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 7120 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

The 7120 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

The 7120 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, the 7120 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference

---

**Features**

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference
### Specifications

**RF Input**
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 μsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**RF Attenuator:**
- Programmable from 0 to 63 dB in 0.5 dB steps

**LO Synthesizer Tuning**
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 μsec
- Phase-Locked Loop Bandwidth: 100 kHz

**Phase Noise**
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

**Noise Figure (referred to input)**
- 60 dB gain: 2.6 dB

**INBAND Output IP3**
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

**Reference Input/Output**
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms

**Reference Input Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**Reference Output Signal**
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

**OCXO Reference**
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  - (20 years): ±4.60 ppm
- Phase Noise
  - 1 Hz Offset: –67 dBc/Hz
  - 10 Hz Offset: –100 dBc/Hz
  - 100 Hz Offset: –130 dBc/Hz
  - 1 kHz Offset: –148 dBc/Hz
  - 10 kHz Offset: –154 dBc/Hz
  - 100 kHz Offset: –155 dBc/Hz

**IF Output**
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

**Programming**
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

**Power**
- Voltage: +12 VDC
- Current: 1.5 A

**PMC/XMC Interface:**
- Power only on PMC P11 (option -104) or XMC P15 (option -105)
- Size: Standard PMC module, 2.91 in. x 5.87 in.
Model 7820

Bandit Two-Channel Analog RF Wideband Downconverter - PCIe

**General Information**

The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

**Programmable Input Level**

The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

**Input Filter Options**

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

**Quadrature Mixers**

The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

**Tuning Accuracy**

The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

**On-board Reference Clock**

In addition to accepting a 10 MHz reference signal on the front panel, the 7820 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

**Wideband Output**

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
## Specifications

### RF Input
- Connector Type: SSMC
- Impedance: 50 ohms
- Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz, ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

### LO Synthesizer Tuning
- Frequency range: 400–4000 MHz
- Resolution: < 10 kHz
- Tuning Speed: < 500 μsec
- Loop Bandwidth: 100 kHz

### Phase Noise
- 1 kHz: -90 dBc/Hz
- 100 kHz: -110 dBc/Hz
- 1 MHz: -130 dBc/Hz

### Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

### Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

### Reference Input/Output
- Connector Type: SSMC
- Impedance: 50 ohms
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

### Reference Output Signal
- Frequency: 10 MHz
- Level: 0 dBm, sine wave

### OCXO Reference
- Center Frequency: 10 MHz
- Stability vs. Change in Temperature: ±50.0 ppb
- Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  - (20 years): ±4.60 ppm
- Phase Noise
  - 1 Hz Offset: -67 dBc/Hz
  - 10 Hz Offset: -100 dBc/Hz
  - 100 Hz Offset: -130 dBc/Hz
  - 1 KHz Offset: -148 dBc/Hz
  - 10 KHz Offset: -154 dBc/Hz
  - 100 KHz Offset: -155 dBc/Hz

### IF Output
- Connector Type: SSMC
- Impedance: 50 ohms
- Frequency: User definable
- Level: 0 dBm, nominal

### Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

### Power
- Voltage: +12 VDC
- Current: 1.5 A

### PCI-Express Interface
- PCI Express Bus: x4 or x8, power only

### Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: -20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

### Size
- Half length PCIe card, 4.38 in. x 7.13 in.

---

### Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7820</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - PCIe</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
General Information
The Bandit® Model 5220 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded 3U VPX board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5220 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level
The 5220 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options
An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers
The 5220 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy
The 5220 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock
In addition to accepting a 10 MHz reference signal on the front panel, the 5220 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output
Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX

Specifications

RF Input
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz

Phase Noise
- 1 kHz: –90 dBc/Hz
- 100 kHz: –110 dBc/Hz
- 1 MHz: –130 dBc/Hz

Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave
- Reference Output Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±300 ppb
- Total Frequency Tolerance
  (20 years): ±4.60 ppm

Phase Noise
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 KHz Offset: –148 dBc/Hz
- 10 KHz Offset: –154 dBc/Hz
- 100 KHz Offset: –155 dBc/Hz

IF Output
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI Express Interface
- PCIe Bus: x4, power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5220</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - 3U VPX</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
General Information

These Bandit® models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded 6U VPIX boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 5720 is a 6U VPX board that provides two channels, while Model 5820 is a double-density 6U VPX board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U OpenVPX

Specifications

RF Input
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to 63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz
- Phase Noise
  - 1 kHz: –90 dBc/Hz
  - 100 kHz: –110 dBc/Hz
  - 1 MHz: –130 dBc/Hz
- Noise Figure (referred to input)
  - 60 dB gain: 2.6 dB

Inband Output IP3
- 20 dB gain: +10 dBm
- 60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms
- Reference Input Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave
- Reference Output Signal
  - Frequency: 10 MHz
  - Level: 0 dBm, sine wave

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  - Daily: ±10 ppb/day
  - First Year: ±30 ppb
- Total Frequency Tolerance (20 years): ±4.60 ppm

Phase Noise
- 1 Hz Offset: –67 dBc/Hz
- 10 Hz Offset: –100 dBc/Hz
- 100 Hz Offset: –130 dBc/Hz
- 1 KHz Offset: –148 dBc/Hz
- 10 KHz Offset: –154 dBc/Hz
- 100 KHz Offset: –155 dBc/Hz

IF Output
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Programming
- Functions: RF Atten, IF Atten, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI Express Interface
- PCI Bus: x4 or x8, power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.
- Size: 233 mm x 160 mm (9.173 in. x 6.299 in.)

Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5720</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - 6U OpenVPX Single Density</td>
</tr>
<tr>
<td>5820</td>
<td>Bandit Four-Channel Analog RF Wideband Downconverter - 6U OpenVPX Double Density</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
General Information

These Bandit® models are two- or four-channel, high-performance, stand-alone analog RF wideband downconverters. Packaged in small, shielded cPCI boards with front-panel connectors for easy integration into RF systems, they offer programmable gain, high dynamic range and a low noise figure.

Model 7320 is a 3U cPCI board while Model 7220 is a 6U cPCI board; both provide two channels, while Model 7420 is a double-density 6U cPCI board that provides four channels.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, these models are ideal solutions for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The models accept RF signals on two or four front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

These models feature Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

These models use the Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, these models include on-board 10 MHz crystal oscillators which can be used as the reference to lock the internal LO frequency synthesizers. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Outputs are provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Bandit Two- or Four-Channel Analog RF Wideband Downconverter - 6U/3U cPCI

Specifications

RF Input
- Connector Type: SSMC
- Input Impedance: 50 ohms
- Input Level Range: -60 dBm to -20 dBm
- Flatness: ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from
  3 GHz to 4 GHz
- RF Attenuator: Programmable from 0 to
  63 dB in 0.5 dB steps

LO Synthesizer Tuning
- Frequency range: 400–4000 MHz,
- Resolution: < 10 kHz
- Tuning Speed: < 500 µsec
- Phase-Locked Loop Bandwidth: 100 kHz
- Phase Noise
  1 kHz: –90 dBc/Hz
  100 kHz: –110 dBc/Hz
  1 MHz: –130 dBc/Hz
- Noise Figure (referred to input)
  60 dB gain: 2.6 dB
- Inband Output IP3
  20 dB gain: +10 dBm
  60 dB gain: +42 dBm

Reference Input/Output
- Connector Type: SSMC
- Input/Output Impedance: 50 ohms
- Reference Input Signal
  Frequency: 10 MHz
  Level: 0 dBm, sine wave
- Reference Output Signal
  Frequency: 10 MHz
  Level: 0 dBm, sine wave

OCXO Reference
- Center Frequency: 10 MHz
- Frequency Stability vs. Change in
  Temperature: ±50.0 ppb
- Frequency Calibration: ±1.0 ppm
- Aging
  Daily: ±10 ppb/day
  First Year: ±300 ppb
- Total Frequency Tolerance
  (20 years): ±4.60 ppm
- Phase Noise
  1 Hz Offset: –67 dBc/Hz
  10 Hz Offset: –100 dBc/Hz
  100 Hz Offset: –130 dBc/Hz
  1 KHz Offset: –148 dBc/Hz
  10 KHz Offset: –154 dBc/Hz
  100 KHz Offset: –155 dBc/Hz

IF Output
- Connector Type: SSMC
- Output Impedance: 50 ohms
- Center Frequency: User definable
- Output Level: 0 dBm, nominal

Programming
- Functions: RF Att, IF Att, Int/Ext
- Reference Select, LO Synthesizer Frequency
- Interface: USB
- Connector Type: MicroUSB

Power
- Voltage: +12 VDC
- Current: 1.5 A

PCI Interface
- PCI Bus: 32-bit, 66 MHz (supports
  33 MHz), power only

Environmental
- Operating Temp: 0° to 50° C
- Storage Temp: –20° to 90° C
- Relative Humidity: 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board

Ordering Information

Model | Description
--- | ---
7220 | Bandit Two-Channel Analog RF Wideband Downconverter - 6U cPCI
7320 | Bandit Two-Channel Analog RF Wideband Downconverter - 3U cPCI
7420 | Bandit Four-Channel Analog RF Wideband Downconverter - 6U cPCI

Option | Description
--- | ---
-015 | Oven Controlled Reference Oscillator
-145 | 1.45 GHz lowpass input filter
-280 | 2.80 GHz lowpass input filter
Bandit Two-Channel Analog RF Wideband Downconverter - AMC

General Information

The Bandit® Model 5620 is a two-channel, high-performance, stand-alone analog RF wideband downconverter. Packaged in a small, shielded AMC board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 5620 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 5620 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from –60 dBm to –20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Input Filter Options

An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic suppression.

Quadrature Mixers

The 5620 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380’s are capable of excellent accuracy with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively.

Tuning Accuracy

The 5620 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

On-board Reference Clock

In addition to accepting a 10 MHz reference signal on the front panel, the 5620 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer. This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

Wideband Output

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. Alternatively, either I or Q output can be used at some intermediate offset frequency convenient to the application. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.

Features

- Accepts RF signals from 400 MHz to 4000 MHz
- Accepts RF input levels from -60 dBm to -20 dBm
- Baseband IF output with up to 390 MHz bandwidth
- Internal OCXO or external 10 MHz frequency reference
## Specifications

### RF Input
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Input Level Range:** -60 dBm to -20 dBm
- **Flatness:** ±2 dB from 400 MHz to 1 GHz,
  ±3 dB from 1 GHz to 3 GHz, ±5 dB from 3 GHz to 4 GHz
- **RF Attenuator:** Programmable from 0 to 63 dB in 0.5 dB steps

### LO Synthesizer Tuning
- **Frequency range:** 400–4000 MHz,
- **Resolution:** < 10 kHz
- **Tuning Speed:** < 500 µsec
- **Phase-Locked Loop Bandwidth:** 100 kHz
- **Phase Noise**
  - 1 kHz: -90 dBc/Hz
  - 100 kHz: -110 dBc/Hz
  - 1 MHz: -130 dBc/Hz

### Noise Figure (referred to input)
- 60 dB gain: 2.6 dB

### RF Attenuator
- Programmable from 0 to 63 dB in 0.5 dB steps

### Inband Output IP3
- **20 dB gain:** +10 dBm
- **60 dB gain:** +42 dBm

### Reference Input/Output
- **Connector Type:** SSMC
- **Input Impedance:** 50 ohms
- **Reference Input Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave
- **Reference Output Signal**
  - **Frequency:** 10 MHz
  - **Level:** 0 dBm, sine wave

### OCXO Reference
- **Center Frequency:** 10 MHz
- **Frequency Stability vs. Change in Temperature:** ±50.0 ppb
- **Frequency Calibration:** ±1.0 ppm

### Aging
- **Daily:** ±10 ppb/day
- **First Year:** ±300 ppb
- **Total Frequency Tolerance**
  - (20 years): ±4.60 ppm

### Phase Noise
- **1 Hz Offset:** -67 dBc/Hz
- **10 Hz Offset:** -100 dBc/Hz
- **100 Hz Offset:** -130 dBc/Hz
- **1 KHz Offset:** -148 dBc/Hz
- **10 KHz Offset:** -154 dBc/Hz
- **100 KHz Offset:** -155 dBc/Hz

### IF Output
- **Connector Type:** SSMC
- **Output Impedance:** 50 ohms
- **Center Frequency:** User definable
- **Output Level:** 0 dBm, nominal

### Programming
- **Functions:** RF Atten, IF Atten, Int/Ext Reference Select, LO Synthesizer Frequency
- **Interface:** USB
- **Connector Type:** MicroUSB

### Power
- **Voltage:** +12 VDC
- **Current:** 1.5 A

### PCI-Express Interface
- **PCI Express Bus:** Gen. 1 x4 or x8, power only

### Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** -20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.
- **Size:** Single-width, full-height AMC module, 2.89 in. x 7.11 in.

## Ordering Information

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5620</td>
<td>Bandit Two-Channel Analog RF Wideband Downconverter - AMC</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-015</td>
<td>Oven Controlled Reference Oscillator</td>
</tr>
<tr>
<td>-145</td>
<td>1.45 GHz lowpass input filter</td>
</tr>
<tr>
<td>-280</td>
<td>2.80 GHz lowpass input filter</td>
</tr>
</tbody>
</table>
General Information

The Bandit® Model 8111 provides a series of high-performance, stand-alone analog RF slot downconverter modules. Packaged in a small, shielded enclosure with connectors for easy integration into RF systems, the modules offer programmable gain, high dynamic range and a low noise figure. With input options to cover specific frequency bands of the RF spectrum, and an IF output optimized for A/D converters, the 8111 is an ideal solution for amplifying and down-converting antenna signals for communications, radar and signal intelligence systems.

Programmable Input Level

The 8111 accepts RF signals on a front panel SMA connector. An LNA (Low Noise-figure Amplifier) is provided along with two programmable attenuators allowing downconversion of input signals ranging from -60 dBm to -20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

Preselector Options

Seven different input-frequency band options are offered, each tunable across a 400 MHz band, with an overlap of 100 MHz between adjacent bands. As a group, these seven options accommodate RF input signals from 800 MHz to 3.000 GHz as follows:

<table>
<thead>
<tr>
<th>Option</th>
<th>Frequency Band</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>800-1200 MHz</td>
</tr>
<tr>
<td>002</td>
<td>1100-1500 MHz</td>
</tr>
<tr>
<td>003</td>
<td>1400-1800 MHz</td>
</tr>
<tr>
<td>004</td>
<td>1700-2100 MHz</td>
</tr>
<tr>
<td>005</td>
<td>2000-2400 MHz</td>
</tr>
<tr>
<td>006</td>
<td>2300-2700 MHz</td>
</tr>
<tr>
<td>007</td>
<td>2600-3000 MHz</td>
</tr>
</tbody>
</table>

Tuning Accuracy

The 8111 uses a low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy, its frequency is programmable across the 400 MHz band with a tuning resolution of 1 MHz. Alternatively, for applications demanding custom local oscillator characteristics, an external LO input signal can be accepted on a front panel connector and used instead of the on-board frequency synthesizer.

On-board Reference Clock

In addition to accepting a reference signal on the front panel, the 8111 includes an on-board 10 MHz crystal oscillator which can be used as the reference to lock the internal LO frequency synthesizer.

This reference is an OCXO (Oven Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

IF Output

An 80 MHz-wide IF output is provided at a 225 MHz center frequency. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt and Onyx families.
Model 8111

Bandit Modular Analog RF Slot Downconverter Series

Specifications

RF Input
Connector Type: SMA
Input Impedance: 50 ohms
Input Level Range: -60 dBm to -20 dBm
Flatness: ±1 dB typical over each 400 MHz range
RF Attenuator: Programmable from 0 to 31.5 dB in 0.5 dB steps

LO Synthesizer Tuning
Frequency range: 800-3000 MHz, across seven different options
Resolution: 1 MHz
Tuning Speed: < 500 µsec
PLL Loop Bandwidth: 100 kHz
Phase Noise
1 kHz: -90 dBc/Hz
100 kHz: -110 dBc/Hz
1 MHz: -130 dBc/Hz
Noise Figure (referred to input)
60 dB gain: 2.6 dB
Inband Output IP3
20 dB gain: +10 dBm
60 dB gain: +42 dBm
Reference/External LO Input
Connector Type: SMA
Input Impedance: 50 ohms
Reference Input Signal
Frequency: 10 MHz
Level: 0 dBm to +20 dBm, sinewave
External LO Input Signal
Frequency: fIN + 225 MHz, where fIN = RF input signal frequency
Level: 0 dBm ±2 dBm

IF Attenuator: Programmable from 0 to 31.5 dB in 0.5 dB steps
IF Output
Connector Type: SMA
Output Impedance: 50 ohms
Center Frequency: 225 MHz
Output Level: 0 dBm, nominal

Programming
Functions: RF Atten, IF Atten, Int/Ext LO Select, LO Synthezier Frequency Interface: USB
Connector Type: MicroUSB

Power
Voltage: +12VDC
Current: 1.5 A
Connector Type: Micro DB-9, female
Size: Module, 3.75 in x 7.5 in x 0.7 in

OCXO Reference Output
Connector Type: SMA
Center Frequency: 10 MHz
Output Impedance: 50 ohms
Output Level: +10 dBm, nominal, sine wave
Frequency Stability vs. Change in Temperature: ±50.0 ppb
Frequency Calibration: ±1.0 ppm
Aging
Daily: ±10 ppb/day
First Year: ±300 ppb
Total Frequency Tolerance (20 years): ±4.60 ppm
Phase Noise
1 Hz Offset: -67 dBc/Hz
10 Hz Offset: -100 dBc/Hz
100 Hz Offset: -130 dBc/Hz
1 KHz Offset: -148 dBc/Hz
10 KHz Offset: -154 dBc/Hz
100 KHz Offset: -155 dBc/Hz

Ordering Information

Model | Description
---|---
8111 | Bandit Modular Analog RF Slot Downconverter

Option | Input Frequency Band
---|---
-001 | 800-1200 MHz
-002 | 1100-1500 MHz
-003 | 1400-1800 MHz
-004 | 1700-2100 MHz
-005 | 2000-2400 MHz
-006 | 2300-2700 MHz
-007 | 2600-3000 MHz
Model 8264

6U OpenVPX Development System for Cobalt and Onyx Boards

General Information

The Model 8264 is a fully-integrated, 6U VPX development system for Pentek Cobalt® and Onyx® software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 9U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt and Onyx analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The 8264 uses a 19” 9U rackmount chassis that is 16” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

All 8264 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8264 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multicore CPUs and choice of Windows or Linux.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 16 GB
Dimensions: 6U Chassis, 19” W x 16” D x 10.5” H
Weight: 50 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: –40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model Description
8264 6U VPX Development System for Cobalt and Onyx Boards
Options:
-094 64-bit Linux OS
-095 64-bit Windows 7 OS

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
General Information

The Model 8266 is a fully-integrated PC development system for Pentek Cobalt®, Onyx® and Flexor™ PCIe Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces.

The 8266 can be configured with 64-bit Windows or Linux operating systems.

The 8266 uses a 19” 4U rackmount chassis that is 21” deep. Enhanced forced-air ventilation assures adequate cooling for Pentek Cobalt, Onyx and Flexor boards.

The chassis is designed to draw cool air from the front and push warm air out the back. A 1000 W, 80+ Gold Power Supply guarantees more than enough power for additional boards.

Configuration

Pentek uses a variety of motherboards to provide the flexibility for operation and cooling of each system. Up to four Pentek Cobalt, Onyx or Flexor boards in the 8266 can be supported. Please contact Pentek to configure a system that requires additional PCIe slots for 3rd party hardware.

Options

Options for high-end multicore CPUs and extended memory support applications that require additional horsepower are available.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 8 GB
Dimensions: 4U Chassis, 19” W x 21” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model   Description
8266    PC Development System for PCIe Cobalt, Onyx and Flexor Boards

Options:
-094    64-bit Linux OS
-095    64-bit Windows 7 OS
-101    Upgrade to 64 GB DDR3 SDRAM

The addition of third-party PCIe cards may affect system performance. Please consult with us before doing so.

Pentek, Inc. One Park Way ● Upper Saddle River ● New Jersey 07458
Tel: 201-818-5900 ● Fax: 201-818-5904 ● Email: info@pentek.com

www.pentek.com
General Information

The Model 8267 is a fully-integrated, 3U VPX development system for Pentek Cobalt®, Onyx® and Flexor™ software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

ReadyFlow Software

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over hardware, and Pentek’s Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

System Implementation

Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The 8267 uses a 19” 4U rackmount chassis that is 12” deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards. Mounting provisions for two 3.5 in. drives with front-accessible trays allow for easy removable storage. Front-panel access to USB, display, Ethernet and RS-232 ports simplifies development; an optional rear transition module supplements the front-panel connections with SATA, audio, a second video interface, and additional USB ports.

Configuration

All 8267 systems come with software and hardware installed and tested. Up to seven Pentek boards in the 8267 can be supported. Please contact Pentek to configure a system that matches your specific requirements.

Options

Available options include high-end multi-core CPUs and extended memory support.

Specifications

Operating System: 64-bit Windows 7 Professional or Linux
Processor: Intel Core i7 processor
Clock Speed: 3.6 GHz
SDRAM: 8 GB standard, 16 GB optional
Dimensions: 4U Chassis, 19” W x 12” D x 7” H
Weight: 35 lb, approx.
Operating Temp: 0° to +50° C
Storage Temp: -40° to +85° C
Relative Humidity: 5 to 95%, non-condensing
Power Requirements: 100 to 240 VAC, 50 to 60 Hz, 1000 W max.

Ordering Information

Model  Description
8267  3U VPX Development System for Cobalt, Onyx and Flexor Boards

Options:
-094  64-bit Linux OS
-095  64-bit Windows 7 OS
-101  Upgrade to 16 GB DDR3 SDRAM

The addition of third-party VPX boards may affect system performance. Please consult with us before doing so.
Customer Information

Placing an Order

When placing a purchase order for Pentek products, please provide the model number and product description. You may place your orders by letter, telephone, email or fax; you should confirm a verbal order by mail, email or fax.

All orders should specify a purchase order number, bill-to and ship-to address, method of shipment, and a contact name and telephone number.

U.S. orders should be made out to Pentek, Inc. and may be placed directly at our office address, or c/o our authorized sales representative in your area.

International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We're glad to respond to your request for price quotation just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

Quantity discounts for large orders are available and will be included in our price quotation, if applicable.

Terms

Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

Shipping

For new orders, we normally ship UPS ground with shipping charges prepaid and added to our invoice. If you are in a hurry, we will ship UPS Red, UPS Blue, FedEx, or the carrier of your choice, as you request.

Order Cancellation and Returns

All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to the buyer, except for products returned from outside the USA.

Limitations of Warranty

This warranty does not apply to products which have been repaired or altered by anyone other than Pentek or its authorized representatives.

The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions, that fall outside of the scope of the product’s environmental specifications.

Due to the normal, finite write-cycle limits of Solid State Drives (SSDs), Pentek shall not be liable for warranty coverage of SSDs caused by wear-related issues that arise as an SSD reaches its write-cycle limit.

Pentek specifically disclaims merchantability or fitness for a particular purpose. Pentek shall not be held liable for incidental or consequential damages arising from the sale, use, or installation of any Pentek product. Regardless of circumstances, Pentek’s liability under this warranty shall not exceed the purchase price of the product.

Extended Warranty

You may purchase an extended warranty on our board-level products for a fee of 1% of the list price per month of coverage, or 10% of the list price per year of coverage.

All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

You must obtain a Return Material Authorization (RMA) before returning any product to Pentek for service or repair. RMA requests must be submitted online at: Return Material Authorization Form

After the form is completed in its entirety and submitted, Pentek shall email you a receipt and start processing your request. Once your request has been approved, Pentek shall e-mail you an RMA number, shipping instructions, and a quotation if the product is out of warranty.

Carefully package the product in its original packaging, if it is still available, and ship it to Pentek prepaid (if within the US) or free domicile DDP (if outside the US). Pentek shall not be responsible for loss or damage in shipment to Pentek, so you are strongly encouraged to insure the shipment for its full replacement value.

When the work is completed, we will return the product to you along with a statement of work performed.

Customer Service phone: 201-818-5900 • fax: 201-818-5697 • email: custsvc@pentek.com