Model 4954-440 GateFlow IP Core

GateFlow Pulse Compression IP Core

For more information and free IP core evaluation go to:
pentek.com/fpga

Features

- Supports Virtex-II™, Virtex-II Pro™, and Spartan-3™ FPGAs
- 155 MHz maximum clock with Virtex-II Pro FPGA
- High-resolution block floating-point calculation using 16, 20 or 24-bit math
- FFT block sizes from 64 to 16384 points
- Complex block floating-point output formats: 16-, 20-, or 24-bit integer plus 6-bit exponent
- Matched filter reference may be entered in time or frequency domain
- Matched filter reference may be changed before processing each pulse, or may be stored and reused
- MatLab pulse compression utility functions included
- ModelSim VHDL test benches included
- Compatible with Xilinx Foundation ISE Tools
- Compatible with Pentek GateFlow FPGA Design Kit

Ordering Information

Model	Description
4954-440	Pulse Compression IP Core

Licensing of these cores follows the Xilinx SignOnce Project License. Simulation models can be downloaded for evaluation.

General Information

The Pentek Model 4954 GateFlow Library IP Core 440 performs radar pulse compression by performing matched filtering using a Fast Convolution Processing (FCP) algorithm.

Pulse compression improves range resolution for radar systems by allowing the use of longer pulses to increase the average transmitted power and receiver SNR. The core is designed specifically for Xilinx Spartan-3, Virtex-II and Virtex-II Pro FPGAs.

Algorithm Description

An input FFT stage, programmable from 64 to 16k points, operates on the returned echo signal. The reference pulse spectrum can be entered directly into the Reference Pulse Spectrum RAM or computed from a reference pulse input using the input FFT. Either path allows the reference spectrum to be updated for each input pulse to support adaptive systems.

A complex multiplication is then performed on the complex conjugate of the reference spectrum and the input signal spectrum. The multiplier output block feeds an inverse FFT (IFFT) to produce the compressed time domain output pulse.

All sections of the core utilize block floating point computation in order to maximize dynamic range and eliminate the need to scale data in the FFT sections. The output is a time domain compressed pulse, represented as a 16-, 20-, or 24-bit integer part and a 6-bit block exponent reflecting total end-to-end scaling.

Flexible Architectures

Two different architectures are available, one optimized for minimal FPGA resources, and one optimized for maximum throughput. The former uses a single, time-shared engine for both the input FFT and the IFFT, while the latter uses two separate engines resulting in twice the maximum frame rate at the expense of additional FPGA resources.

Within each architecture, four maximum FFT size versions are available: 2k, 4k, 8k and 16k points. Each version may be adjusted during operation to accommodate binary FFT sizes from 64 samples up to the maximum size. Also, each architecture is configurable with three data resolutions: 16, 20 and 24 bits.

Speed Performance

Operational speed of the core also depends on these same factors (architecture version, maximum FFT size and resolution), but additionally on the speed grade of the Xilinx FPGAs.

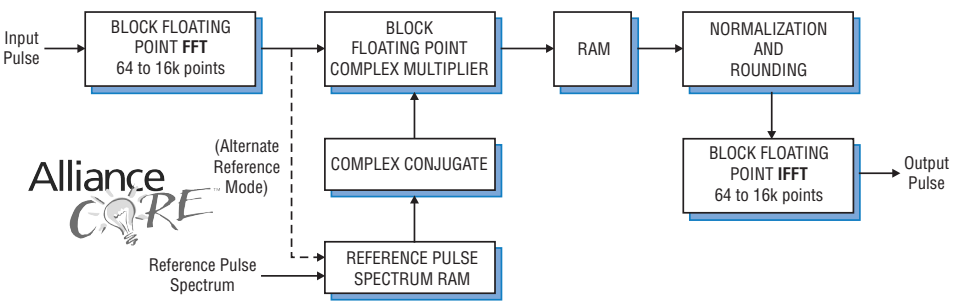
The chart below shows the maximum clock speed and the minimum frame-to-frame period between two consecutive input data frames using 24-bit resolution.

	Maximum Throughput		Minimal Resource	
Speed Grade	-5	-7	-5	-7
Max Clk (MHz)	122	155	122	155
Minimum Frame Spacing (µsec)				
64 points	2.00	1.57	4.02	3.16
512 points	14.09	11.09	28.21	22.21
8k points	252.4	198.6	504.7	397.3

Resource Utilization

FPGA resource utilization is shown below for four of the 24 combinations of the two architectures (maximum throughput or minimal resource), maximum FFT sizes (2k, 4k, 8k, and 16k) and bit resolutions (16, 20 and 24).

	Maximum Throughput		Minimal Resource	
FFT size	16k	2k	16k	2k
Resolution-bits	24	16	24	16
Slices	10,166	5,527	6,072	3,202
Slice LUTs	12,995	7,277	7,708	4,168
Slice FFs	13,503	6,732	7,936	3,902
Block RAM	253	26	191	19
Block Mults	88	22	52	13
Global Clocks	1	1	1	1



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