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FPGAs Drive Digital I/O Solutions

FPGAs are particularly well suited to handle not only the digital I/O requirements for a range of popular interfaces, but also to support complex protocols and extended signal processing functions for embedded systems.

by Rodger Hosking, Vice President and Co-Founder, Pentek

Digital I/O is unquestionably one of the most common requirements for real-time embedded systems, representing a vast assortment of interfaces and protocols. These devices connect process control sensors, audio and ultrasonic transducers, imaging devices and cameras, wideband data acquisition and generation systems for communications and radar, and detectors for high-energy physics applications. In addition, these embedded systems must connect to other systems for networking, control, recording and high-speed data transfer.

Traditionally, these interfaces required dedicated ASICs to handle the electrical connections and the protocol processing. Today, both of these aspects are nicely handled by the latest generation of FPGAs with configurable I/O, logic and processing elements.

System Requirements

Digital I/O generally defines a device that interfaces with a very specific peripheral and then connects that peripheral to standard buses or links within the application system. Figure 1 shows a generic system architecture for contemporary processors and chip sets.

Digital I/O products, like most expansion cards, connect to the system using PCIe (PCI Express). This applies to PC-based systems with motherboards with multiple PCIe card slots, as well as the newer card cage standards such as VPX and CompactPCI Serial where PCIe links join the boards across the backplane. The same applies to single board computers (SBCs) through mezzanine or daughter card connections like XMC.

Using this system view, it is clear that the digital I/O card must provide the specialized interface to the peripheral, and it must communicate through a PCIe engine to the rest of the system. The card uses PCIe for all the required control and status functions for the peripheral, as well as streaming data to and from the peripheral. Software drivers for the card must be developed in compliance with the CPU operating system.

FPGAs: The I/O Superstars

FPGAs fill the bill for digital I/O functions better than any other component. For example, the Xilinx Virtex-6 FPGA supports many different types of single-ended CMOS outputs with push-pull drivers equipped with high-impedance tri-state enables. In addition, both the output current and slew rate can be specified to meet special I/O requirements. Voltage compliance levels for input and output range from 1.2V to 2.5V.

Supported differential standards include LVDS, HT, RSDS, BLVDS, differential SSTL and differential HSTL, and are capable of handling bit rates up to 800 MHz. Since many of these standards are used for bidirectional traffic, Xilinx provides digitally controlled series output impedance and Thevenin-equivalent input termination for maximum signal integrity in both directions. Not only does this reduce the number of external components, but it also saves power because the active input termination can be turned off when the device is in output mode.

In most cases the direct electrical lines or optical links to the connected peripheral will be buffered, translated or converted with special devices matched to the peripheral. This provides full compliance to safety, shock, over-voltage and static discharge, while protecting the FPGA from damage. The flexibility of the FPGA I/O pins allows compatibility with virtually every type of interface chip.

Because many digital interfaces use serial streams, another benefit of FPGAs are the extremely fast serial interface engines combining receiver and transmitter functions and parallel/serial converters handling word widths of 16, 20, 32, or 40 bits with bit rates as high as 6.6 GHz in the Virtex-6 GTX transceivers. These engines include PLL clock generation and clock/data encoding and decoding support for 8B10B and 64B66B traffic, and also feature dynamic feedback equalizers to compensate for signal channel characteristics.

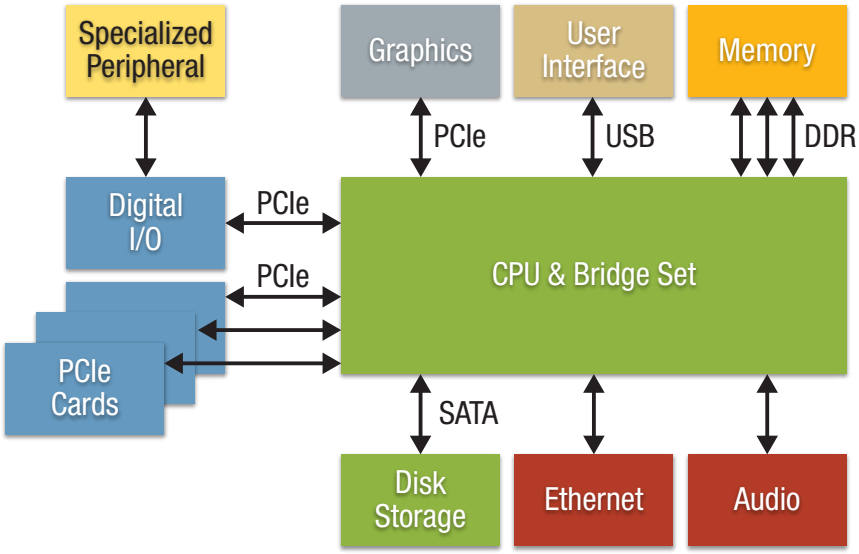

FIGURE 1

Generic embedded system showing digital I/O connectivity.

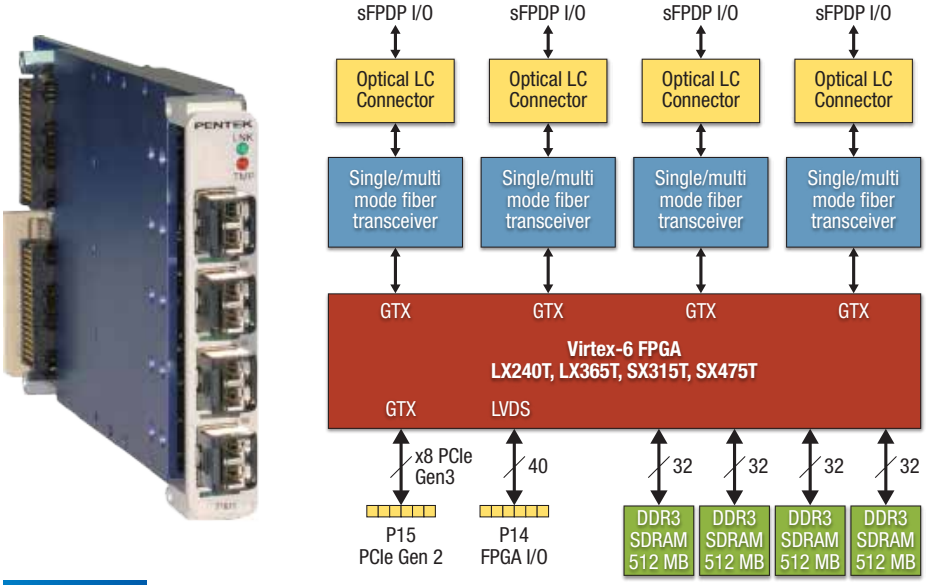

FIGURE 2

Pentek Model 71611 Quad sFPDP Transceiver XMC Module.

Integrated PCIe Interfaces

Because the system side of the digital I/O card is almost always PCIe, FPGAs simplify designs with their integrated PCIe interface engines for endpoints. In the Virtex-6 devices from Xilinx, the speed of the PCIe engines is compliant with PCIe Gen 2 delivering a transfer rate of 4 Gbyte/s for a x8 PCIe interface to take advantage of the wealth of PCIe Gen 2 motherboards and embedded SBCs now available.

While not every application needs such extreme speeds, many peripherals, such as high-resolution imaging devices and wideband A/D and D/A converters, are driving toward increasingly higher data rates.

Serial FPDP

As one example of a popular digital I/O standard, Serial Front Panel Data Port (sFPDP) is defined in the VITA 17.1 specification as the serial implementation of the older parallel FPDP standard used to connect digital devices across a 32-bit parallel flat ribbon cable. Because of its relative simplicity, sFPDP offers a fast, efficient, bi-directional point-to-point interconnect solution. Applications such as industrial sensors, medical imaging and wideband data acquisition can take advantage of this high-throughput, minimum-latency protocol.

Data is encoded in groups of four 8B10B (10-bit) fields to support 32-bit data transfers, channel balance, clock recovery and control codes. The control codes are a subset of Fibre Channel ordered sets and include IDLE, start of frame (SOF), end of frame (EOF), sync with data valid (SWDV), GO and STOP. A data frame can contain from 0 to 512 32-bit words.

Bit rates (baud rate) for sFPDP may be 1.0625, 2.125, or 2.5 GHz, resulting in data payload rates of 105, 210 and 247 Mbyte/s, respectively. The sFPDP specification does not restrict the cable type and offers many different candidates for both copper and optical media.

The sFPDP links can be unidirectional or full duplex, where the reverse channel serves as a data channel, or handles flow control signaling to prevent overflow at the receiver, or both. The Copy mode allows one device to receive data and forward it to another device as in a daisy chain. Cycle redundancy check (CRC) is supported, but optional.

Even though sFPDP is a relatively lightweight protocol, it still requires control code detection and generation, frame detection and generation, flow control management, CRC processing, packet validation and acknowledgement, and error detection and recovery.

These functions are ideally suited for the hallmark resources of FPGAs—logic elements, arithmetic blocks and state machines. In addition, the integrated serial transceivers simplify the 8B10B coding as well as the clock and data generation and recovery. The ability to reconfigure these FPGA resources to match the specific requirements of the peripheral protocol and functions allows designers to accommodate additional features such as custom signal processing for both inbound and outbound data streams.

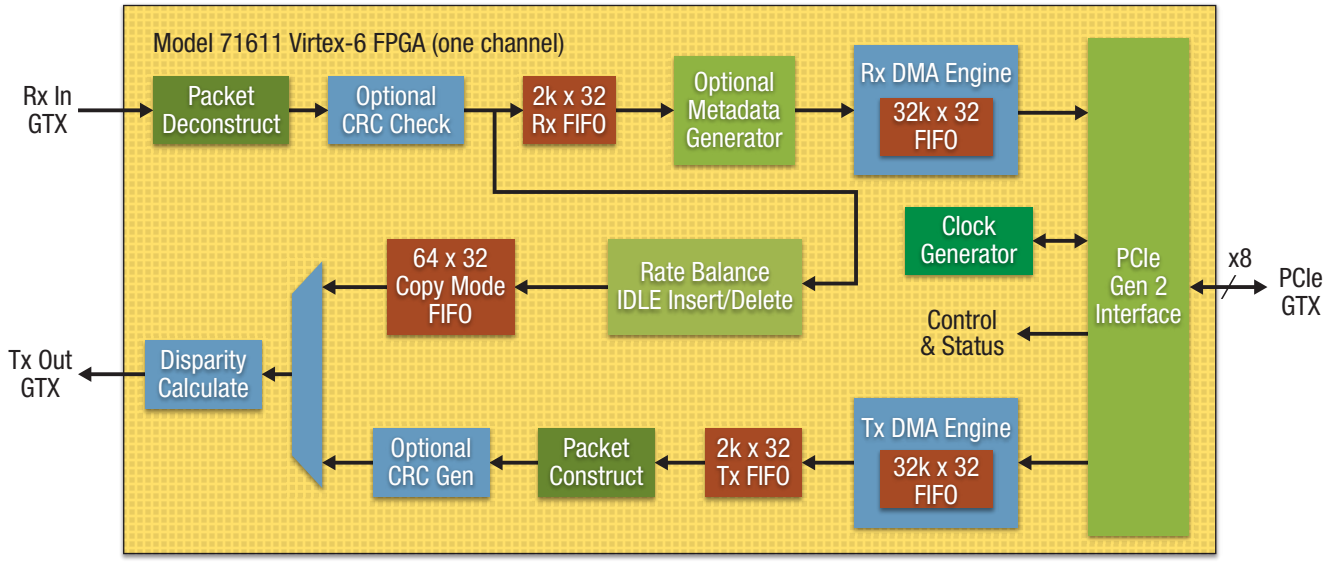

FIGURE 3

Simplified data flow and FPGA structures for sFPDP (one of four identical channels shown).

Serial FPDP XMC Module

One example of an FPGA-based sFPDP product is the Pentek 71611 Quad sFPDP XMC module. Based on the Xilinx Virtex-6 FPGA, it offers four independent full-duplex sFPDP ports using optical cable with standard LC connectors. The XMC form factor with its PCIe system interface is the most popular mezzanine card format because it can be used in virtually all types of embedded systems including PCI, PCIe, VME, VPX and CompactPCI.

Figure 2 illustrates the simplicity of the hardware implementation, made possible because virtually all circuitry is inside the FPGA. Four optical transceivers and the PCIe interface lines are attached directly to the GTX gigabit serial ports of the Virtex-6 device. All 8B10B encoding and decoding for sFPDP are handled in these hardware structures.

Optional external SDRAM memory arranged as four banks of 512 Mbyte each are not required in the standard product, but are optionally available for custom FPGA algorithms installed by developers.

Taking a closer look inside the FPGA, Figure 3 shows the data flow and major processing sections for one of the four identical sFPDP channels. The PCIe interface engine on the right supports configuration and status of the module from the host computer to set the mode of operation and track transfer operations. It also handles streaming data transfers for all sFPDP traffic.

Four receive (Rx) DMA controller engines move receive data from the module into system memory tables at locations specified in a user-defined linked list. This allows automated data delivery to one or more buffers with interrupt signaling to the host when each buffer is complete. Four transmit (Tx) DMA engines pull data from system memory into the module for transmission using the same scheme. This method helps match all sFPDP data transfer operations to the software application they serve.

Because sFPDP supports a variable number of payload data words, the 71611 features a metadata generator that counts the number of words from the start of a transmission until the SWDV control character is detected. Any data in the DMA buffer is then immediately flushed to memory, and the counter value and the destination memory buffer address are optionally appended to the payload data. This allows payloads of any length spanning any number of frames to be received in full, identified in size and delivered to memory as complete entities.

The 71611 operates on any of the three bit rate clock frequencies defined in the sFPDP standard: 1.0625, 2.125, or 2.5 GHz. The rate is selectable in software through the PCIe interface, with a power on default rate specified when ordering.

Applications

One major advantage of sFPDP is the relatively small size and light weight of the copper or optical cables compared to bulkier parallel cables. In addition, optical cables offer complete immunity to EMI interference and radiation, so they are ideal for noisy electrical environments with heavy industrial machinery and for airborne installations with sensitive radio equipment.

Remote sensors can take advantage of single-mode fiber optical links to deliver sFPDP traffic across distances as great as 10 km. This can connect transducers in buildings or equipment sheds across large industrial installations such as refineries or mills with fast, dedicated low-latency links.

On board large commercial or military ships, sFPDP links can deliver sensor data to the bridge from multiple antenna masts including radar and communication systems, navigation systems and all other critical functions on the ship requiring high-speed links. Optical cables are highly resistant to water, salt and corrosion, making them perfect for marine installations.

Because FPGAs also include DSP blocks, they are well suited for high-performance signal processing functions on receive and transmit data streams. For example, real-time image processing algorithms might be performed on streaming

data from a camera, such as edge detection, noise reduction, motion detection or feature recognition.

Signals from A/D converters located near an antenna and fed down the mast through a sFPDP optical link could be processed with software radio functions including digital down conversion and filtering. The optional 2 Gbyte of DDR3 SDRAM is useful for implementing large memory buffers or delay blocks to support the needs of some applications.

Pentek offers its GateFlow FPGA Design Kit so customers can extend the factory-installed functions of the 71611 to add these new features, functions and algorithms. It contains complete VHDL source code and the entire Xilinx project for the product.

FPGAs are especially useful for digital I/O products because they contain nearly every resource to handle a wide range of interfaces through flexible I/O options. The configurable logic, state machines and DSP blocks handle complex protocol and signal processing tasks. The built-in gigabit serial interfaces handle the clock/data channel coding and equalization. Finally, the integrated PCIe interfaces simplify connection to the host processor and other system elements.

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