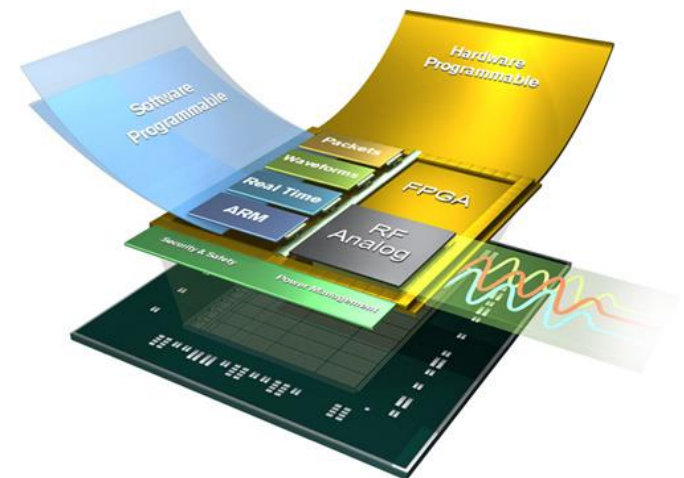


Strategies for Deploying RFSoc Technology for SIGINT, EW and Radar Applications



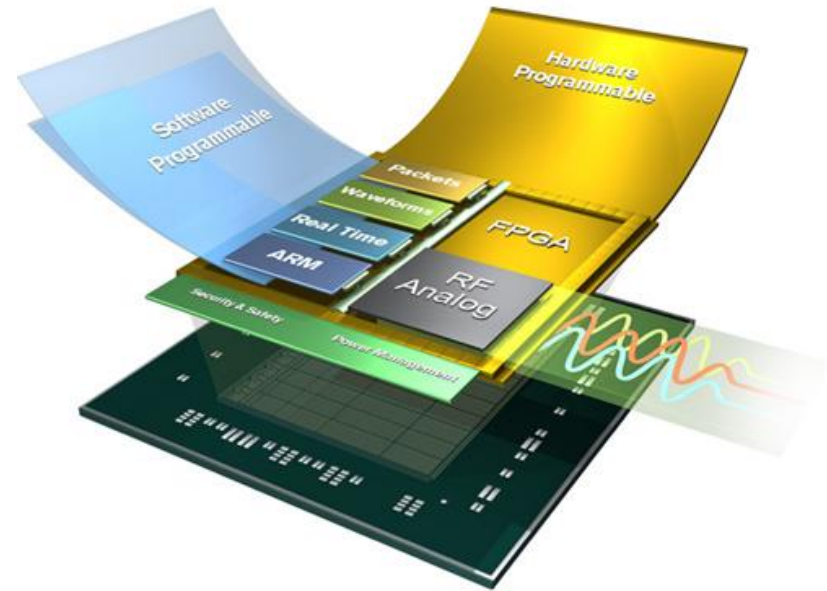
Fall 2018

*Rodger Hosking
Pentek, Inc.*



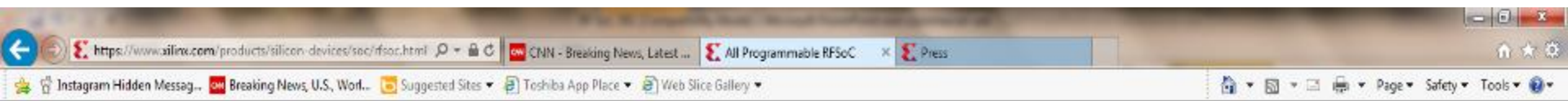
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February 2017: Xilinx Announced RFSoc



APPLICATIONS PRODUCTS DEVELOPER ZONE SUPPORT ABOUT

“Xilinx Unveils Disruptive Integration and Architectural Breakthrough for 5G Wireless with RF-Class Analog Technology”

Integrated RF-Class Analog
RF Data Converters in
an All Programmable MPSoC

White Paper Press Release IEEE Paper

Overview RF Sampling Documentation Developer Zone

RF Data Converters in an All Programmable MPSoC

Xilinx has integrated multi-giga-sample RF data converters into its 16nm MPSoCs devices for the industry's first All Programmable RFSoc. This eliminates the need for discrete ADCs and DACs and enables next-generation radio and RF communication systems to scale for power, footprint, and channel density requirements.

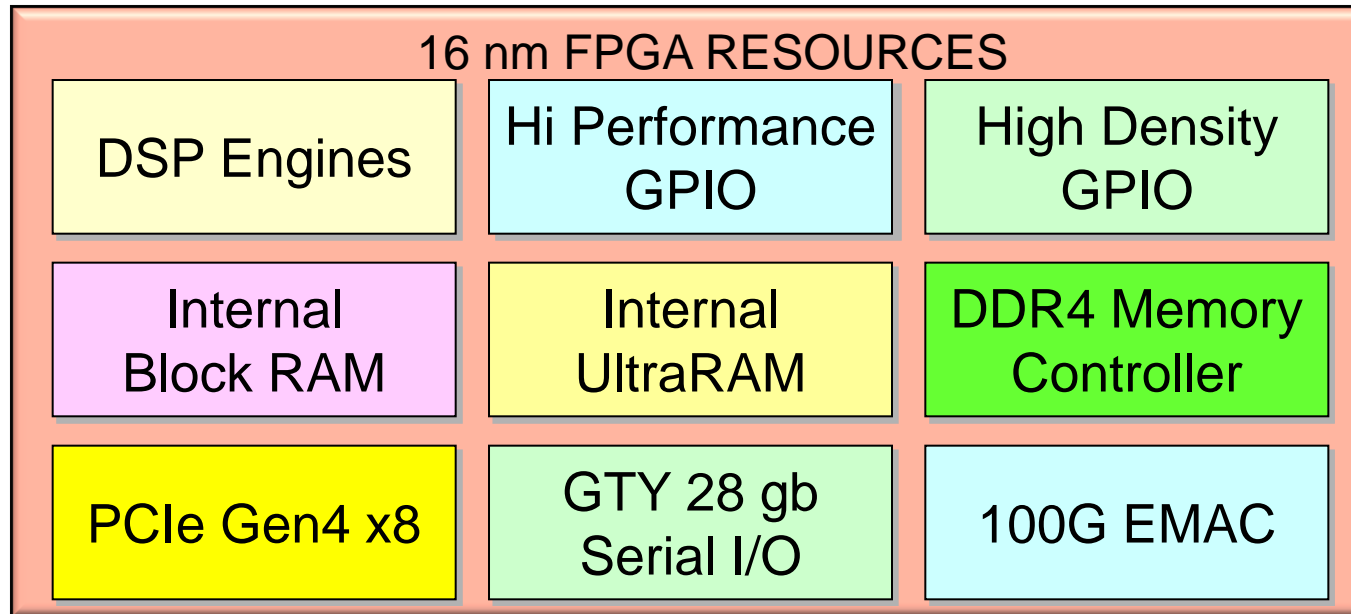
Value	Capabilities
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Xilinx UltraScale+ FPGA Fabric

- 16 nm Kintex FPGA Resources
- Advanced Real-Time Digital Signal Processing Engines
- Extensive General Purpose I/O for Peripherals

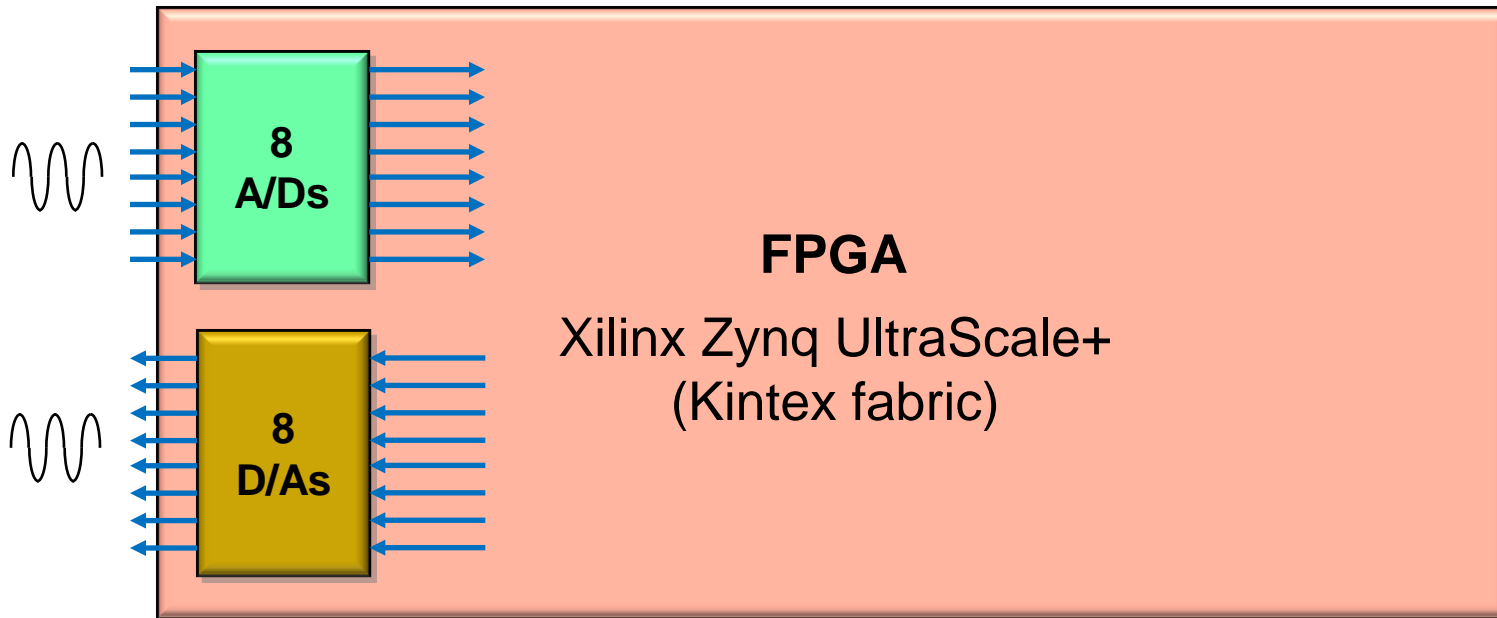


- Fast Internal Memory and Controller for External DDR4
- PCIe Gen4 x8 System Interface
- Enhanced 28 gb GTY Serial I/O and MAC for 100 GbE



Integrated Data Converters in the FPGA

- A/Ds and D/As are connected directly to FPGA fabric
- Lowest latency parallel interfaces

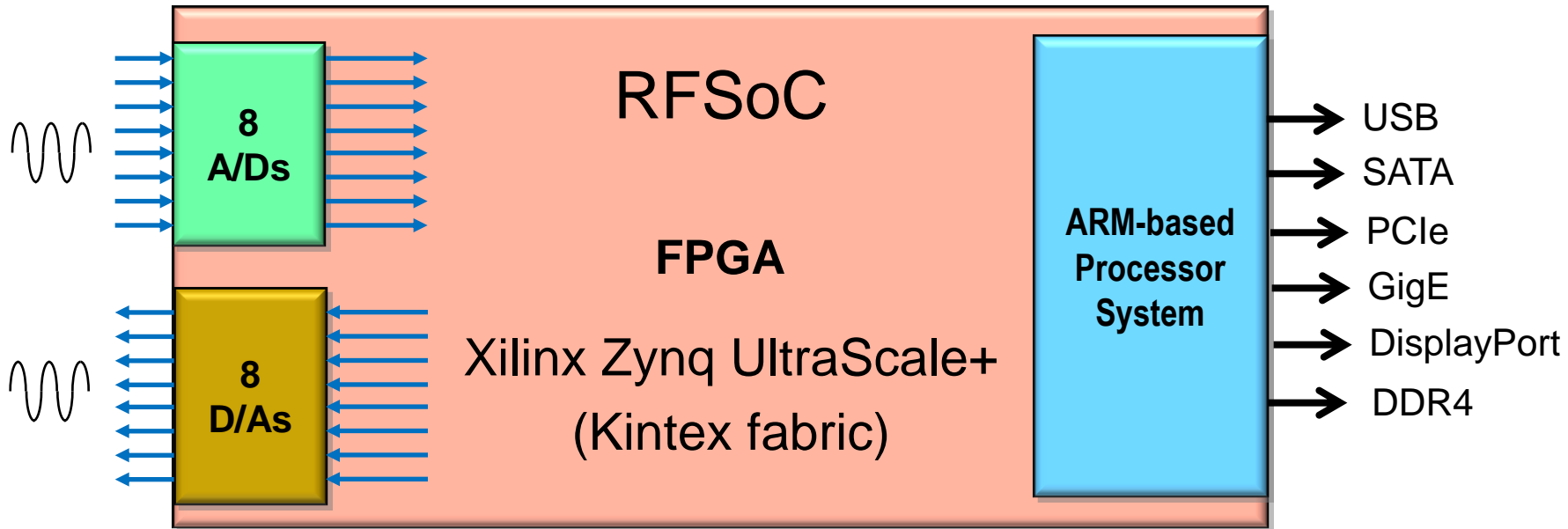


- 8 A/Ds: 12-bit, 4 GHz with integrated Digital Downconverters
- 8 D/As: 14-bit, 6.4 GHz with integrated Digital Upconverters



RFSoc – ARM-based Processor

- On-chip ARM-based MPSoC Processor System

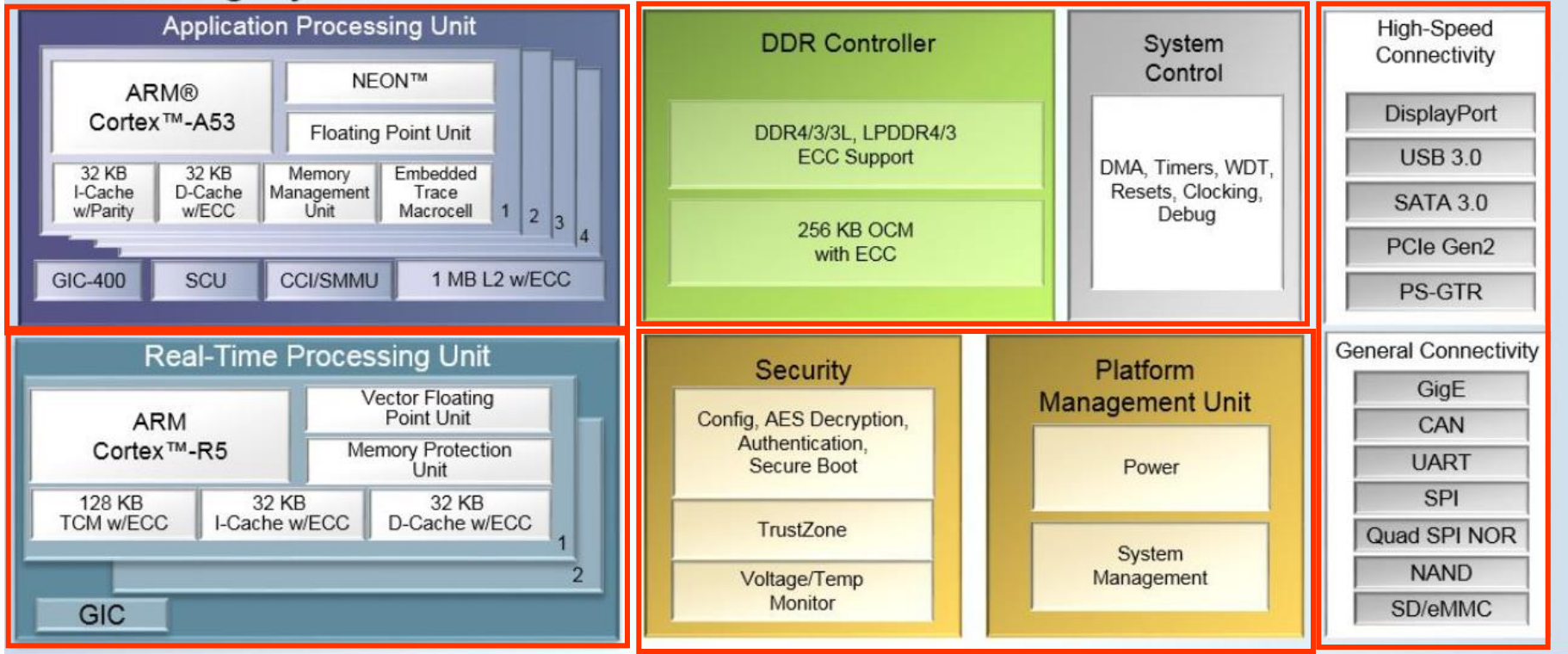




ARM Based Processor System

- Application Processor: Four 64-bit ARM Cortex-A53 cores
- Real-Time Processor: Two ARM Cortex-R5 real time cores

Processing System

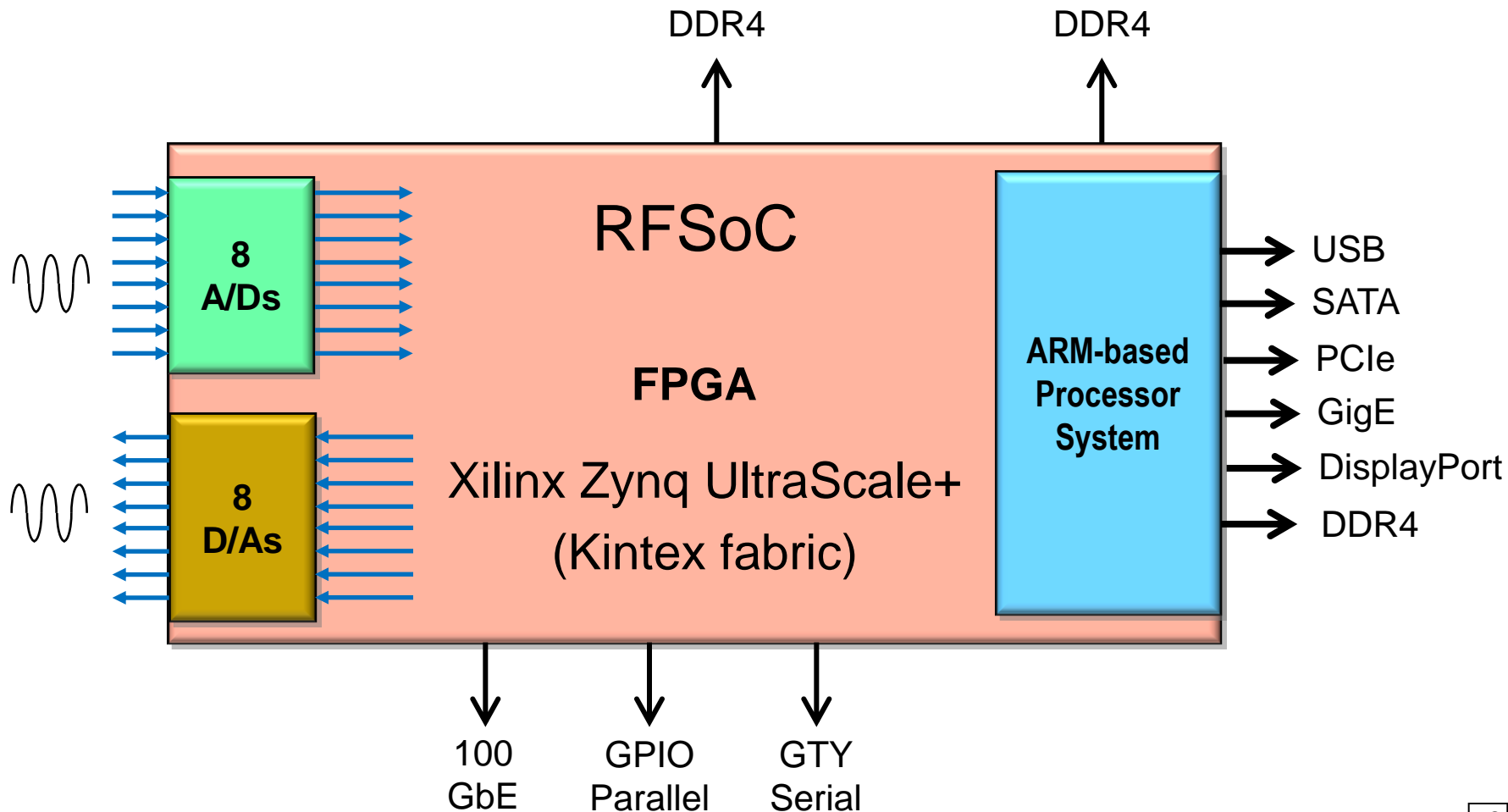


- DDR4 Memory Controller and System Controller
- Security Manager and Platform Management Unit
- High-Speed Connectivity and Processor I/O



RFSoc – Complete RF System on Chip

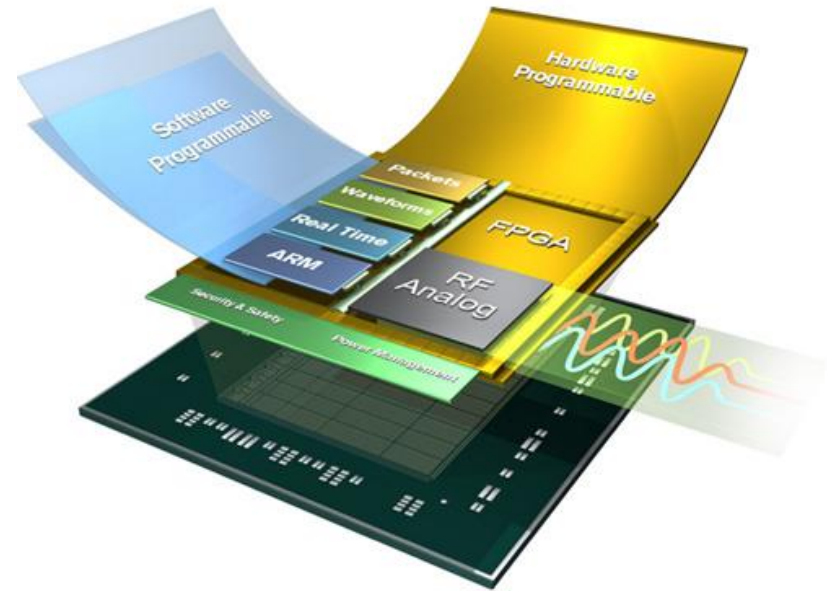
- Includes DDR4 memory Interfaces for FPGA Fabric and ARM Proc
- Includes 100GbE, LVDS Parallel, and Gigabit Serial Interfaces
- Complete sub-system on a single monolithic chip!





Topics

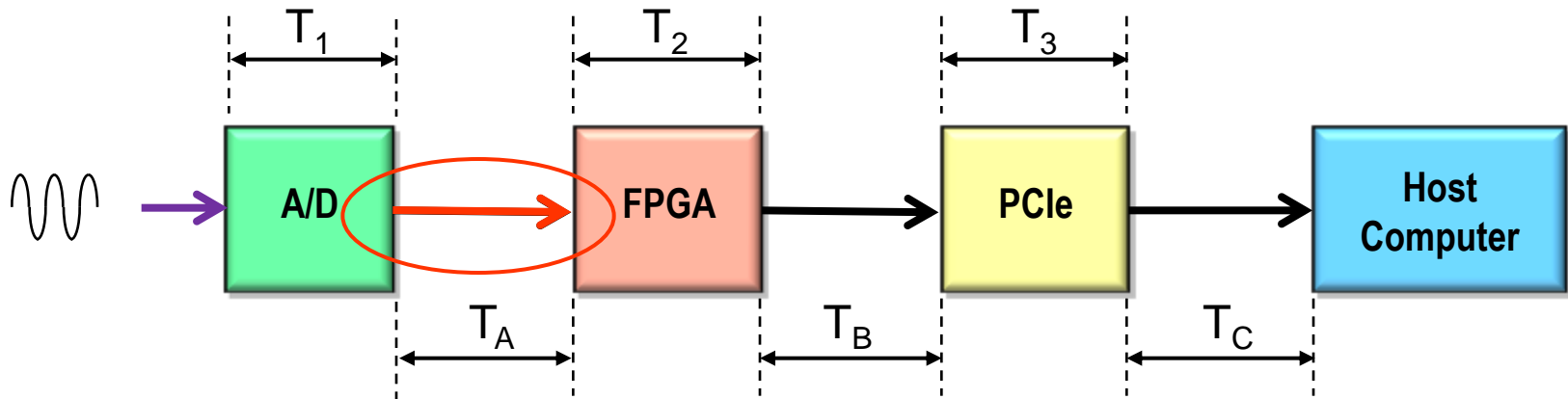
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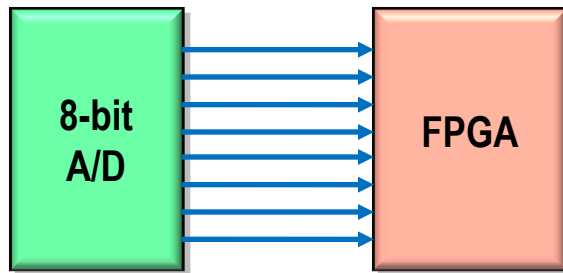
What Is Latency?

- Time delay through the system from input to output
- Includes delays within each element
- Includes delays in the links between each element
- Data converter links are becoming a critical limiting factor!





Parallel vs. Serial Converter Interfaces



Parallel connection (LVDS)

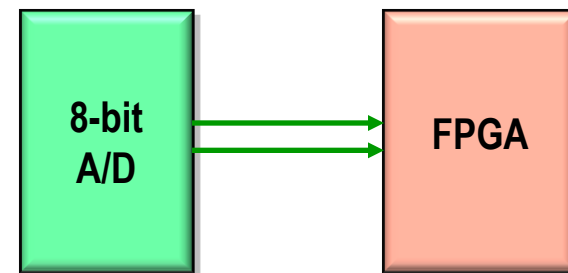
Pro

Simple
Low latency

Con

Limited speed

Many lines to route on PCB



Serial connection (JESD204B)

Pro

Can handle high speed A/Ds
Fewer lines to route on PCB

Con

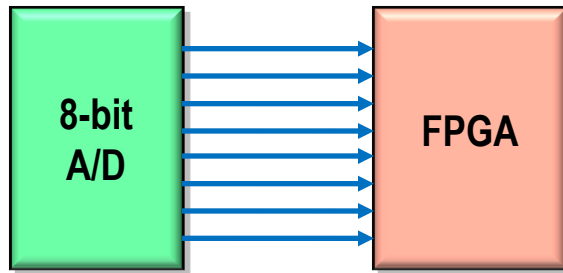
Complex to implement

Serial protocol introduces latency

- The latest and fastest discrete data converters use JESD204B
- JESD204B imposes a high latency interface



RFSoc – Eliminates All “Cons”



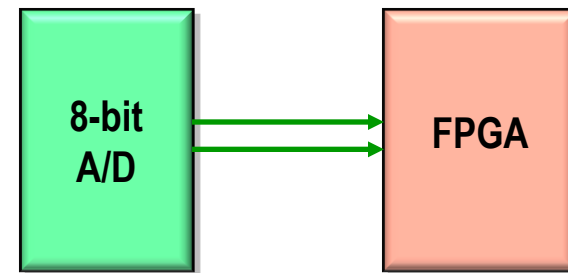
Parallel connection (LVDS)

Pro

- Simple
- Low latency

Con

- ~~Limited speed~~
- ~~Many lines to route on PCB~~



Serial connection (JESD204B)

Pro

- Can handle high speed A/Ds
- Fewer lines to route on PCB

Con

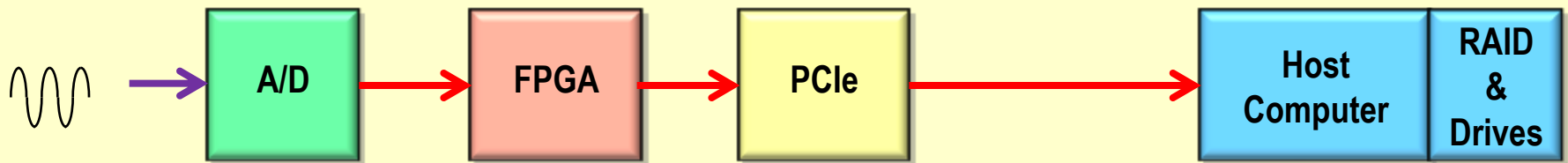
- ~~Complex to implement~~
- ~~Serial protocol introduces latency~~

- RFSoc Uses Parallel Data Converter Interfaces
 - Simplest Interface
 - Lowest Latency
- All A/D and D/A connections are internal to RFSoc chip
 - Eliminates Speed Limitations
 - Eliminates PCB lines



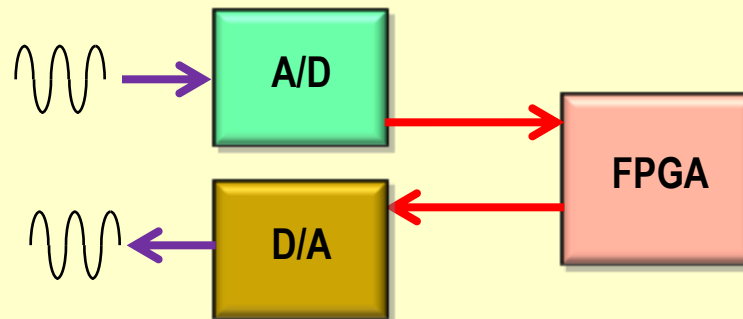
Applications and Data Transfer Latency

Application not affected by latency - Recording



Latency introduced by JESD204B not a problem

Application affected by latency – Countermeasures



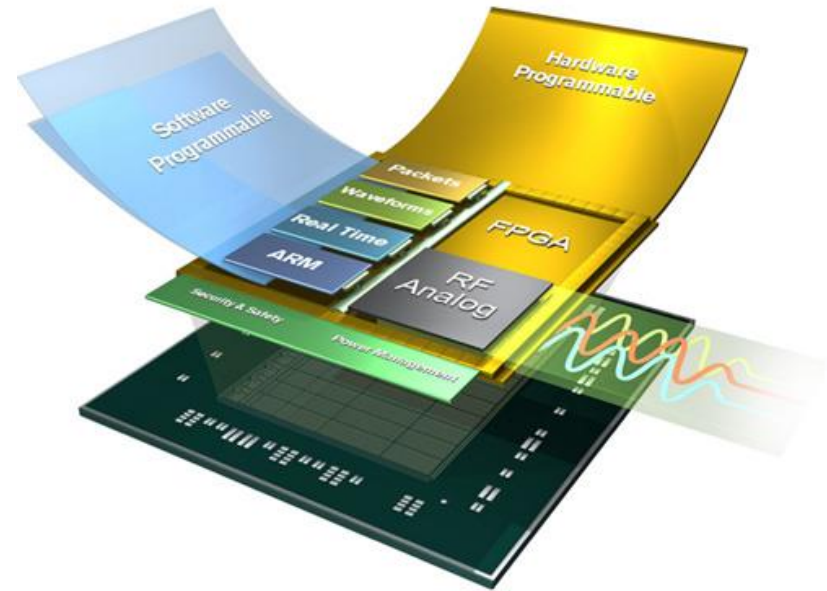
Latency introduced by JESD204B is a big problem!

- RFSoc Covers Applications for **ALL** Latency Requirements!



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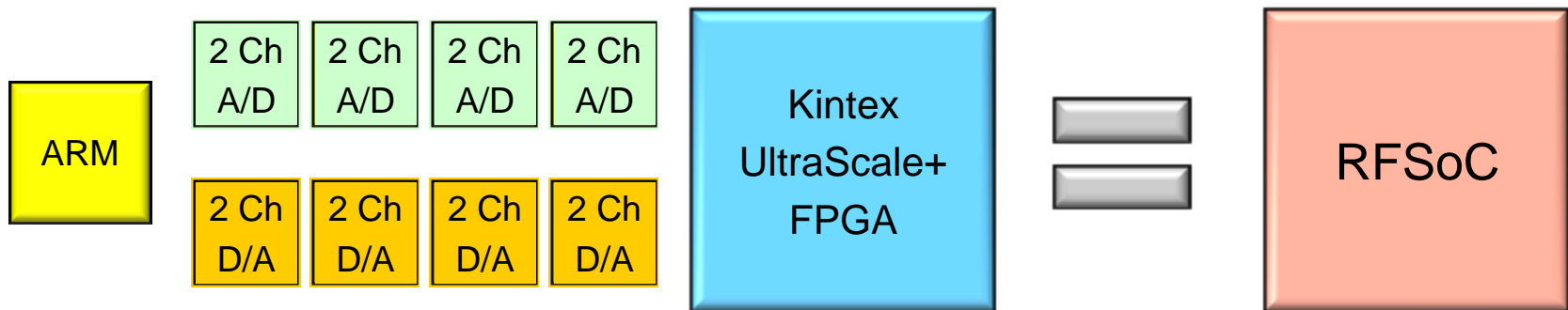
RFSoc Market Opportunities

- Radar
 - Multi-function Phased Array Radar (MPAR) initiative combines U.S. weather and radar networks
 - Common Module beamformer for DARPA Arrays Commercial Time Scales (ACT) program
- EW and Countermeasures
 - Low latency applications
- Communications
 - SATCOM and Military / Airborne Radios
- SIGINT
 - Monitoring, Interception, and Analysis
- 5G Wireless & Cable Remote PHY
 - Remote radio head for Massive-MIMO, wireless backhaul, and fixed wireless access
 - Implements DOCSIS 3.x PHY Spectral Efficiency requirements for distributed broadband digital networks



How Does RFSoc Change the Market?

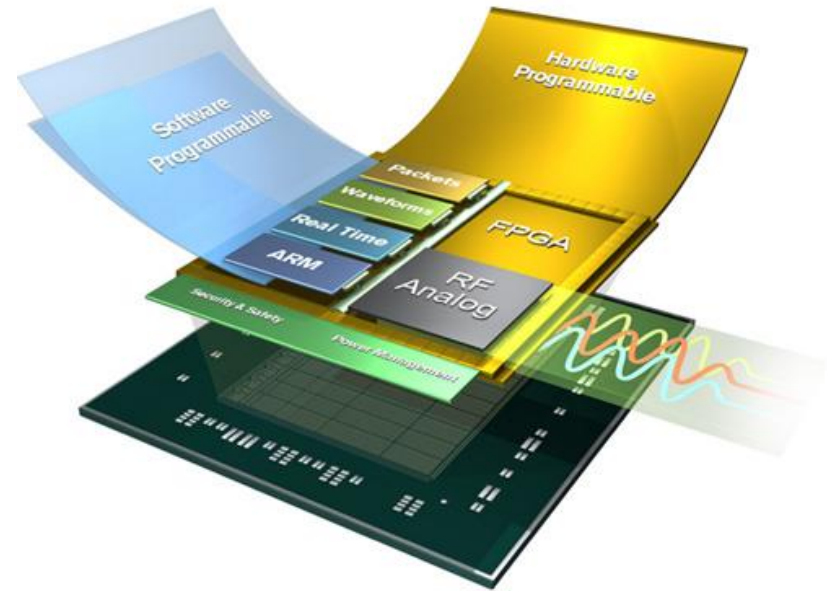
- Reduced size and footprint
 - About 50% less compared with discrete data converters, FPGA & processor
- Reduced power
 - About 30-40% total power savings
- Reduced cost
 - About 40-60% total cost savings
- Reduced latency
 - About 80-90% less delay than JESD204 data converters





Topics

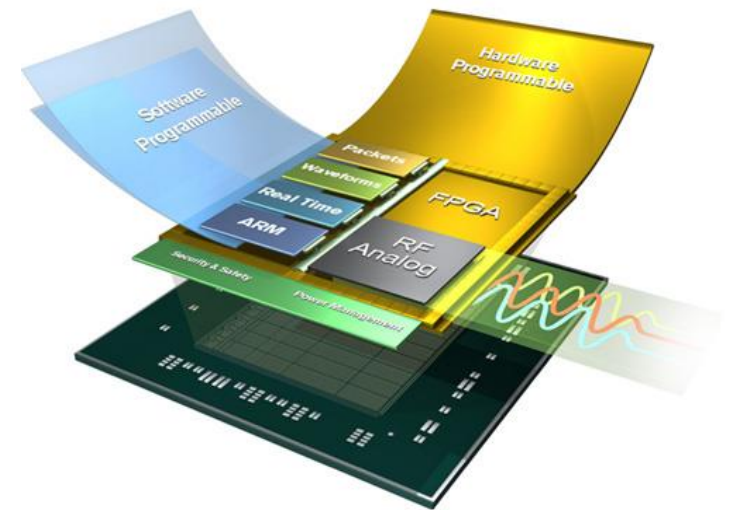
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RFSoc: Board Level Design Issues

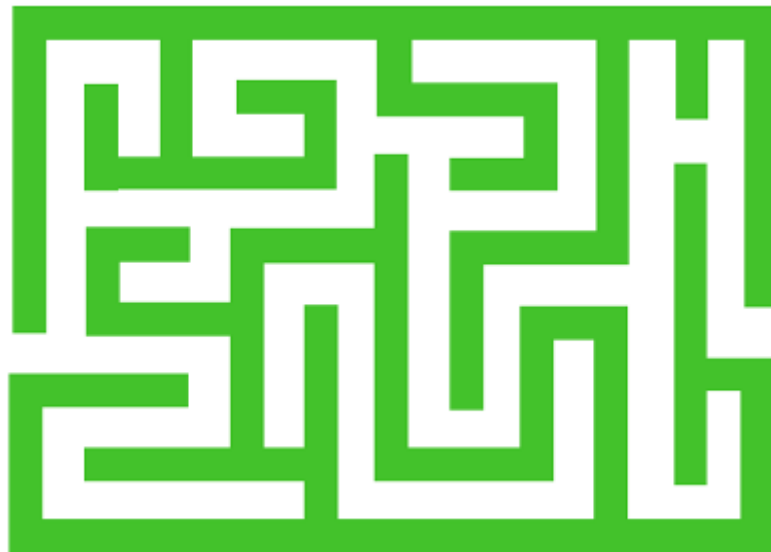
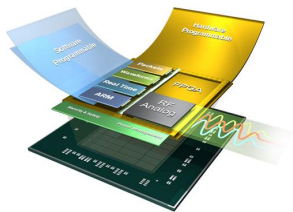
- RF Signal Integrity
 - 16 Analog RF Signals with GHz Bandwidths
 - Spurious digital signal pickup
 - Crosstalk between analog channels
 - Signal path integrity and impedance
- Gigabit Serial Links – 28 Gbit GTY
 - Signal path integrity and impedance
 - Bit error rate considerations
- Clock Management
 - Data Converter Sample Clocks
 - FPGA Fabric and Gigabit Serial Links
- Power Supply Requirements
 - RFSoc chip requires 13 different power supplies
 - Analog supplies must be extremely clean
- Thermal Management
 - Air- or conduction-cooling provisions





Design Strategies for RFSoc

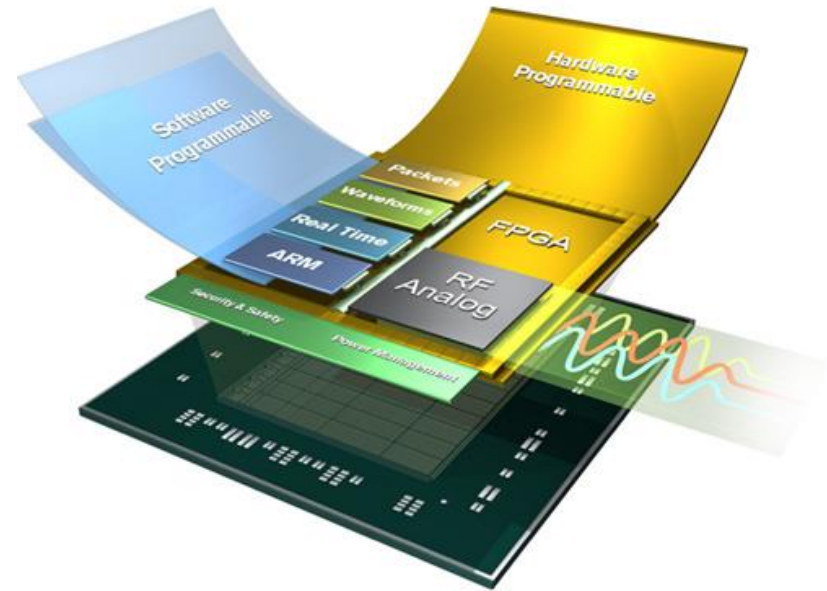
- What's the shortest path from RFSoc chip to Deployed Product?
 - Hardware Strategies
 - System Integration Strategies
 - FPGA Design Strategies
 - ARM Processor Software Development
- How can I get a running start?





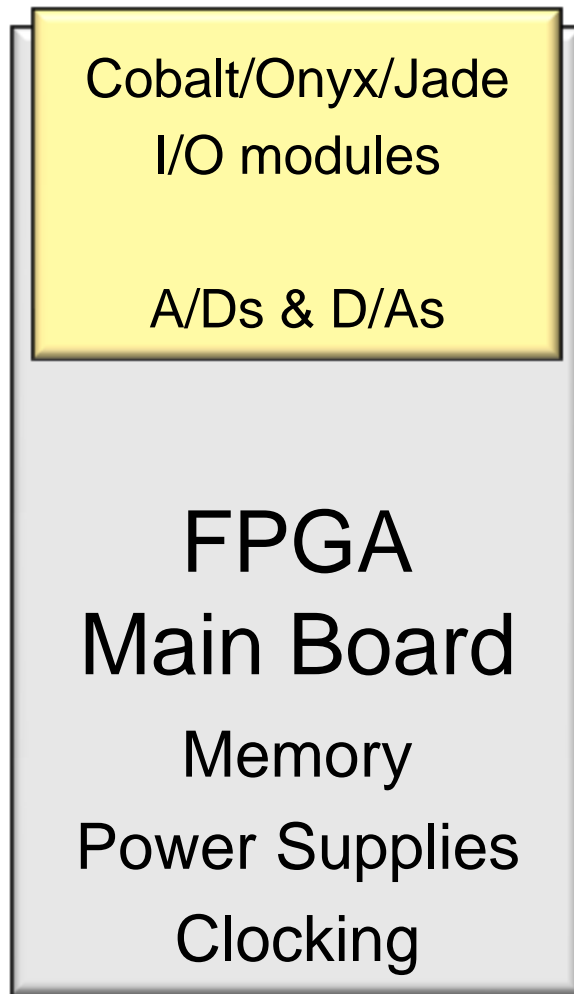
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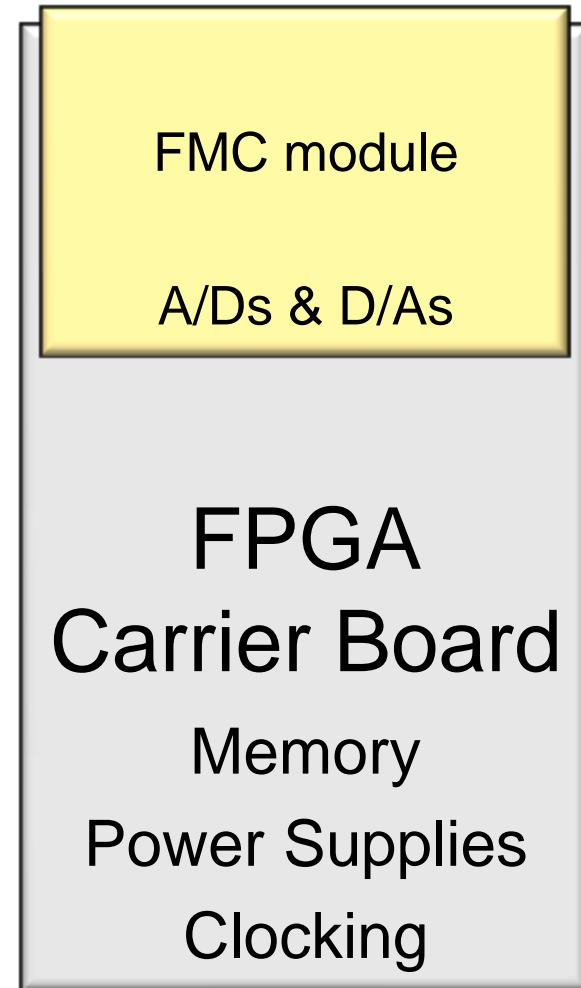




Traditional Modular Designs



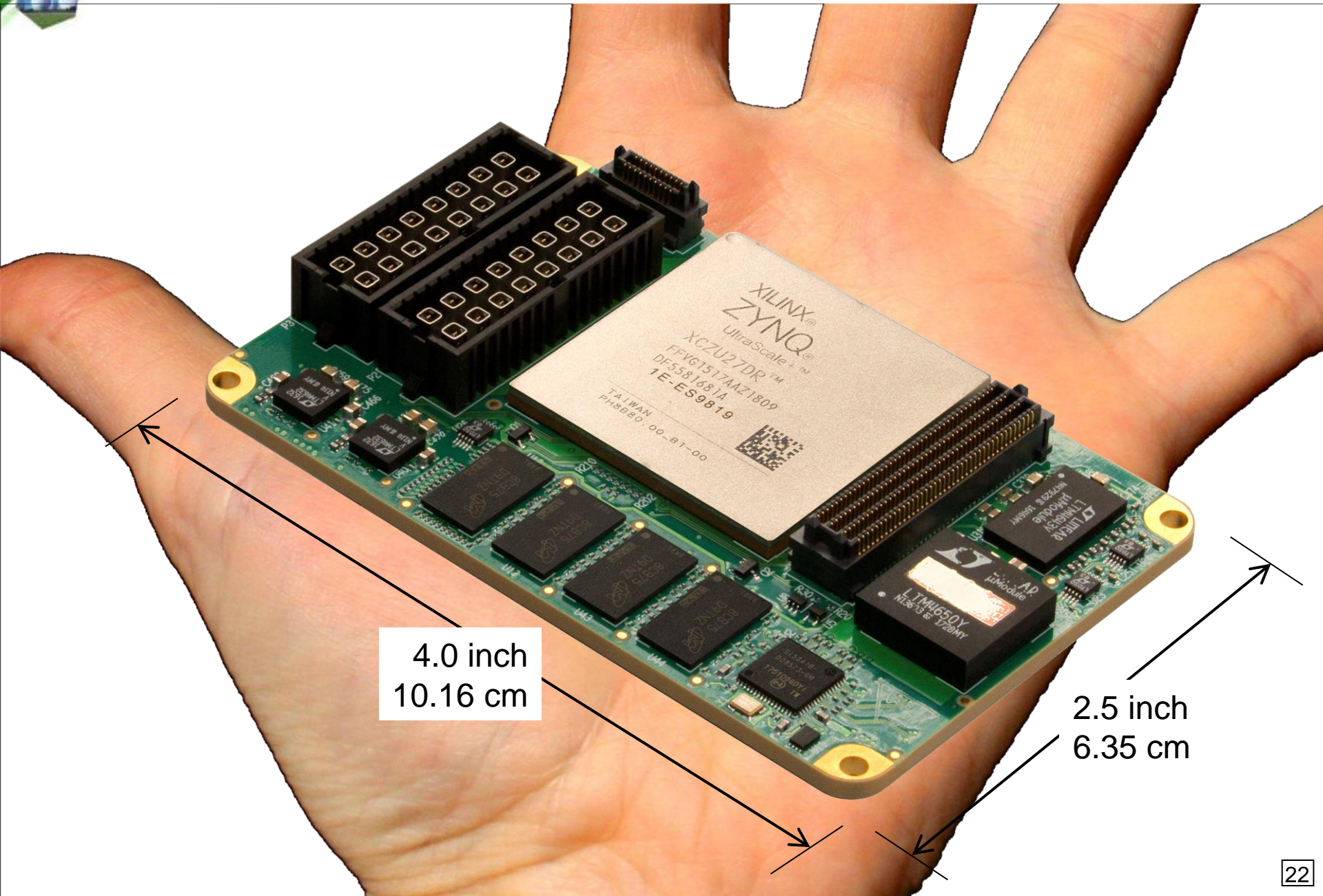
XMC Products



FMC Products



QuartzXM: RFSoC eXpress Module



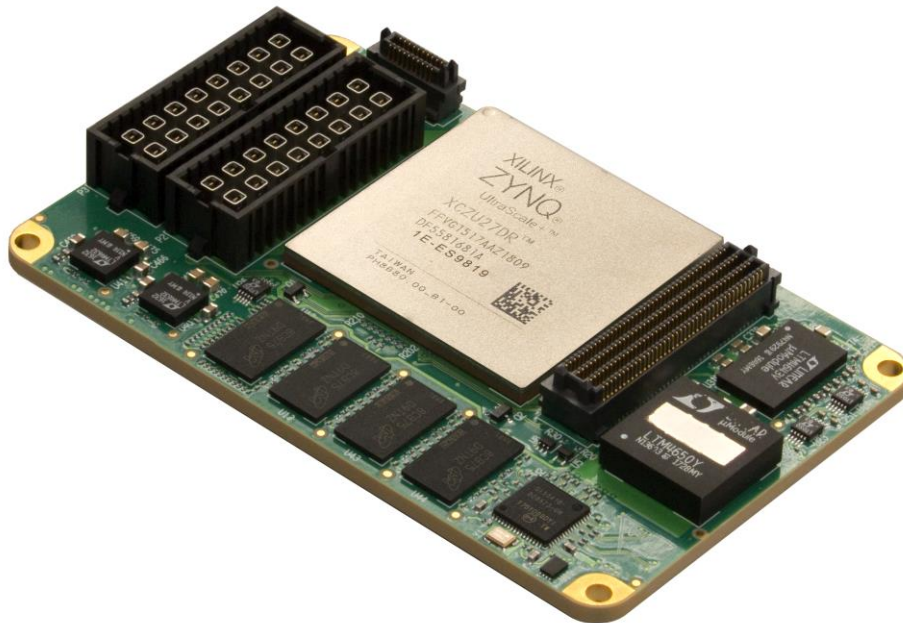
4.0 inch
10.16 cm

2.5 inch
6.35 cm



Benefits of the RFSoc Module Concept

- Mezzanine module simplifies and speeds RFSoc product designs
- Connectorizes & preserves integrity of RF and gigabit serial signals
- Generates all 13 RFSoc power supplies from a single +12V input
- Includes FLASH and DDR4 memories for FPGA & ARM processor
- Maintains PCB constraints for bypassing, filtering, & geometries
- Includes clock management and health monitoring facilities
- Excellent path for addressing SWaP requirements

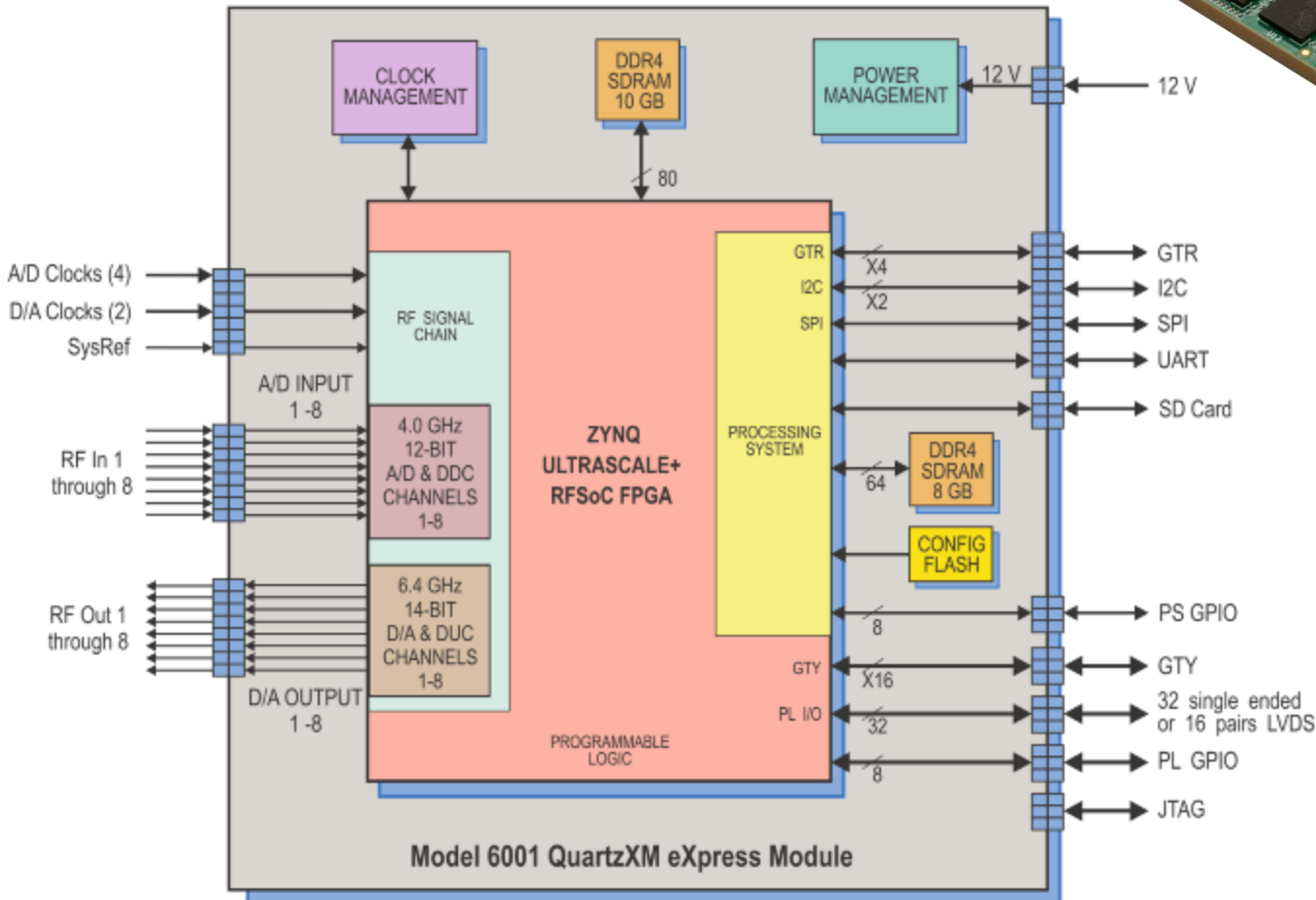
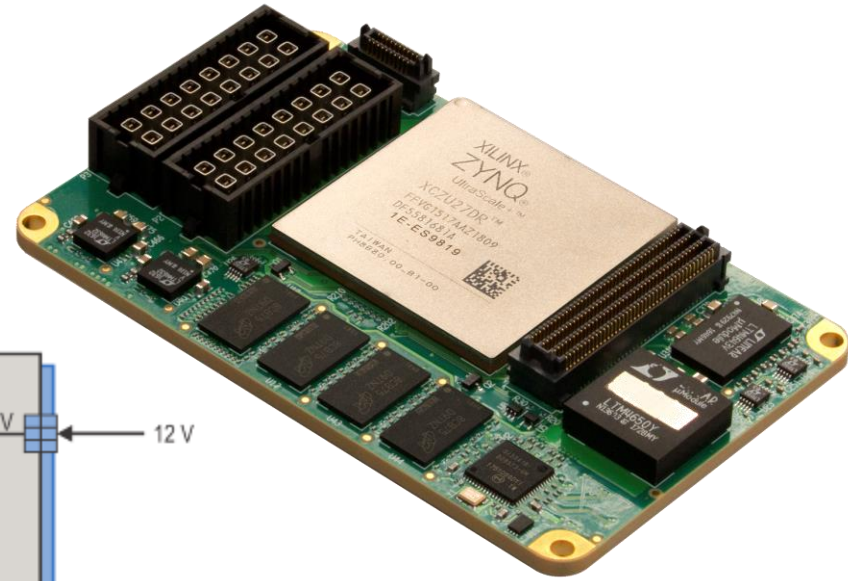


- Some technical details:
 - 28 layer PCB
 - Over 4000 drilled holes
 - Uses advanced PCB fabrication techniques including: *sequential lamination, backdrilling, blind and buried vias, etc.*
 - Supports 28Gbps GTY serial interfaces



Model 6001 - QuartzXM RFSoc Module

- Contains all the infrastructure circuitry to support the RFSoc

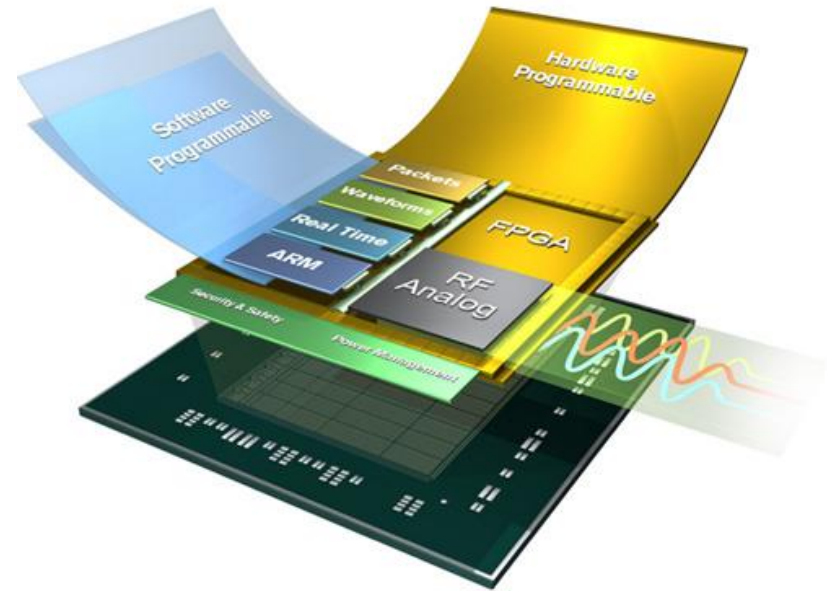


- Power supplies and power management
- Clock management
- DDR4 SDRAM for both the FPGA fabric and processors
- Configuration FLASH
- Connectors for bringing ALL RFSoc signals to a carrier board



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VPX Standards for Embedded Systems

■ VITA 66.x Optical Backplane I/O

- Several full- and half- width blind-mate optical connector types
- Provides high bandwidth data paths between boards and chassis



Photo: Elma

■ VITA 67.x Coax Backplane I/O

- Several multi-position connector types – up to 12 coax signals
- RF signal bandwidths to 40 GHz
- Eliminates front panel signal cables



Photo: SV Microwave

■ VITA 65.0 & 65.1 OpenVPX - 2017

- Most popular MIL-AERO standard for deployed systems
- Major enhancements reflect widespread use and adoption of OpenVPX
- New Card, Slot and Backplane Profiles
- Radial Backplane Clock distribution ensures precision timing and synchronization across boards
- Provision for a 100 MHz reference clock
- New definitions of combinations of VITA 66.x optical and VITA 67.x coaxial backplane I/O

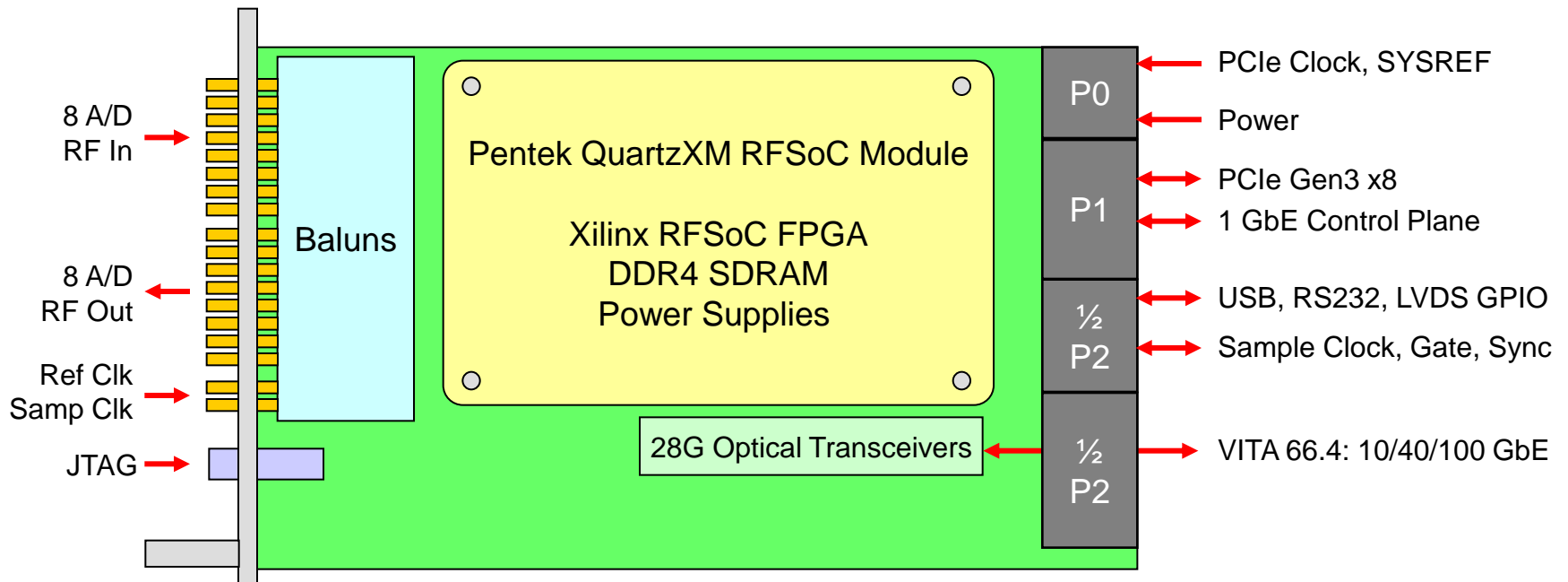


Photo: TE Connectivity



QuartzXM on 3U VPX – Front Analog I/O

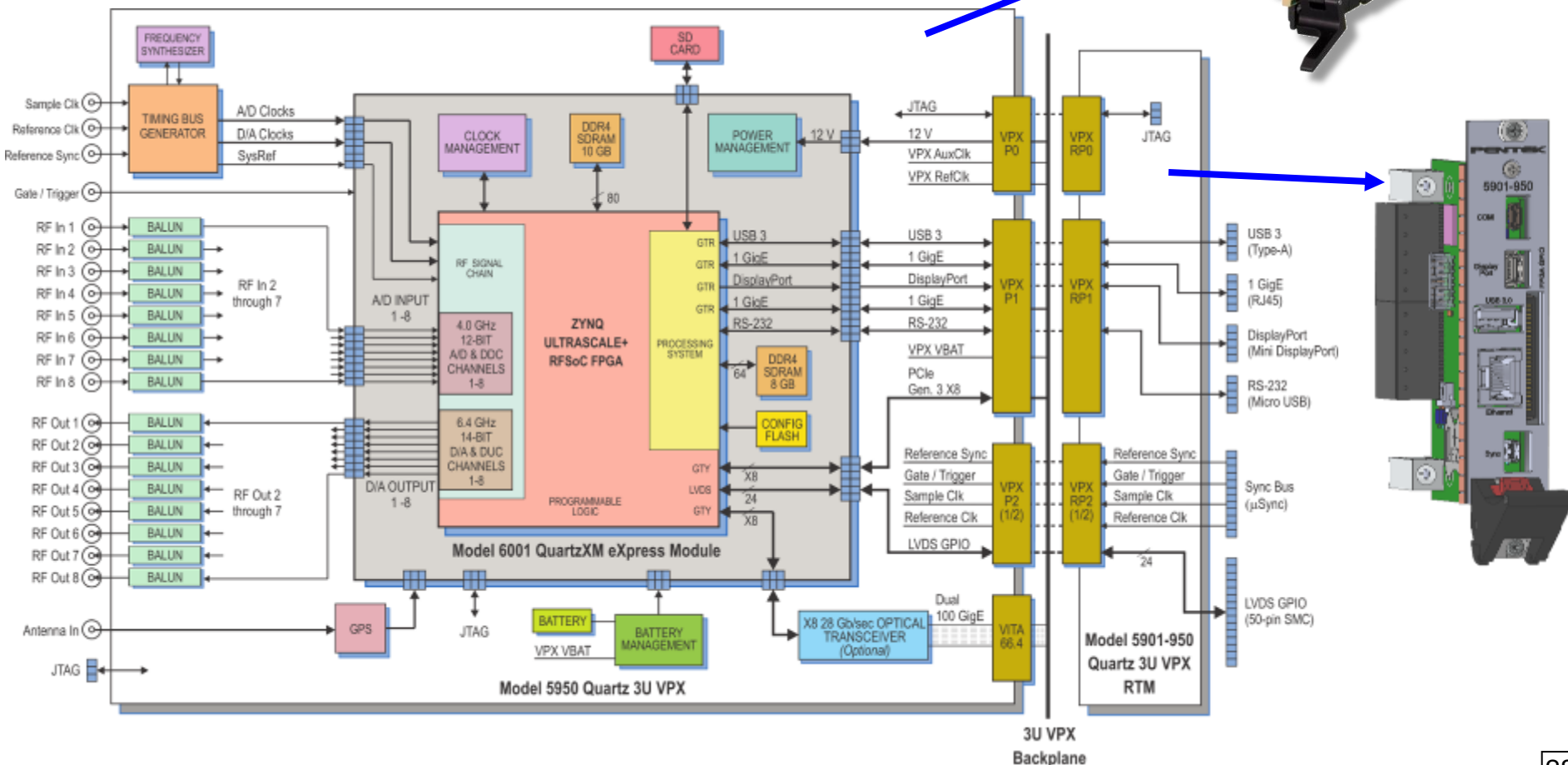
- Model 5950 3U VPX Carrier for QuartzXM RFSoc Module
- Open Architecture Form Factor Supporting Industry Standards
 - VITA 65.1 OpenVPX
 - VITA 66.4 Optical Serial Backplane I/O
- Complete functional sub-system on one 3U VPX module
- Scales easily to support high-channel count systems
- Synchronization across multiple modules





Model 5950 Quartz 3U VPX

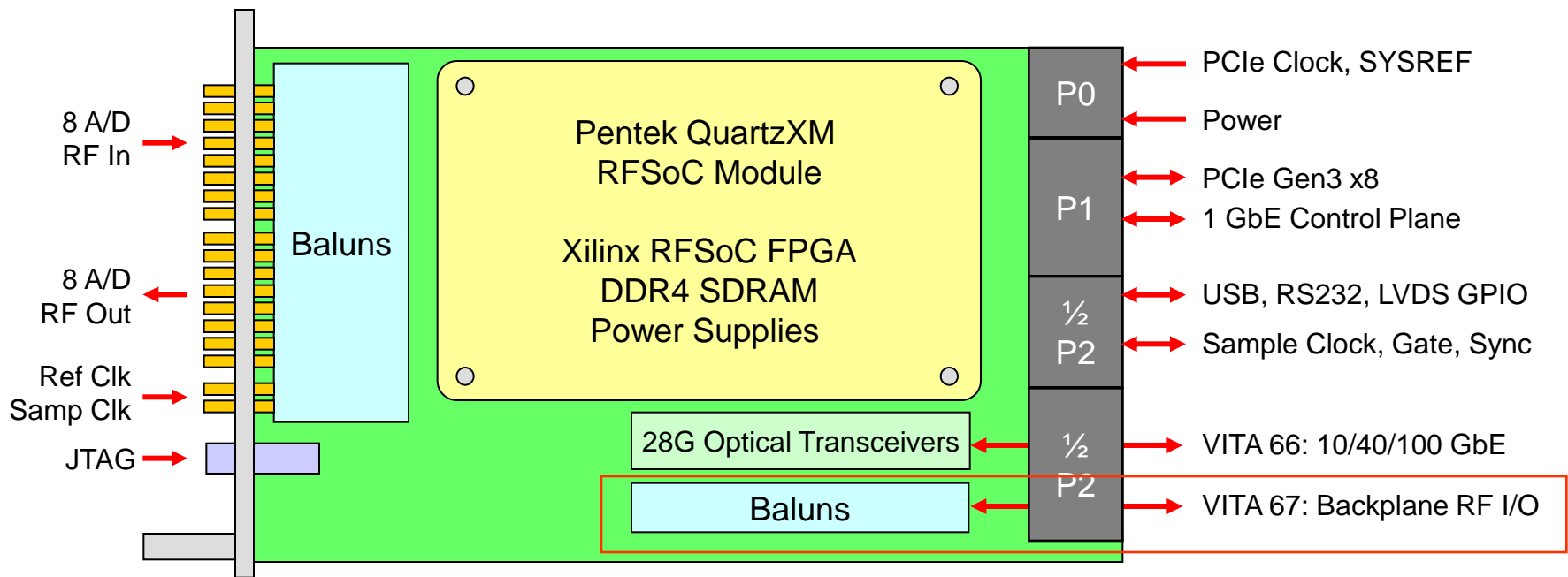
- 3U VPX Carrier provides Coaxial RF Front Panel I/O
- Rear Transition Module provides ARM processor I/O
- Air- and Conduction-cooled Versions





QuartzXM for 3U VPX – Backplane RF I/O

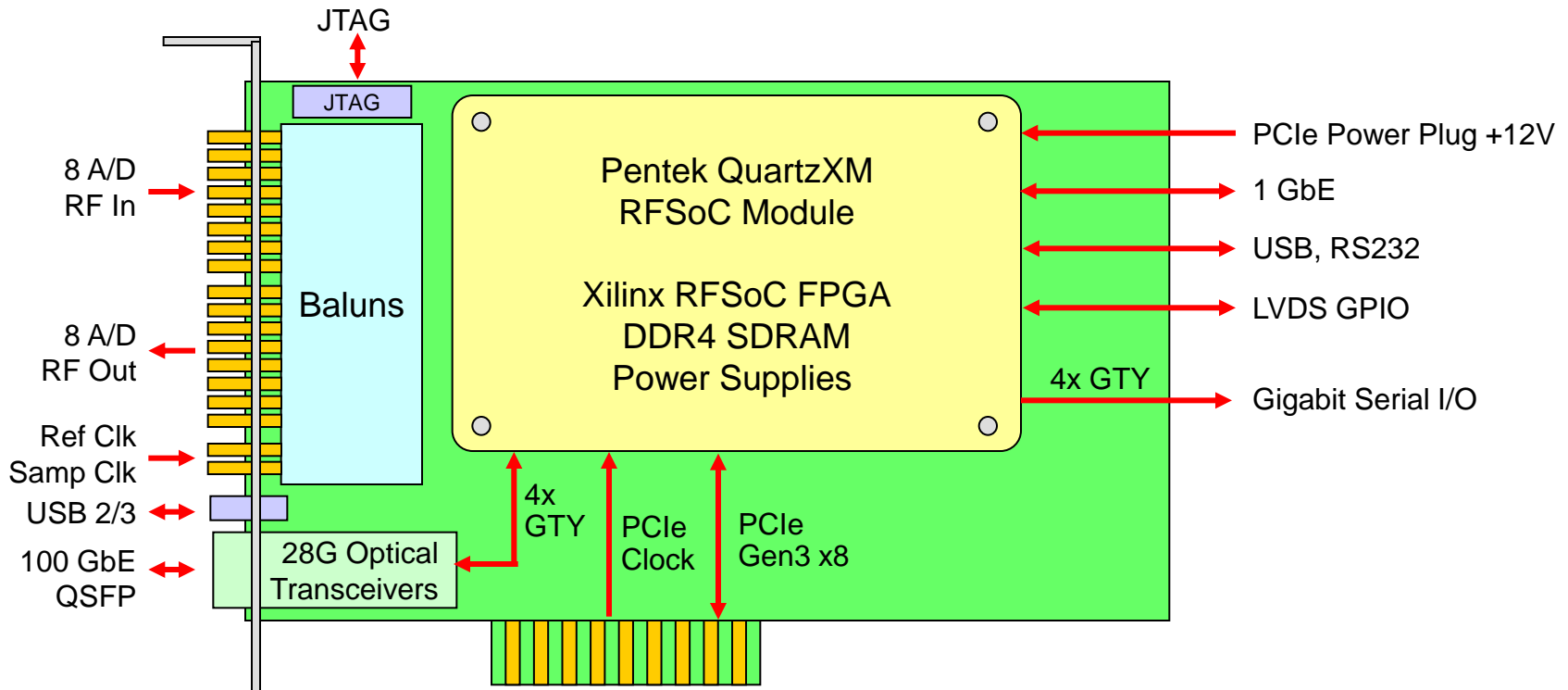
- Similar to Model 5950 except analog RF I/O connects through backplane
- VITA 67 defines several possible RF backplane connector formats
- Simplifies system integration and maintenance tasks
- Improves reliability by eliminating cables





QuartzXM on PCIe Carrier for PC Platform

- Allows RFSoc development tasks in a low cost PC platform
- Perfect for software and FPGA development seats
- Perfect for continuation engineering and support
- Supports deployed applications for benign environments





Model 4801: QuartzXM Carrier Design Package

- All documentation needed for a customer to design his own carrier for the Model 6001 QuartzXM RFSoc Module
 - Pin definitions and electrical specifications of all signals on the QuartzXM
 - 3D mechanical models
 - Thermal profiles of the module and components
 - Carrier reference design schematics
 - PCB stack-up recommendations
 - PCB design guidelines and routing rules
 - Operating system and bootstrap guidelines
 - Additional electrical and mechanical engineering guidance
- Carrier Design Package purchase requires an NDA





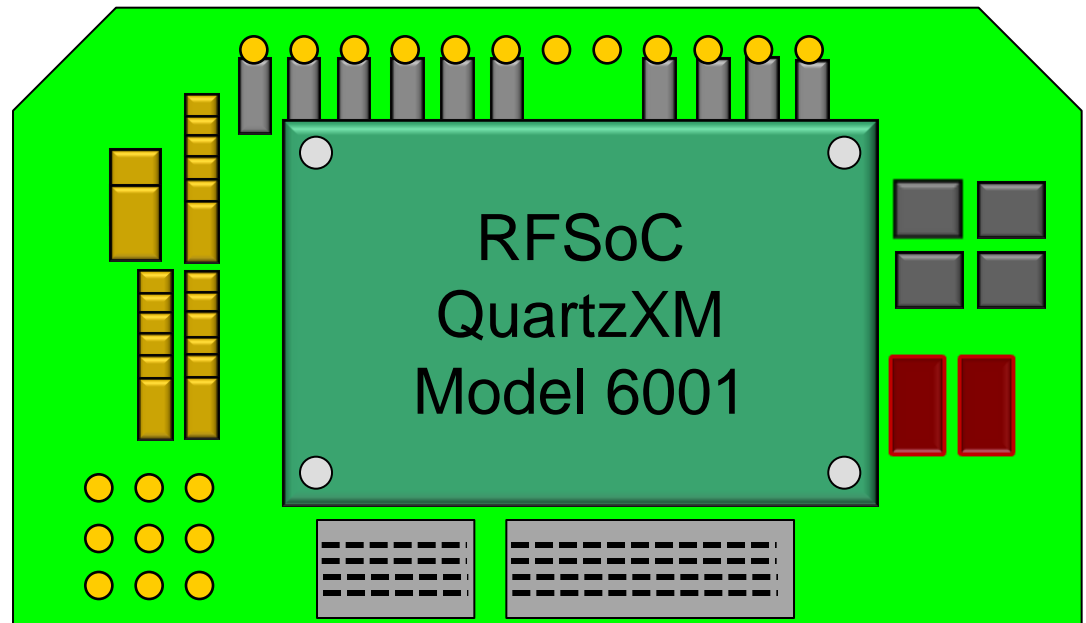
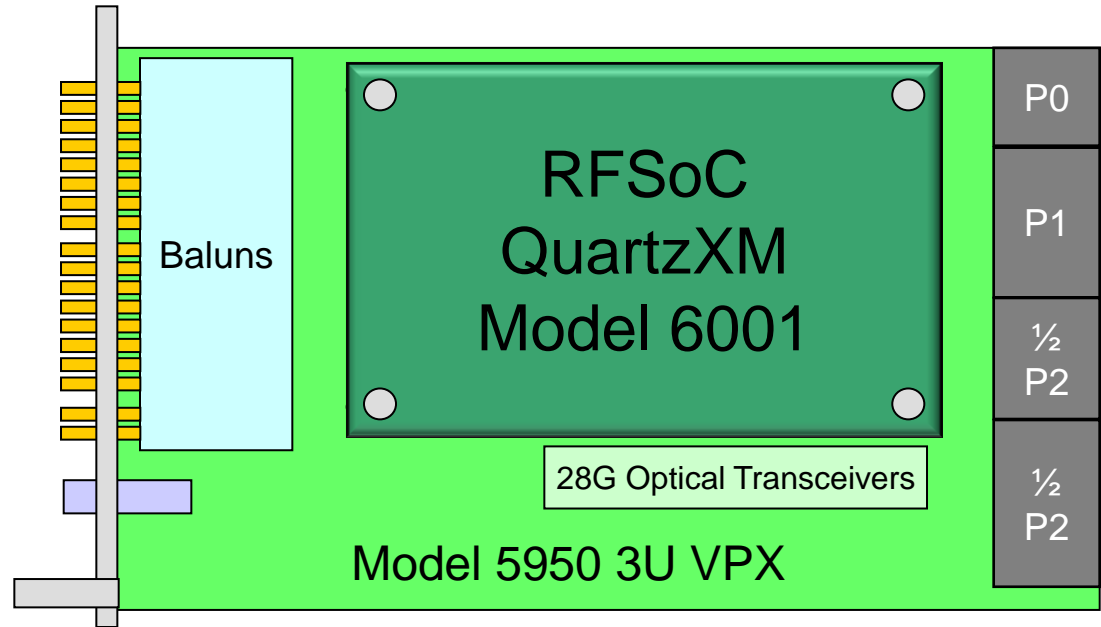
Migrating QuartzXM to Custom Platforms

■ Development Strategy

- Start with standard open-architecture product like 5950
- Develop software and IP for custom form factor application

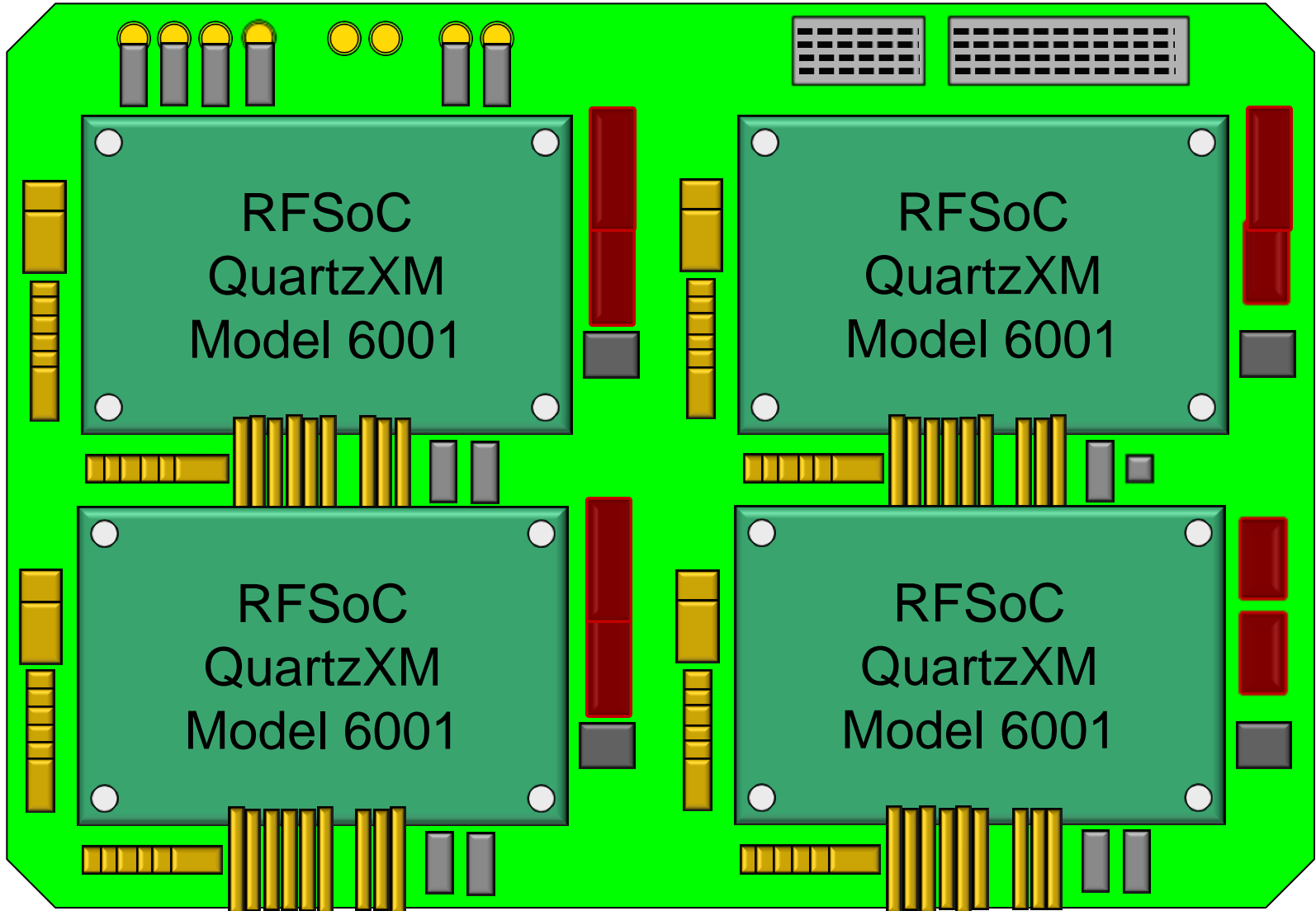
■ Custom Carrier

- Use Pentek Model 4801 Carrier Design Package
- Pin definition, design rules, layout guidance and design review
- Attach QuartzXM Module
- Keep 5950 as a development platform



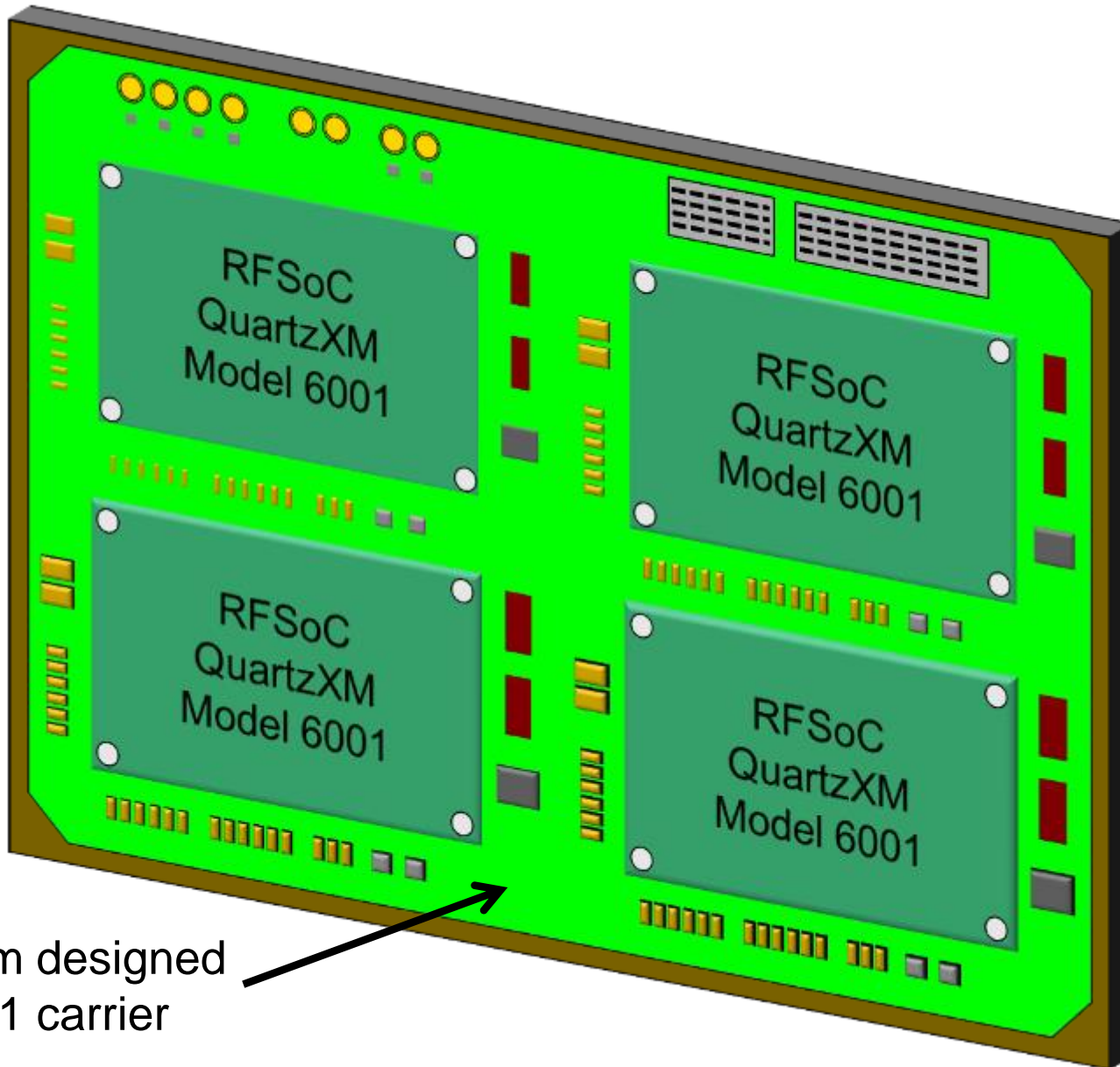


Custom QuartzXM RFSoc Module Solutions





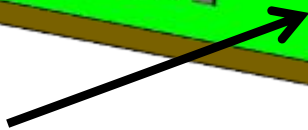
Custom QuartzXM RFSoC Module Solutions



Customer's
8 x 4 antenna
array



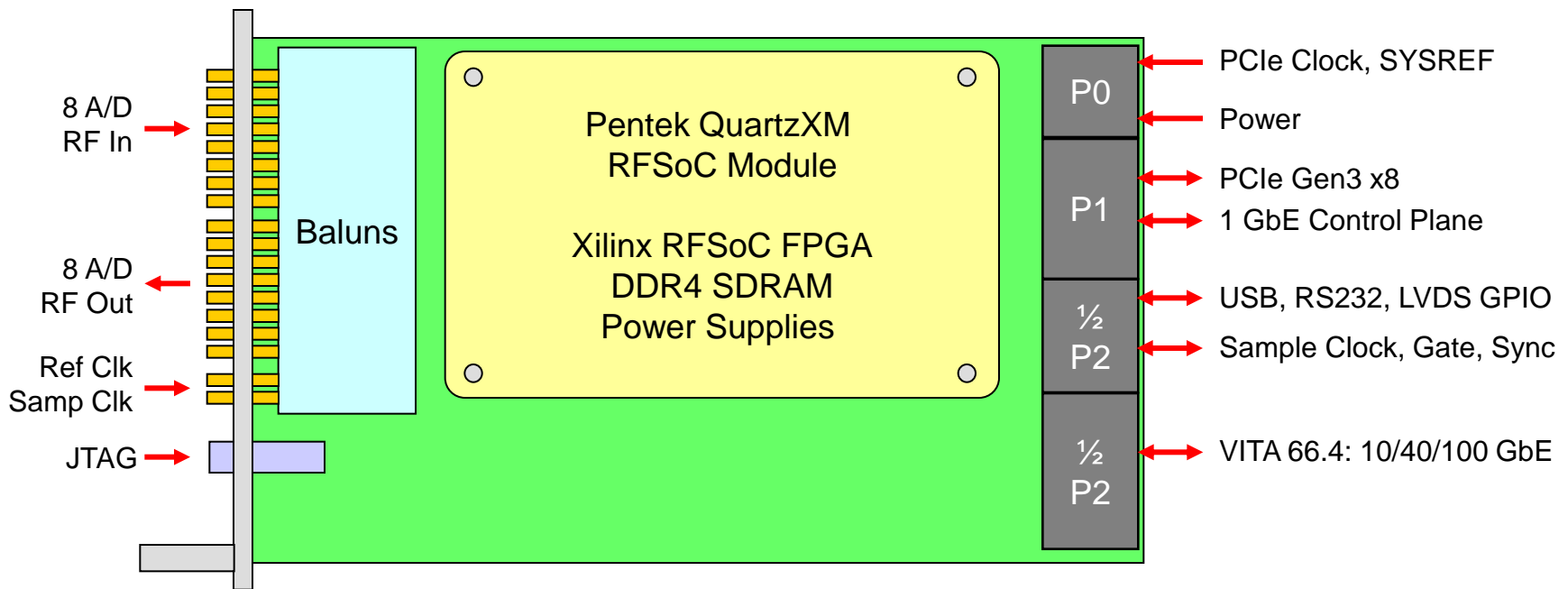
Custom designed
6001 carrier





Small Form Factor Remote Box

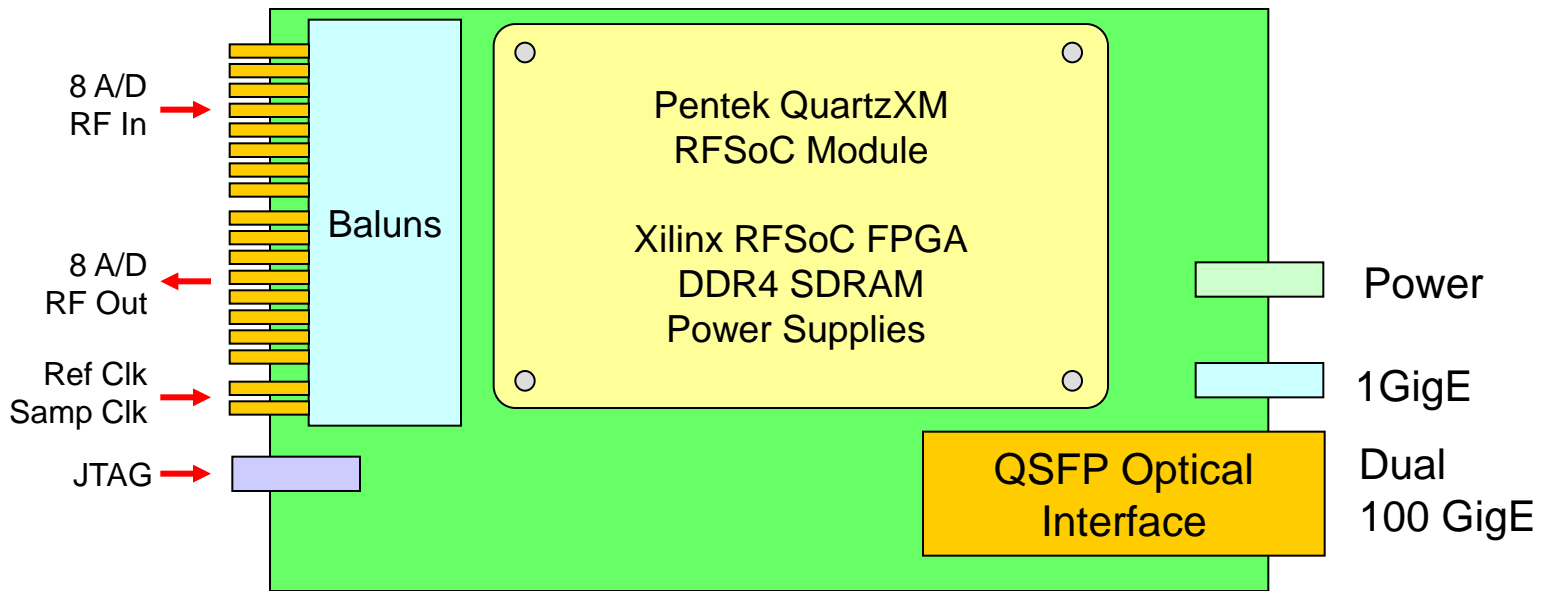
- Create or adapt an existing carrier for the QuartzXM module
- For example, start with the Model 5950 3U VPX board
- Modify the PCB design to remove VPX connectors & hardware





Small Form Factor Remote Box

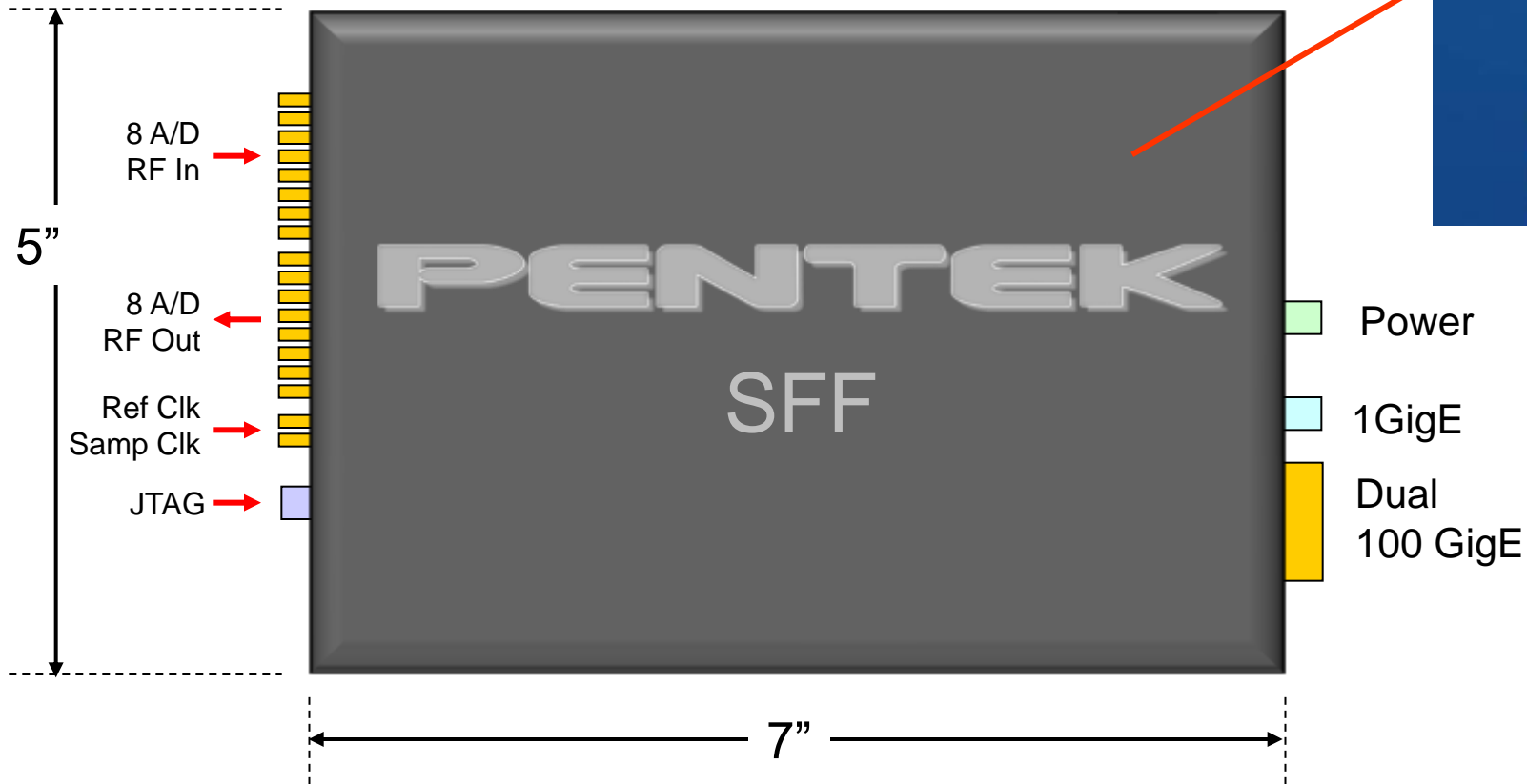
- Add connectors appropriate for the application





Small Form Factor Remote Box

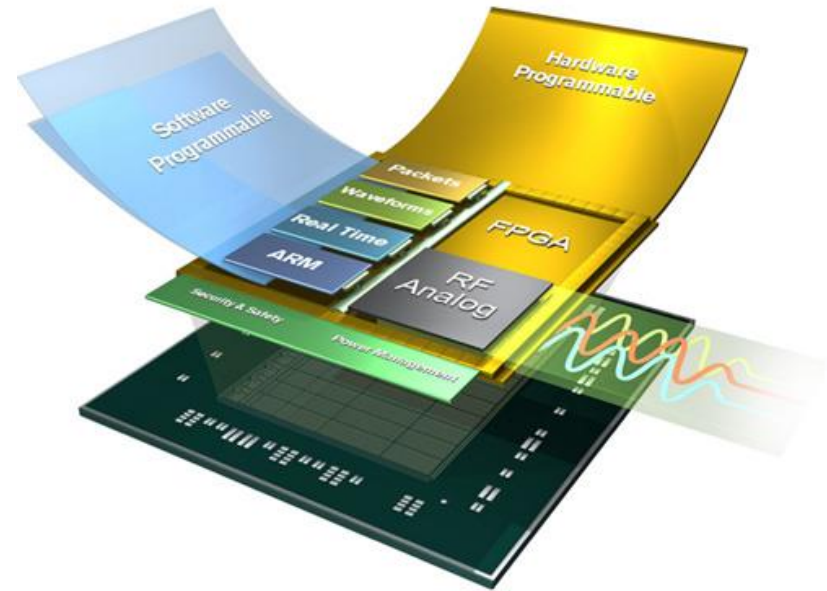
- Install it within a suitable SFF sealed enclosure
- Mount the unit on a mast near the antenna
- Complete 8-channel RF transceiver sub-system





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FPGA Design Strategies for RFSoc



■ Xilinx Vivado Tool Suite

- Vivado IP Integrator
 - Graphical Design Entry Tool
- Vivado AXI-4 IP Library Modules
 - Standardized for compatibility
- Vivado High-Level Synthesis
 - Generates RTL from C & C++
- Vivado Simulator
 - Design Verification
- TCL Tool Command Language
 - Scripting language

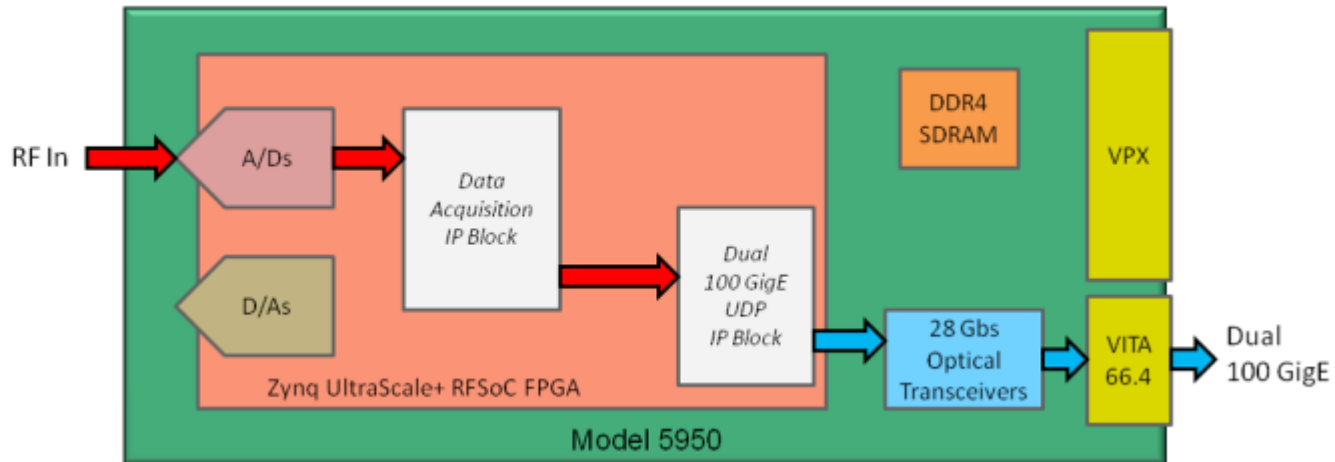
■ Pentek Navigator FDK for RFSoc

- Complete Vivado Project Folder
 - All files included ready for development
- Full AXI-4 Compliant IP Library
 - Full IP Source code included
- Pentek FPGA Resource Modules
 - DMA controllers, triggering & gating
 - Timing & synchronization
 - 100 GbE engines
- Factory Installed RFSoc Applications
 - Radar & Data Acquisition
 - Waveform Generation

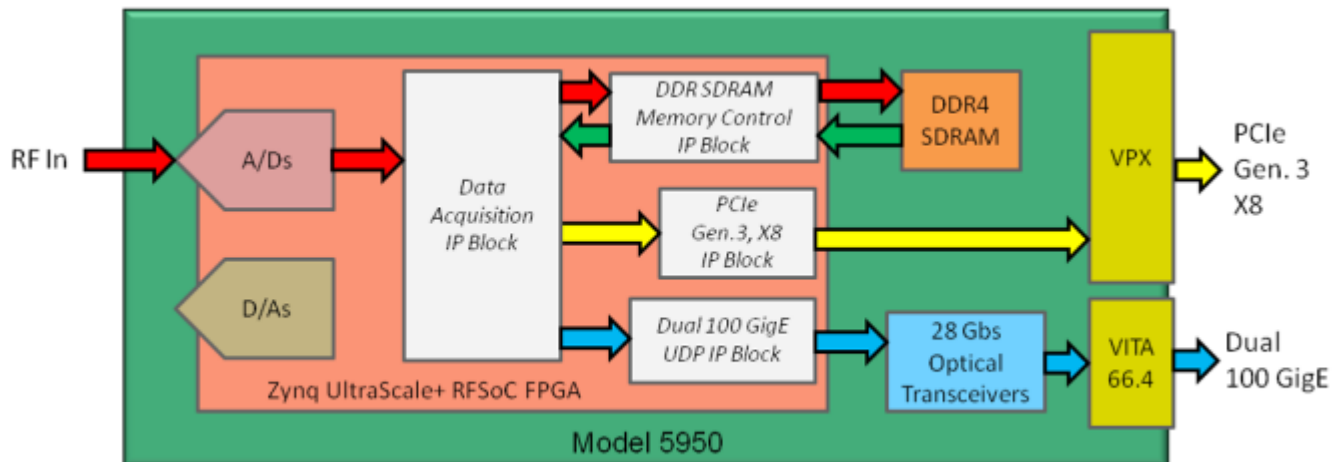


Included RFSoc Starter Applications

A/D Acquisition Engine to 100 GbE Optical Streaming



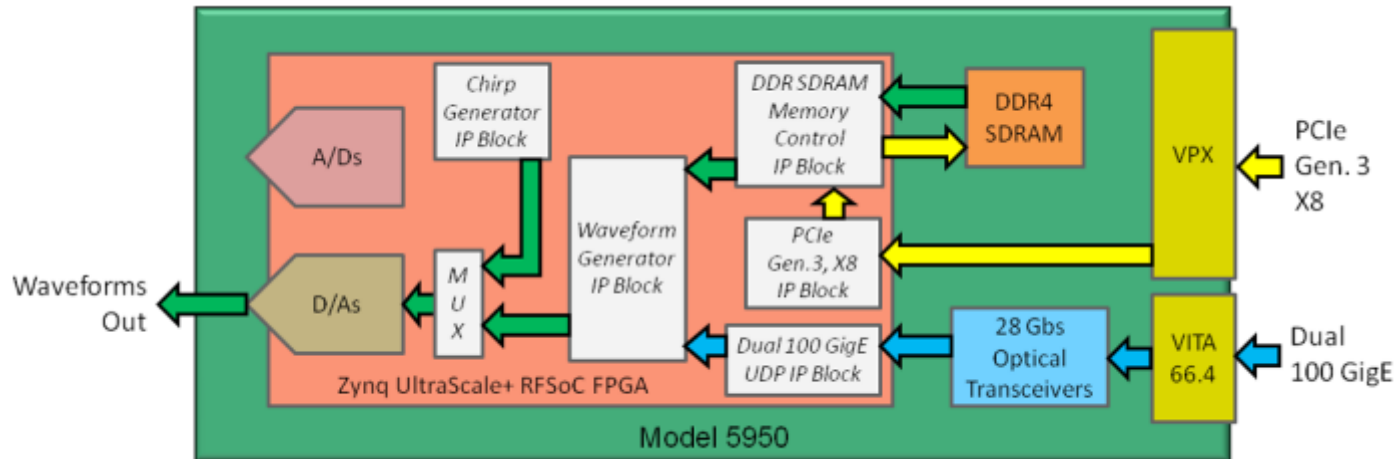
Multi-mode Acquisition to Delay Memory, PCIe, or GbE





Included RFSoc Starter Applications

Waveform Generator from Memory, PCIe, or 100 GbE



■ Benefits of Pentek Factory-Installed Starter Applications

- Installed IP provides immediate demonstrations of several typical applications
- Customer can start by modifying these applications to develop custom applications
- Starter applications serve as a reference for trouble shooting during development



Software Design Strategies for RFSoc



■ Xilinx Vivado Tools for RFSoc

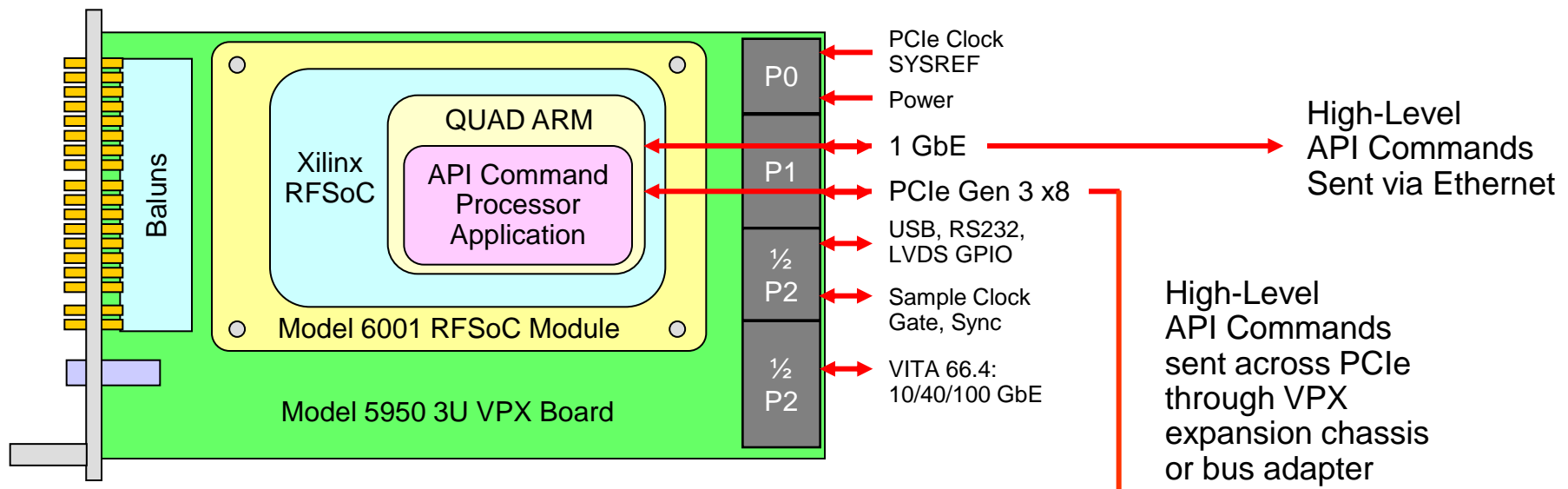
- Xilinx RFSoc ARM SDK
 - Complete Integrated Design Environment (IDE) interfaces to Vivado FPGA tools
 - Multi-processor hardware/software co-debug capabilities
 - Editor, compilers, build tools, flash memory management
 - Libraries and device drivers
 - Xilinx Software Command Line Tool (XSCT) for scripting
- Xilinx PetaLinux
 - Linux OS for ARM Processor
 - Linux Tools and Utilities

■ Pentek Navigator BSP for RFSoc

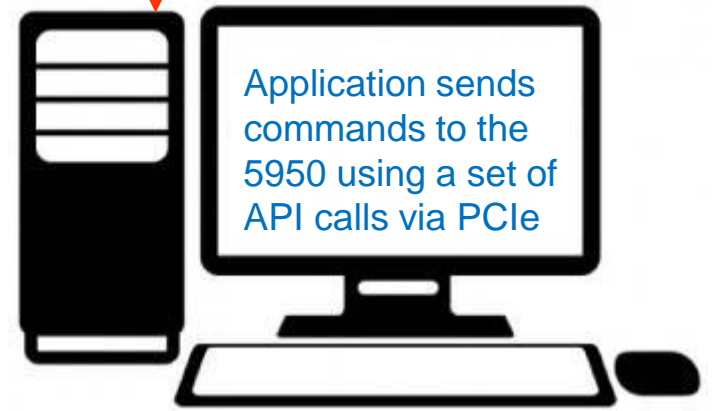
- Navigator command processor
 - RFSoc ARM command processor application executes high-level API commands from PCIe or Ethernet
- Powerful Tool Suite
 - Initialization and control of all FPGA IP
 - Delivery of all operational parameters
 - High-Level C-Language Libraries
 - Full C Source Code Provided
 - Numerous Program Code Examples
 - Device Drivers for Windows & Linux
- Signal Viewer Utility
 - Displays acquired signals on virtual spectrum analyzer and oscilloscope



Flexible API Command Processing



- ARM Processor on QuartzXM runs the Pentek Navigator RFSoc API Command Processor
- Accepts API commands across Ethernet
- Accepts API commands across PCIe bus
- Flexible options for different system architectures

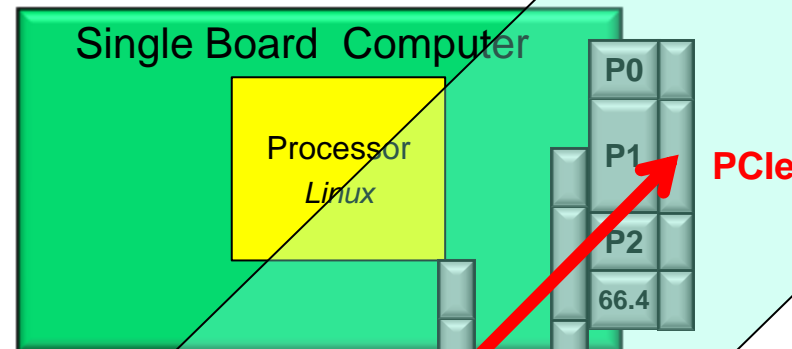
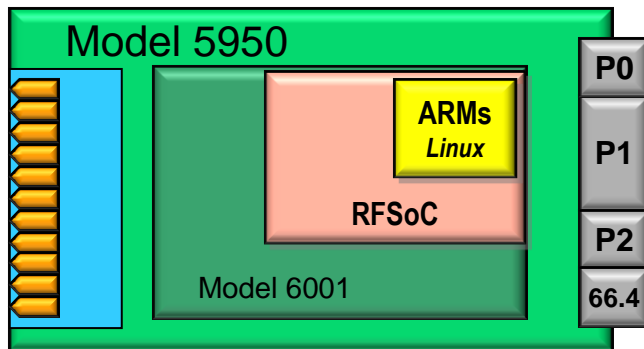




Multiboard 3U VPX System Architectures

Model 5950 3U VPX PCIe Interface can be configured as a Root Complex

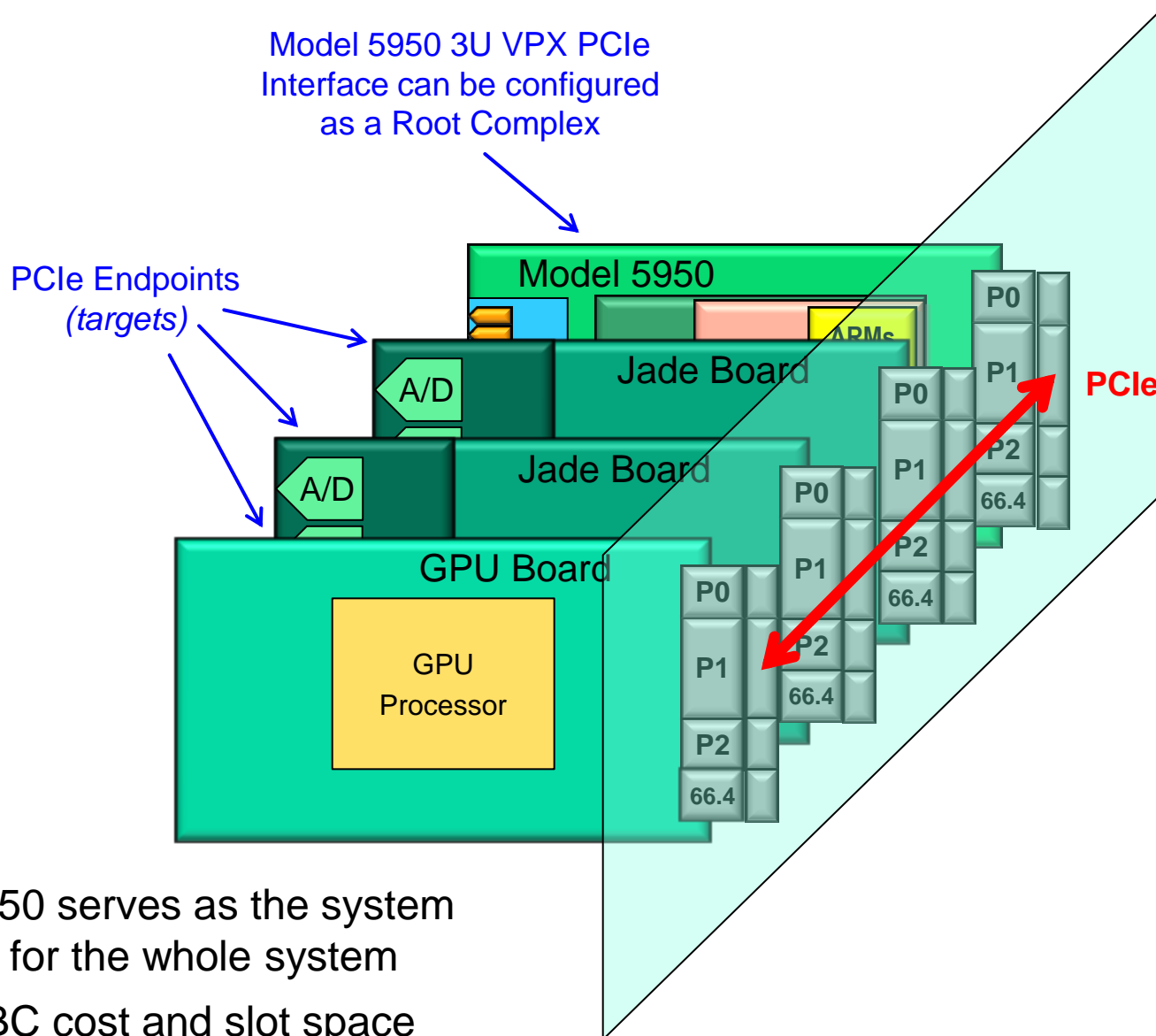
PCIe Root Complex (system controller)



- Most VPX systems use a SBC as the system controller
- Model 5950 Quartz 3U VPX board can configure the ARM processor to replace the SBC



Multiboard 3U VPX System Architectures

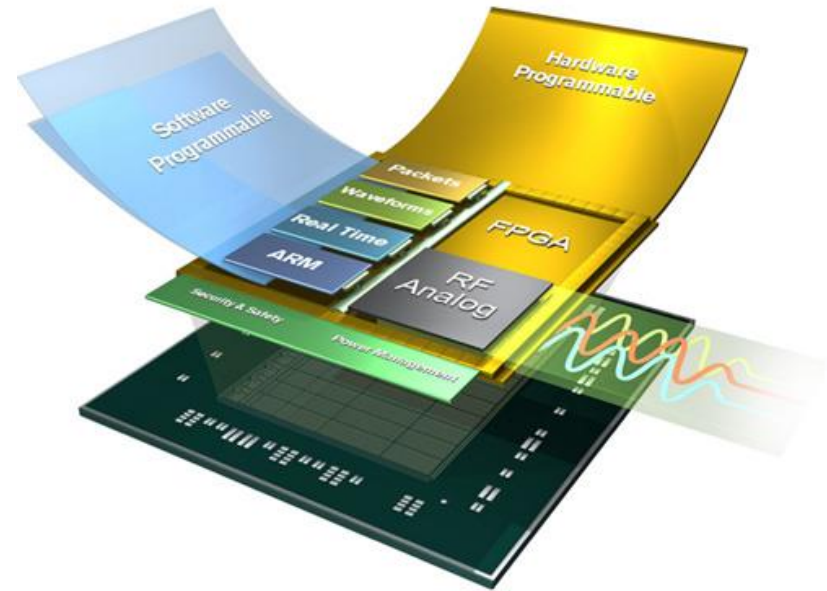


- Model 5950 serves as the system controller for the whole system
- Saves SBC cost and slot space



Topics

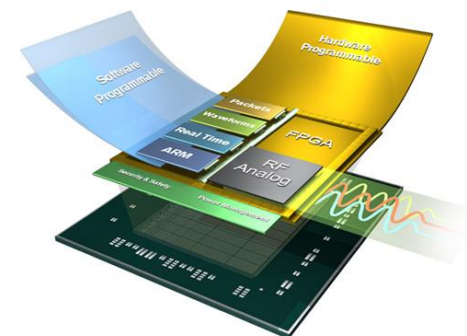
- Xilinx RFSoc Overview
- Impact of Latency on Applications
- RFSoc Market Opportunities
- RFSoc Design Challenges
- RFSoc Module Concept:
- Deployment Platforms for RFSoc
- FPGA IP Development Strategies
- ARM Software Development Strategies
- Summary





RFSoc Deployment Strategies

- **Xilinx RFSoc Offers Extreme Integration**
 - A/D, D/A, FPGA, ARM Processor, Flexible I/O
 - Low Latency for wideband RF signals
- **Pentek QuartzXM Simplifies System Design**
 - Complete RFSoc infrastructure with DDR4, clock management, & power supplies
 - High performance RF and digital connectors
 - Small footprint for high density applications
- **Xilinx Vivado Tools**
 - FPGA development tools
 - ARM processor OS and development tools
- **Pentek Navigator FDK and BSP Tools**
 - API command processor for ARM
 - Factory installed FPGA IP modules for timing, DMA controllers, PCIe, memory controllers
 - FPGA IP AXI-4 library functions
 - Four starter application examples installed
- **Speeds development cycles, saves costs**





Thank you! For More Information.....

- Visit www.pentek.com/RFSoc
- Data Sheets
 - [Model 5950 3U VPX RFSoc Board](#)
 - [Model 6001 QuartzXM Module](#)
- Whitepaper
 - [Xilinx's Zynq UltraScale+ RFSoc](#)
- Pentek Pipeline Summer 2018
 - [Strategies for Deploying RFSoc](#)
- [Live Signal Acquisition Video](#)
 - Shows A/D acquisition using ARM-based API Command Processor

Model 5950 8-Channel A/D & D/A Zynq UltraScale+ RFSoc Processor - 3U VPX

General Information

The Quartz Model 5950 is a high performance 3U VPX board based on the Xilinx Zynq UltraScale+ RFSoc FPGA. The RFSoc integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip. The Model 5950 brings RFSoc performance to 3U VPX with a complete system on a board.

A/D Converter Stage

The front end acquires analog RF or RF

Model 6001 8-Channel A/D & D/A Zynq UltraScale+ RFSoc Processor - QuartzXM

General Information

The Quartz Model 6001 is a high performance Quartz Express Module (QuartzXM) based on the Xilinx Zynq UltraScale+ RFSoc FPGA. The RFSoc FPGA integrates eight RF-class A/D and D/A converters into the Zynq's multiprocessor architecture, creating a multichannel data conversion and processing solution on a single chip.

The Model 6001 has been designed to bring RFSoc performance to a wide range of

Features

- Support UltraScale
- 18 GB of DRAM
- On-board PCI Exp. interface
- LVDS or Zynq UI (customer)
- Optima interface (optional)
- Dual 10 interface
- Compact VITA as VITA-46 (66.4 V) (Quartz Specific)
- Ruggedized and conduction cooled
- Unique Module other I/O

Features

- Unique QuartzXM Module available in custom form
- Supports Xilinx UltraScale+ RFSoc
- 18 GB of DRAM
- LVDS connected Zynq UltraScale+ custom I/O
- GTF connector serial communication
- Ruggedized and conduction cooled available
- Includes a complete IP functions and applications

Strategies for Deploying Xilinx's Zynq UltraScale+ RFSoc

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In This Issue

- Feature: Using terms like "disruptive" and "breakthrough" to describe new technology can sound like advertising hype, but in the case of RFSoc, such a description is true. Our feature article explores how to best use the advantages of this technology.

Strategies for Deploying Xilinx's Zynq UltraScale+ RFSoc
by Bob Spandora

What is RFSoc?

On February 21st, 2017, Xilinx announced the introduction of a new technology called RFSoc, with the rather dramatic headline: **Xilinx Unveils Disruptive Integration and Architectural Breakthrough for 5G Wireless with RF-Class Analog Technology**. The proposition was simple: add RF-class analog to digital and digital to analog data converters to Xilinx's already powerful MPSoC, ARM processor enhanced family of high performance FPGAs. And while the concept was simple, the implications were profound, changing the way engineers could design and package small, high channel count systems. And this technology not only offers new possibilities for 5G applications, but has significant impact in military and scientific systems, justifying the claim in Xilinx's announcement. To get better appreciation of the capabilities of RFSoc and understand how to best use the advantages of this technology, it's worth taking a quick look at current trends in data converters and signal processing.

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Live Signal Acquisition: Quartz Model 5950 and Model 6001 RFSoc boards